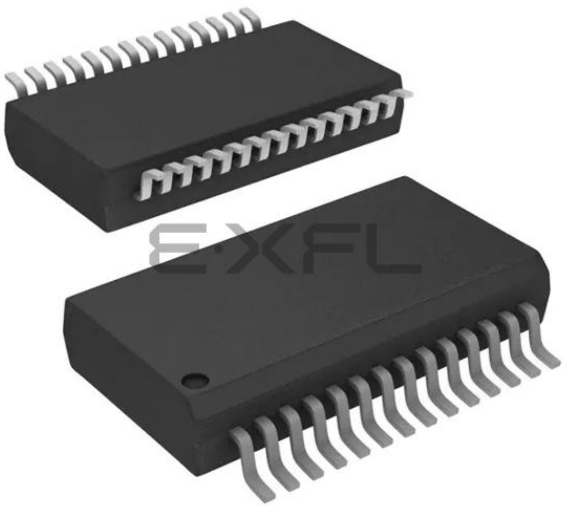

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## What is "Embedded - Microcontrollers"?

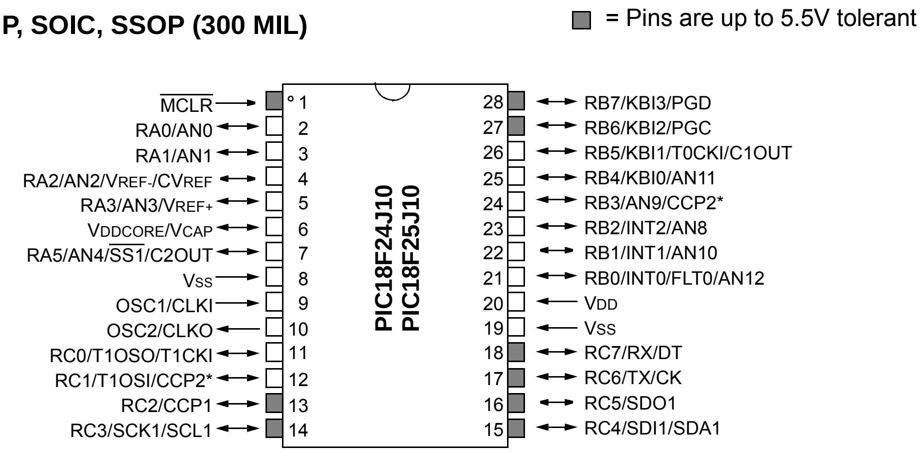
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 16KB (8K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18lf24j10-i-ss |

## Pin Diagrams

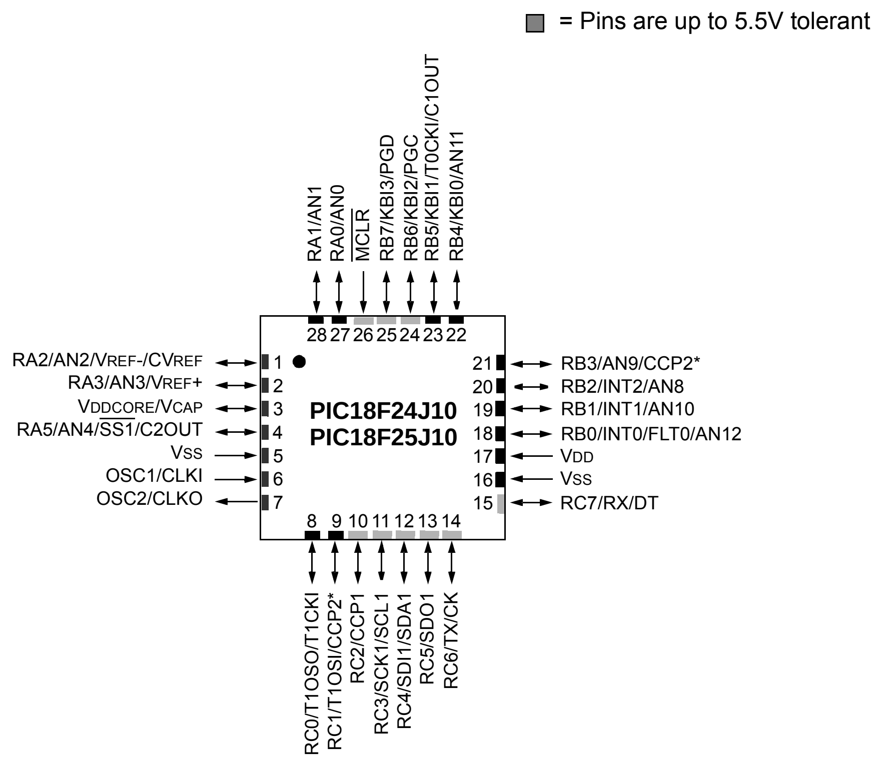
**28-Pin SPDIP, SOIC, SSOP (300 MIL)**




* Pin feature is dependent on device configuration.

.

**28-Pin QFN**




* Pin feature is dependent on device configuration.

## Table of Contents

**TABLE 1-3: PIC18F44J10/45J10 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTE is a bidirectional I/O port. |
| RE0/$\overline{RD}$/AN5 | 8 | 25 | 25 | | | |
| RE0 | | | | I/O | ST | Digital I/O. |
| $\overline{RD}$ | | | | I | TTL | Read control for Parallel Slave Port (see also $\overline{WR}$ and $\overline{CS}$ pins). |
| AN5 | | | | I | Analog | Analog input 5. |
| RE1/$\overline{WR}$/AN6 | 9 | 26 | 26 | | | |
| RE1 | | | | I/O | ST | Digital I/O. |
| $\overline{WR}$ | | | | I | TTL | Write control for Parallel Slave Port (see $\overline{CS}$ and $\overline{RD}$ pins). |
| AN6 | | | | I | Analog | Analog input 6. |
| RE2/$\overline{CS}$/AN7 | 10 | 27 | 27 | | | |
| RE2 | | | | I/O | ST | Digital I/O. |
| $\overline{CS}$ | | | | I | TTL | Chip Select control for Parallel Slave Port (see related $\overline{RD}$ and $\overline{WR}$ pins). |
| AN7 | | | | I | Analog | Analog input 7. |
| $V_{SS}$ | 12, 31 | 6, 30, 31 | 6, 29 | P | — | Ground reference for logic and I/O pins. |
| $V_{DD}$ | 11, 32 | 7, 8, 28, 29 | 7, 28 | P | — | Positive supply for logic and I/O pins. |
| $V_{DDCORE}$/$V_{CAP}$ | 6 | 23 | 23 | | | |
| $V_{DDCORE}$ | | | | P | — | Positive supply for logic and I/O pins. |
| $V_{CAP}$ | | | | P | — | Ground reference for logic and I/O pins. |
| NC | — | 13 | 12, 13, 33, 34 | — | — | No connect. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

### 4.4.1 PRI_IDLE MODE

This mode is unique among the three low-power Idle modes, in that it does not disable the primary device clock. For timing-sensitive applications, this allows for the fastest resumption of device operation with its more accurate primary clock source, since the clock source does not have to “warm up” or transition from another oscillator.

PRI_IDLE mode is entered from PRI_RUN mode by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then set the SCS<1:0> bits to ‘10’ and execute SLEEP. Although the CPU is disabled, the peripherals continue to be clocked from the primary clock source specified by the FOSC0 Configuration bit. The OSTS bit remains set (see Figure 4-6).

When a wake event occurs, the CPU is clocked from the primary clock source. A delay of interval, TCSD, is required between the wake event and when code execution starts. This is required to allow the CPU to become ready to execute instructions. After the wake-up, the OSTS bit remains set. The IDLEN and SCS bits are not affected by the wake-up (see Figure 4-7).

### 4.4.2 SEC_IDLE MODE

In SEC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the Timer1 oscillator. This mode is entered from SEC_RUN by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then set SCS<1:0> to ‘01’ and execute SLEEP. When the clock source is switched to the Timer1 oscillator, the primary oscillator is shut-down, the OSTS bit is cleared and the T1RUN bit is set.

When a wake event occurs, the peripherals continue to be clocked from the Timer1 oscillator. After an interval of TCSD following the wake event, the CPU begins executing code being clocked by the Timer1 oscillator. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run (see Figure 4-7).

| **Note:** | The Timer1 oscillator should already be running prior to entering SEC_IDLE mode. If the T1OSCEN bit is not set when the SLEEP instruction is executed, the SLEEP instruction will be ignored and entry to SEC_IDLE mode will not occur. If the Timer1 oscillator is enabled, but not yet running, peripheral clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result. |
|---|---|

**FIGURE 4-6: TRANSITION TIMING FOR ENTRY TO IDLE MODE**

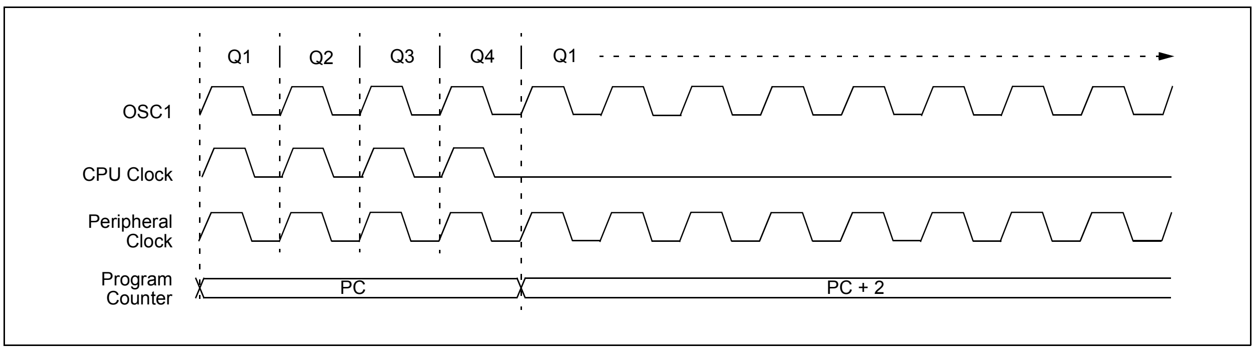
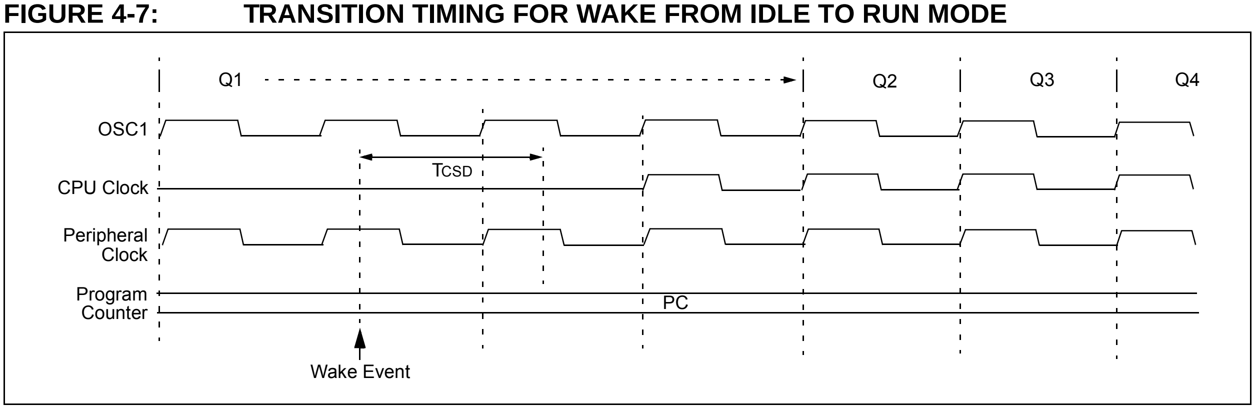



**FIGURE 4-7: TRANSITION TIMING FOR WAKE FROM IDLE TO RUN MODE**



## 7.5 Writing to Flash Program Memory

The minimum programming block is 32 words or 64 bytes. Word or byte programming is not supported.

Table writes are used internally to load the holding registers needed to program the Flash memory. There are 64 holding registers used by the table writes for programming.

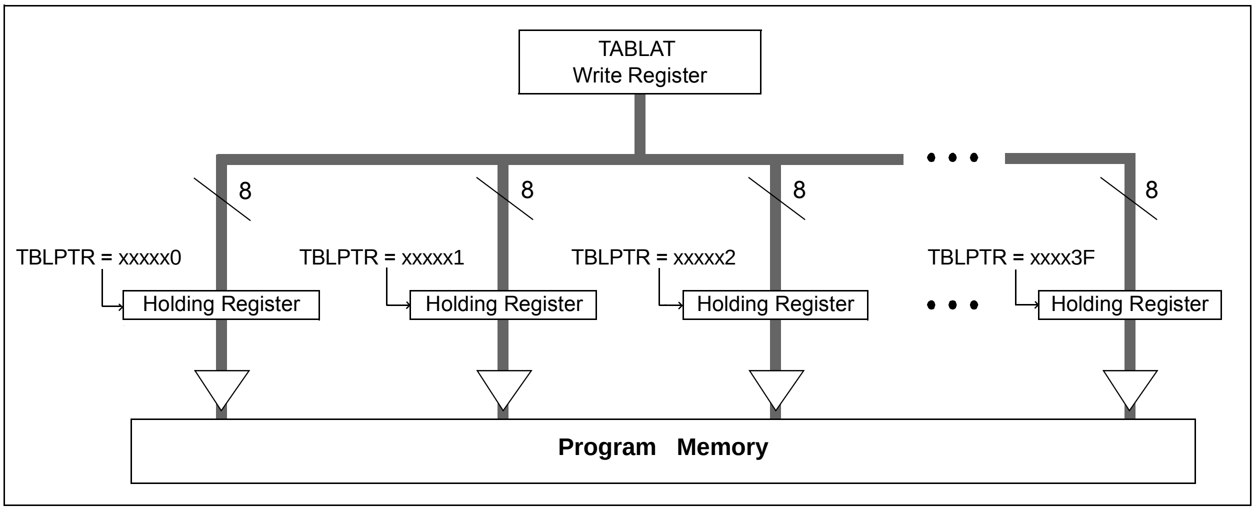
Since the Table Latch (TABLAT) is only a single byte, the TBLWTinstruction may need to be executed 64 times for each programming operation. All of the table write operations will essentially be short writes because only the holding registers are written. At the end of updating the 64 holding registers, the EECON1 register must be written to in order to start the programming operation with a long write.

The long write is necessary for programming the internal Flash. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

The EEPROM on-chip timer controls the write time. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device.

| **Note:** | Unlike previous devices, the PIC18F45J10 family of devices does not reset the holding registers after a write occurs. The holding registers must be cleared or overwritten before a programming sequence.<br><br>In order to maintain the endurance of the cells, each Flash byte should not be programmed more then twice between erase operations. Either a Bulk or Row Erase of the target row is required before attempting to modify the contents a third time. |
|---|---|

**FIGURE 7-5: TABLE WRITES TO FLASH PROGRAM MEMORY**




### 7.5.1 FLASH PROGRAM MEMORY WRITE SEQUENCE

The sequence of events for programming an internal program memory location should be:

1. If the section of program memory to be written to has been programmed previously, then the memory will need to be erased before the write occurs (see **Section 7.4.1 "Flash Program Memory Erase Sequence"**).
2. Write the 64 bytes into the holding registers with auto-increment.
3. Set the EECON1 register for the write operation:
   - set WREN to enable byte writes.
4. Disable interrupts.
5. Write 55h to EECON2.
6. Write 0AAh to EECON2.
7. Set the WR bit. This will begin the write cycle.
8. The CPU will stall for duration of the write (about 2 ms using internal timer).
9. Re-enable interrupts.
10. Verify the memory (table read).

An example of the required code is shown in Example 7-3.

| **Note:** | Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the 64 bytes in the holding register. |
|---|---|

## BRA Unconditional Branch

| | |
|---|---|
| Syntax: | BRA n |
| Operands: | -1024 dn d1023 |
| Operation: | (PC) + 2 + 2n o PC |
| Status Affected: | None |
| Encoding: | 1101 \| 0nnn \| nnnn \| nnnn |
| Description: | Add the 2 s complement number, 2n , to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal n | Process Data | Write to PC |
| No operation | No operation | No operation | No operation |

Example: HERE BRA Jump

Before Instruction
PC = address (HERE)
After Instruction
PC = address (Jump)

## BSF Bit Set f

| | |
|---|---|
| Syntax: | BSF f, b {,a} |
| Operands: | 0 df d255<br>0 db d7<br>a [0,1 ] |
| Operation: | 1 o f<b> |
| Status Affected: | None |
| Encoding: | 1000 \| bbba \| ffff \| ffff |
| Description: | Bit b in register f is set.<br>If a is 0 , the Access Bank is selected. If a is 1 , the BSR is used to select the GPR bank (default).<br>If a is 0 and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f d95 (5Fh). See Section 22.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details. |
| Words: | 1 |
| Cycles: | 1 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register f | Process Data | Write register f |

Example: BSF FLAG_REG, 7, 1

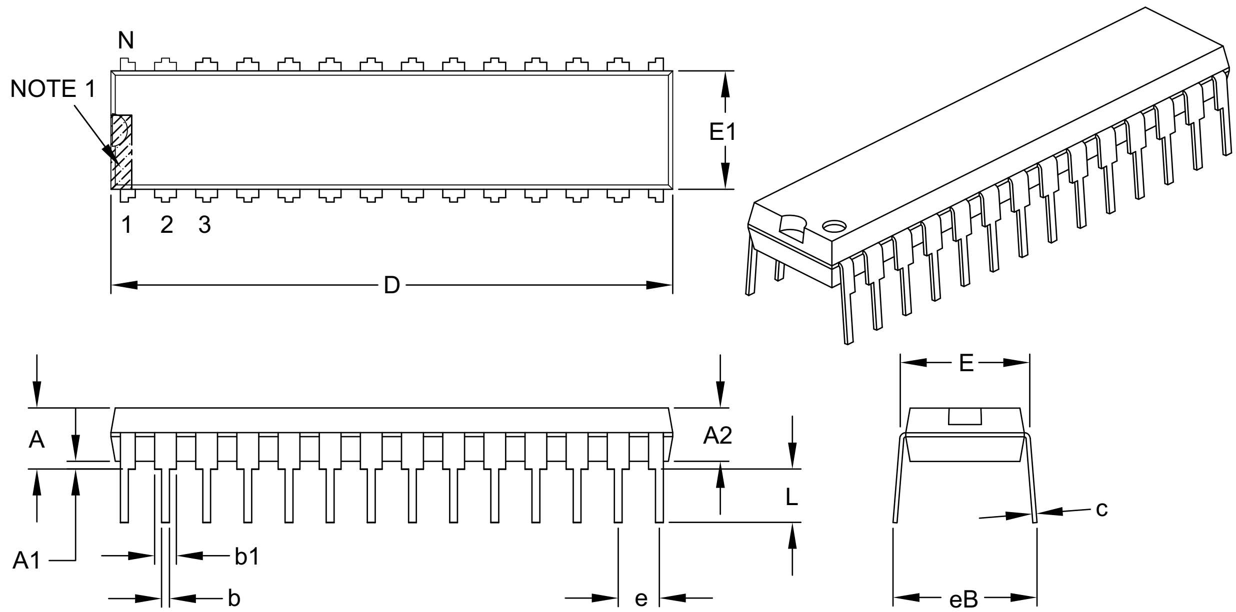
Before Instruction
FLAG_REG = 0Ah
After Instruction
FLAG_REG = 8Ah

## 25.2 Package Details

The following sections give the technical details of the packages.

### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




| | | Units | INCHES | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

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