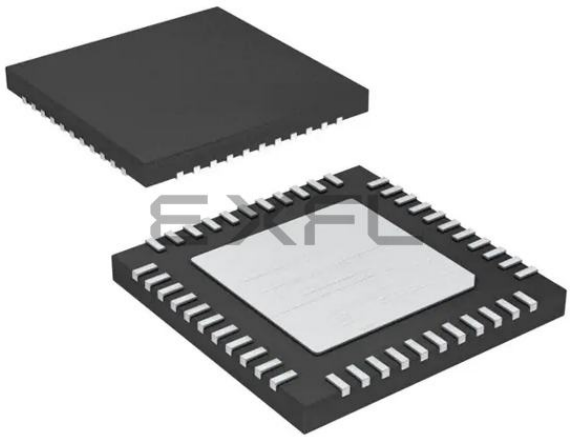

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf44j10-i-ml

1.2 Other Special Features

- Communications: The PIC18F45J10 family incorporates a range of serial communication peripherals, including 1 independent Enhanced USART and 2 Master SSP modules capable of both SPI and I^2C (Master and Slave) modes of operation. Also, one of the general purpose I/O ports can be reconfigured as an 8-bit Parallel Slave Port for direct processor-to-processor communications.
- Self-Programmability: These devices can write to their own program memory spaces under internal software control. By using a bootloader routine, it becomes possible to create an application that can update itself in the field.
- Extended Instruction Set: The PIC18F45J10 family introduces an optional extension to the PIC18 instruction set, which adds 8 new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- Enhanced CCP module: In PWM mode, this module provides 1, 2 or 4 modulated outputs for controlling half-bridge and full-bridge drivers. Other features include Auto-Shutdown, for disabling PWM outputs on interrupt or other select conditions and Auto-Restart, to reactivate outputs once the condition has cleared.
- Enhanced Addressable USART: This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution.
- 10-bit A/D Converter: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.
- Extended Watchdog Timer (WDT): This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See Section 24.0 “Electrical Characteristics” for time-out periods.

1.3 Details on Individual Family Members

Devices in the PIC18F45J10 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in five ways:

1. Flash program memory (16 Kbytes for PIC18F24J10/44J10 devices and 32 Kbytes for PIC18F25J10/45J10).
2. A/D channels (10 for 28-pin devices, 13 for 40/44-pin devices).
3. I/O ports (3 bidirectional ports on 28-pin devices, 5 bidirectional ports on 40/44-pin devices).
4. CCP and Enhanced CCP implementation (28-pin devices have 2 standard CCP modules, 40/44-pin devices have one standard CCP module and one ECCP module).
5. Parallel Slave Port (present only on 40/44-pin devices).
6. One MSSP module for PIC18F24J10/25J10 devices and 2 MSSP modules for PIC18F44J10/45J10 devices
7. Parts designated with an “F” part number (i.e., PIC18F25J10) have a minimum V_{DD} of 2.7 volts, whereas parts designated with an “LF” part number (i.e., PIC18LF25J10) can operate between 2.0-3.6 volts on V_{DD}; however, V_{DDCORE} should never exceed V_{DD}.

All of the other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

The PIC18F45J10 family of devices provides an on-chip voltage regulator to supply the correct voltage levels to the core. Parts designated with an “F” part number (such as PIC18F25J10) have the voltage regulator enabled. These parts can run from 2.7-3.6 volts on V_{DD} but should have the V_{DDCORE} pin connected to V_{SS} through a low-ESR capacitor. Parts designated with an “LF” part number (such as PIC18LF24J10) do not enable the voltage regulator. An external supply of 2.0-2.7 Volts has to be supplied to the V_{DDCORE} pin while 2.0-3.6 Volts can be supplied to V_{DD} (V_{DDCORE} should never exceed V_{DD}). See Section 21.3 “On-Chip Voltage Regulator” for more details about the internal voltage regulator.

REGISTER 7-1: EECON1: EEPROM CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-x	R/W-0	R/S-0	U-0
—	—	—	FREE	WRERR	WREN	WR	—
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	S = Settable bit (cannot be cleared in software)	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: Read as '0'

bit 4 FREE: Flash Row Erase Enable bit
1 = Performs an erase operation on the next WR command (cleared by completion of erase operation)
0 = Perform write only

bit 3 WRERR: Flash Program Error Flag bit
1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation, or an improper write attempt)
0 = The write operation completed

bit 2 WREN: Flash Program Write Enable bit
1 = Allows write cycles to Flash program
0 = Inhibits write cycles to Flash program

bit 1 WR: Write Control bit
1 = Initiates a program memory erase cycle or write cycle.
(The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle is complete

bit 0 Unimplemented: Read as '0'

REGISTER 9-11: IPR2: PERIPHERAL INTERRUPT PRIORITY REGISTER 2

R/W-1	R/W-1	U-0	U-0	R/W-1	U-0	U-0	R/W-0
OSCFIP	CMIP	—	—	BCL1IP	—	—	CCP2IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 OSCFIP: Oscillator Fail Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6 CMIP: Comparator Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5-4 Unimplemented: Read as ‘0’

bit 3 BCL1IP: Bus Collision Interrupt Priority bit (MSSP1 module)
1 = High priority
0 = Low priority

bit 2-1 Unimplemented: Read as ‘0’

bit 0 CCP2IP: CCP2 Interrupt Priority bit
1 = High priority
0 = Low priority

REGISTER 9-12: IPR3: PERIPHERAL INTERRUPT PRIORITY REGISTER 3

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
SSP2IP	BCL2IP	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 SSP2IP: Master Synchronous Serial Port 2 Interrupt Priority bit
1 = High priority
0 = Low priority

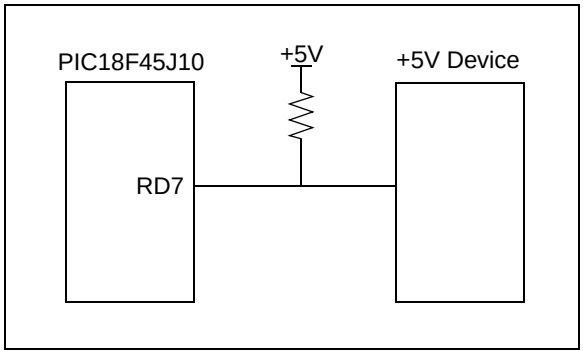
bit 6 BCL2IP: Bus Collision Interrupt Priority bit (MSSP2 module)
1 = High priority
0 = Low priority

bit 5-0 Unimplemented: Read as ‘0’

10.1.3 INTERFACING TO A 5V SYSTEM

Though the V_{DDMAX} of the PIC18F45J10 family is 3.6V, these devices are still capable of interfacing with 5V systems, even if the V_{IH} of the target system is above 3.6V. This is accomplished by adding a pull-up resistor to the port pin (Figure 10-2), clearing the LAT bit for that pin and manipulating the corresponding TRIS bit (Figure 10-1) to either allow the line to be pulled high or to drive the pin low. Only port pins that are tolerant of voltages up to 5.5V can be used for this type of interface (refer to Section 10.1.2 “Input Pins and Voltage Considerations”).

FIGURE 10-2: +5V SYSTEM HARDWARE INTERFACE



EXAMPLE 10-1: COMMUNICATING WITH THE +5V SYSTEM

```
BCF    LATD, 7    ; set up LAT register so
                  ; changing TRIS bit will
                  ; drive line low
BCF    TRISD, 7   ; send a 0 to the 5V system
BCF    TRISD, 7   ; send a 1 to the 5V system
```

10.2 PORTA, TRISA and LATA Registers

PORTA is a 5-bit wide, bidirectional port. The corresponding Data Direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch (LATA) register is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The other PORTA pins are multiplexed with analog inputs, the analog V_{REF+} and V_{REF-} inputs and the comparator voltage reference output. The operation of pins RA<3:0> and RA5 as A/D converter inputs is selected by clearing or setting the control bits in the ADCON1 register (A/D Control Register 1).

Pins RA0 and RA3 may also be used as comparator inputs and RA5 may be used as the C2 comparator output by setting the appropriate bits in the CMCON register. To use RA<3:0> as digital inputs, it is also necessary to turn off the comparators.

Note:	On a Power-on Reset, RA5 and RA<3:0> are configured as analog inputs and read as ‘0’.

All PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-2: INITIALI ZING PORTA

```
CLRF    PORTA     ; Initialize PORTA by
                  ; clearing output
                  ; data latches
CLRF    LATA      ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW   07h       ; Configure A/D
MOVWF   ADCON1    ; for digital inputs
MOVWF   07h       ; Configure comparators
MOVWF   CMCON     ; for digital input
MOVLW   0CFh      ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISA     ; Set RA<3:0> as inputs
                  ; RA<5:4> as outputs
```

TABLE 10-3: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0	RA0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	I	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	I	ANA	A/D Input Channel 0 and Comparator C1- input. Default input configuration on POR; does not affect digital output.
RA1/AN1	RA1	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	I	TTL	PORTA<1> data input; disabled when analog input enabled.
	AN1	1	I	ANA	A/D Input Channel 1 and Comparator C2- input. Default input configuration on POR; does not affect digital output.
RA2/AN2/ VREF-/CVREF	RA2	0	O	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	I	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.
	AN2	1	I	ANA	A/D Input Channel 2 and Comparator C2+ input. Default input configuration on POR; not affected by analog output.
	VREF-	1	I	ANA	A/D and comparator voltage reference low input.
	CVREF	x	O	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/VREF+	RA3	0	O	DIG	LATA<3> data output; not affected by analog input.
		1	I	TTL	PORTA<3> data input; disabled when analog input enabled.
	AN3	1	I	ANA	A/D Input Channel 3 and Comparator C1+ input. Default input configuration on POR.
	VREF+	1	I	ANA	A/D and comparator voltage reference high input.
RA5/AN4/$\overline{SS1}$/ C2OUT	RA5	0	O	DIG	LATA<5> data output; not affected by analog input.
		1	I	TTL	PORTA<5> data input; disabled when analog input enabled.
	AN4	1	I	ANA	A/D Input Channel 4. Default configuration on POR.
	$\overline{SS1}$	1	I	TTL	Slave select input for MSSP1 (MSSP1 module).
	C2OUT	0	O	DIG	Comparator 2 output; takes priority over port data.
OSC2/CLKO	OSC2	x	O	ANA	Main oscillator feedback output connection (HS mode).
	CLKO	x	O	DIG	System cycle clock output (FOSC/4) in RC and EC Oscillator modes.
OSC1/CLKI	OSC1	x	I	ANA	Main oscillator input connection.
	CLKI	x	I	ANA	Main clock input connection.

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

14.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCPxCON) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte). All registers are both readable and writable.

14.1.1 CCP MODULES AND TIMER RESOURCES

The CCP modules utilize Timers 1 or 2, depending on the mode selected. Timer1 is available to modules in Capture or Compare modes, while Timer2 is available for modules in PWM mode.

TABLE 14-1: ECCP/CCP MODE – TIMER RESOURCE

ECCP/CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

Both modules may be active at any given time and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM) at the same time. The interactions between the two modules are summarized in Figure 14-1 and Figure 14-2. In Timer1 in Asynchronous Counter mode, the capture operation will not work.

14.1.2 CCP2 PIN ASSIGNMENT

The pin assignment for CCP2 (Capture input, Compare and PWM output) can change, based on device configuration. The CCP2MX Configuration bit determines which pin CCP2 is multiplexed to. By default, it is assigned to RC1 (CCP2MX = 1). If the Configuration bit is cleared, CCP2 is multiplexed with RB3.

Changing the pin assignment of CCP2 does not automatically change any requirements for configuring the port pin. Users must always verify that the appropriate TRIS register is configured correctly for CCP2 operation regardless of where it is located.

TABLE 14-2: INTERACTIONS BETWEEN ECCP1/ CCP1 AND CCP2 FOR TIMER RESOURCES

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Each module uses TMR1 as the time base.
Capture	Compare	CCP2 can be configured for the Special Event Trigger to reset TMR1. Automatic A/D conversions on the trigger event can also be done. Operation of ECCP1/CCP1 will be affected.
Compare	Capture	ECCP1/CCP1 can be configured for the Special Event Trigger to reset TMR1. Operation of CCP2 will be affected.
Compare	Compare	Either module can be configured for the Special Event Trigger to reset TMR1. Automatic A/D conversions on the CCP2 trigger event can be done.
Capture	PWM(1)	None
Compare	PWM(1)	None
PWM(1)	Capture	None
PWM(1)	Compare	None
PWM(1)	PWM	Both PWMs will have the same frequency and update rate (TMR2 interrupt).

Note 1: Includes standard and Enhanced PWM operation.

14.3 Compare Mode

In Compare mode, the 16-bit CCPRx register value is constantly compared against the TMR1 register value. When a match occurs, the CCPx pin can be:

- driven high
- driven low
- toggled (high-to-low or low-to-high)
- remain unchanged (that is, reflects the state of the I/O latch)

The action on the pin is based on the value of the mode select bits (CCPxM<3:0>). At the same time, the interrupt flag bit, CCPxIF, is set.

14.3.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRIS bit.

Note:	Clearing the CCP2CON register will force the RB3 or RC1 compare output latch (depending on device configuration) to the default low level. This is not the PORTB or PORTC I/O data latch.

14.3.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

14.3.3 SOFTWARE INTERRUPT MODE

When the Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the corresponding CCPx pin is not affected. Only a CCP interrupt is generated, if enabled and the CCPxIE bit is set.

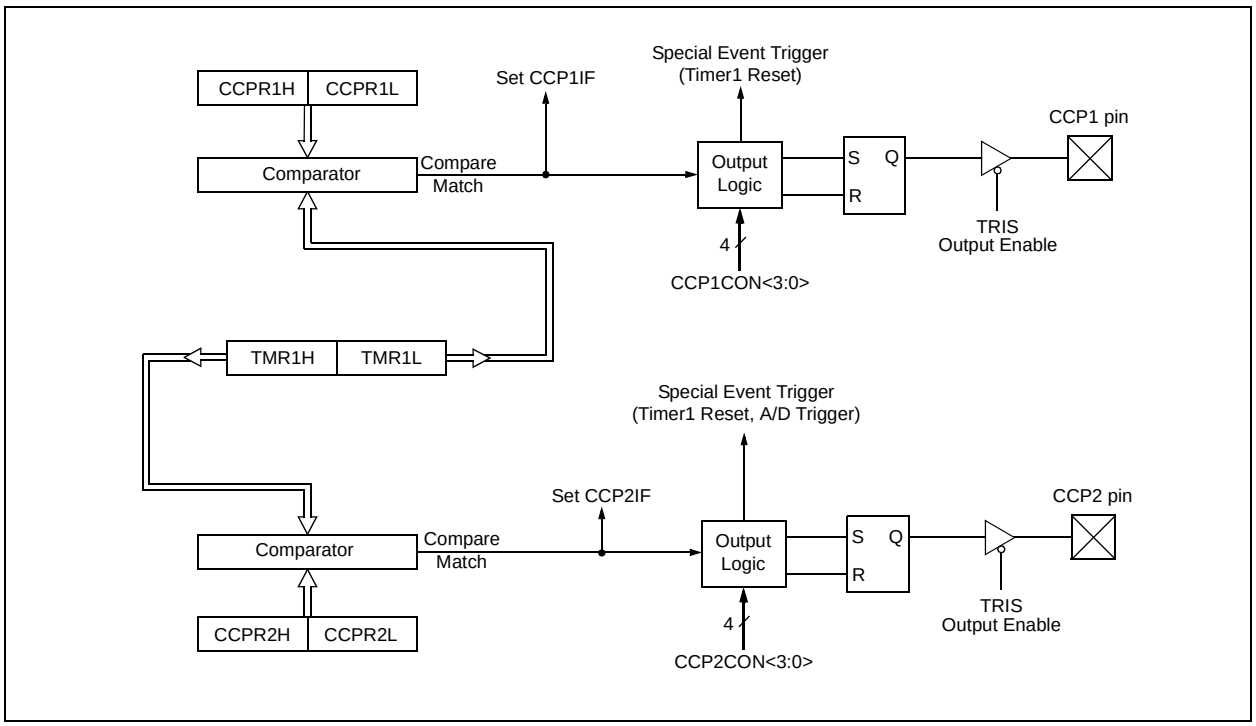
14.3.4 SPECIAL EVENT TRIGGER

Both CCP modules are equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCPxM<3:0> = 1011).

For either CCP module, the Special Event Trigger resets the Timer register pair for whichever timer resource is currently assigned as the module's time base. This allows the CCPRx registers to serve as a Programmable Period register for either timer.

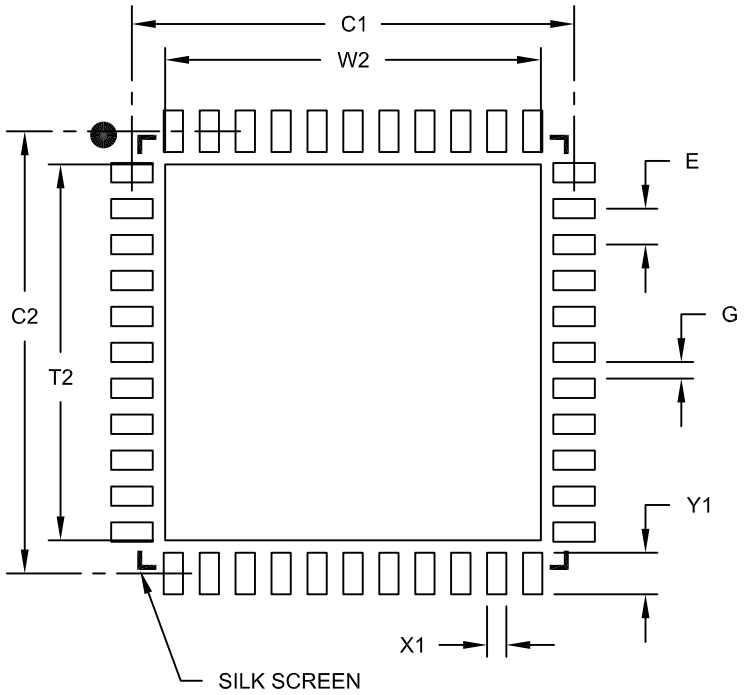
The Special Event Trigger for CCP2 can also start an A/D conversion. In order to do this, the A/D converter must already be enabled.

FIGURE 14-2: COMPARE MODE OPERAT ION BLOCK DIAGRAM



44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

PIC18F45J10 FAMILY PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC18F24J10/25J10, PIC18F44J10/45J10, PIC18F24J10/25J10T(1), PIC18F44J10/45J10T(1); V_{DD} range 2.7V to 3.6V PIC18LF24J10/25J10, PIC18LF44J10/45J10, PIC18LF24J10/25J10T(1), PIC18LF44J10/45J10T(1); V_{DDCORE} range 2.0V to 2.7V
Temperature Range	I = -40°C to +85°C (Industrial)
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny Plastic DIP P = PDIP ML = QFN SS = SSOP
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18LF45J10-I/P 301 = Industrial temp., PDIP package, QTP pattern #301.

b) PIC18LF24J10-I/SO = Industrial temp., SOIC package.

c) PIC18LF44J10-I/P = Industrial temp., PDIP package.

Note 1: T = in tape and reel TQFP packages only.