

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf44j10-i-p

PIC18F45J10 FAMILY

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 3.0 “Oscillator Configurations”** for details).

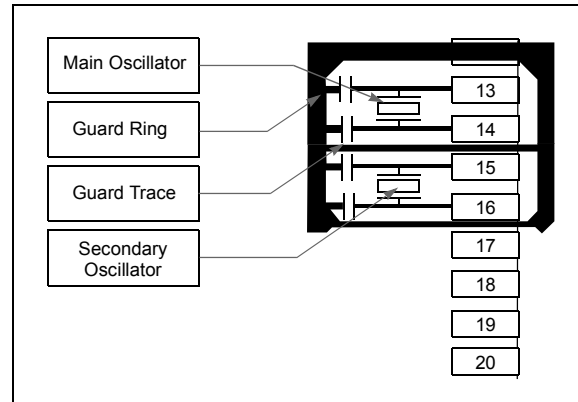
The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-4.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices”
- AN849, “Basic PICmicro® Oscillator Design”
- AN943, “Practical PICmicro® Oscillator Analysis and Design”
- AN949, “Making Your Oscillator Work”

FIGURE 2-4: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

PIC18F45J10 FAMILY

REGISTER 3-2: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	R-q ⁽¹⁾	U-0	R/W-0	R/W-0
IDLEN	—	—	—	OSTS	—	SCS1	SCS0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 7 **IDLEN:** Idle Enable bit
1 = Device enters an Idle mode on *SLEEP* instruction
0 = Device enters Sleep mode on *SLEEP* instruction
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3 **OSTS:** Oscillator Start-up Time-out Status bit⁽¹⁾
1 = Oscillator Start-up Timer (OST) time-out has expired; primary oscillator is running
0 = Oscillator Start-up Timer (OST) time-out is running; primary oscillator is not ready
- bit 2 **Unimplemented:** Read as '0'
- bit 1-0 **SCS<1:0>:** System Clock Select bits⁽⁴⁾
11 = Internal oscillator
10 = Primary oscillator
01 = Timer1 oscillator
When FOSC2 = 1:
00 = Primary oscillator
When FOSC2 = 0:
00 = Internal oscillator

Note 1: The Reset value is '0' when HS mode and Two-Speed Start-up are both enabled; otherwise, it is '1'.

3.7 Effects of Power-Managed Modes on the Various Clock Sources

When *PRI_IDLE* mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the *OSC1* pin is disabled. The *OSC1* pin (and *OSC2* pin if used by the oscillator) will stop oscillating.

In secondary clock modes (*SEC_RUN* and *SEC_IDLE*), the Timer1 oscillator is operating and providing the device clock. The Timer1 oscillator may also run in all power-managed modes if required to clock Timer1 or Timer3.

In *RC_RUN* and *RC_IDLE* modes, the internal oscillator provides the device clock source. The 31 kHz *INTRC* output can be used directly to provide the clock and may be enabled to support various special features, regardless of the power-managed mode (see **Section 21.2 “Watchdog Timer (WDT)”** through **Section 21.5 “Fail-Safe Clock Monitor”** for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up).

If the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The *INTRC* is required to support WDT operation. The Timer1 oscillator may be operating to support a real-time clock. Other features may be operating that do not require a device clock source (i.e., *MSSP* slave, *PSP*, *INTx* pins and others). Peripherals that may add significant current consumption are listed in **Section 24.2 “DC Characteristics: Power-Down and Supply Current”**.

PIC18F45J10 FAMILY

6.5.3 MAPPING THE ACCESS BANK IN INDEXED LITERAL OFFSET MODE

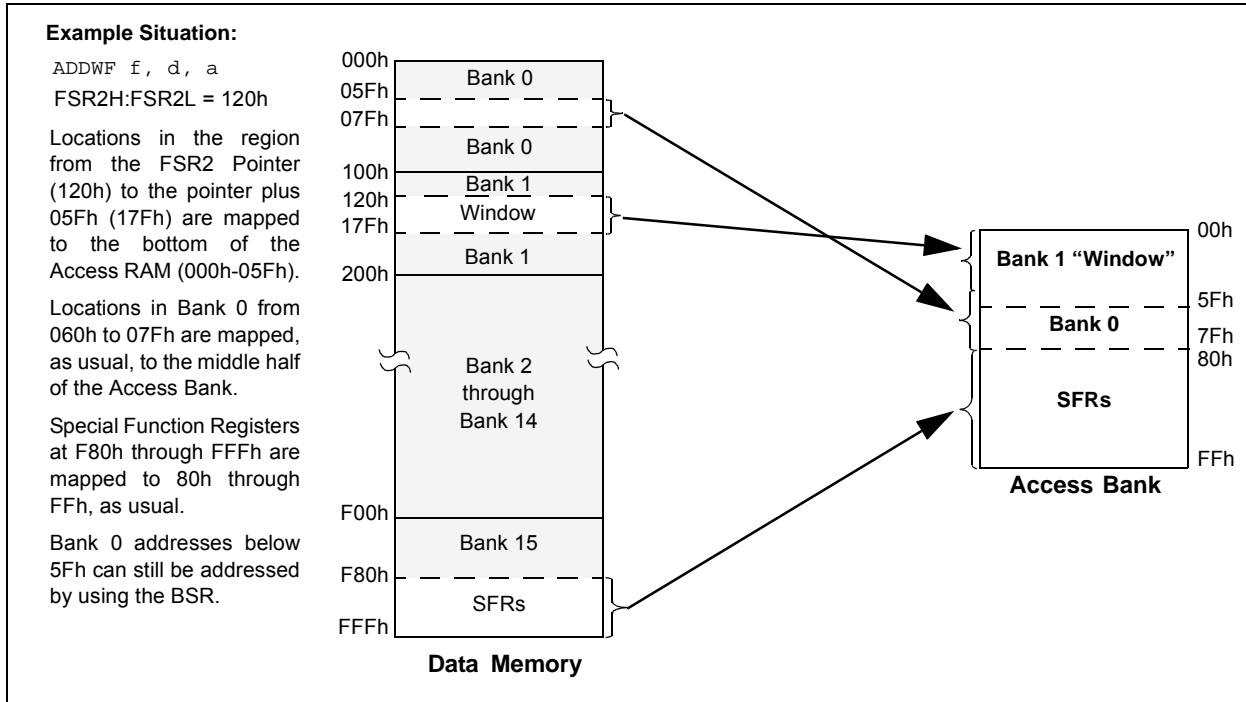
The use of Indexed Literal Offset Addressing mode effectively changes how the first 96 locations of Access RAM (00h to 5Fh) are mapped. Rather than containing just the contents of the bottom half of Bank 0, this mode maps the contents from Bank 0 and a user-defined “window” that can be located anywhere in the data memory space. The value of FSR2 establishes the lower boundary of the addresses mapped into the window, while the upper boundary is defined by FSR2 plus 95 (5Fh). Addresses in the Access RAM above 5Fh are mapped as previously described (see **Section 6.3.2 “Access Bank”**). An example of Access Bank remapping in this addressing mode is shown in Figure 6-10.

Remapping of the Access Bank applies *only* to operations using the Indexed Literal Offset mode. Operations that use the BSR (Access RAM bit is ‘1’) will continue to use Direct Addressing as before.

6.6 PIC18 Instruction Execution and the Extended Instruction Set

Enabling the extended instruction set adds eight additional commands to the existing PIC18 instruction set. These instructions are executed as described in **Section 22.2 “Extended Instruction Set”**.

FIGURE 6-10: REMAPPING THE ACCESS BANK WITH INDEXED LITERAL OFFSET ADDRESSING



14.0 CAPTURE/COMPARE/PWM (CCP) MODULES

PIC18F45J10 family devices all have two CCP (Capture/Compare/PWM) modules. Each module contains a 16-bit register which can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register.

In 28-pin devices, the two standard CCP modules (CCP1 and CCP2) operate as described in this chapter. In 40/44-pin devices, CCP1 is implemented as an Enhanced CCP module (ECCP1) with standard Capture and Compare modes and Enhanced PWM modes. The Enhanced CCP implementation is discussed in **Section 15.0 “Enhanced Capture/Compare/PWM (ECCP) Module”**.

The Capture and Compare operations described in this chapter apply to all standard and Enhanced CCP modules.

Note: Throughout this section and **Section 15.0 “Enhanced Capture/Compare/PWM (ECCP) Module”**, references to the register and bit names for CCP modules are referred to generically by the use of ‘x’ or ‘y’ in place of the specific module number. Thus, “CCPxCON” might refer to the control register for CCP1, CCP2 or ECCP1. “CCPxCON” is used throughout these sections to refer to the module control register regardless of whether the CCP module is a standard or Enhanced implementation.

REGISTER 14-1: CCPxCON: CCP1/CCP2 CONTROL REGISTER IN 28-PIN DEVICES

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared
		x = Bit is unknown

- bit 7-6 **Unimplemented:** Read as ‘0’
- bit 5-4 **DCxB<1:0>:** PWM Duty Cycle bit 1 and bit 0
 - Capture mode:
Unused.
 - Compare mode:
Unused.
 - PWM mode:
These bits are the two LSbs (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight MSbs (DCxB<9:2>) of the duty cycle are found in CCPxL.
- bit 3-0 **CCPxM<3:0>:** CCPx Mode Select bits
 - 0000 = Capture/Compare/PWM disabled (resets CCPx module)
 - 0001 = Reserved
 - 0010 = Compare mode, toggle output on match (CCPxIF bit is set)
 - 0011 = Reserved
 - 0100 = Capture mode, every falling edge
 - 0101 = Capture mode, every rising edge
 - 0110 = Capture mode, every 4th rising edge
 - 0111 = Capture mode, every 16th rising edge
 - 1000 = Compare mode: initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)
 - 1001 = Compare mode: initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)
 - 1010 = Compare mode: generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)
 - 1011 = Compare mode: trigger special event, reset timer, start A/D conversion on CCPx match (CCPxIF bit is set)
 - 11xx = PWM mode

PIC18F45J10 FAMILY

14.3 Compare Mode

In Compare mode, the 16-bit CCPRx register value is constantly compared against the TMR1 register value. When a match occurs, the CCPx pin can be:

- driven high
- driven low
- toggled (high-to-low or low-to-high)
- remain unchanged (that is, reflects the state of the I/O latch)

The action on the pin is based on the value of the mode select bits (CCPxM<3:0>). At the same time, the interrupt flag bit, CCPxIF, is set.

14.3.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRIS bit.

Note: Clearing the CCP2CON register will force the RB3 or RC1 compare output latch (depending on device configuration) to the default low level. This is not the PORTB or PORTC I/O data latch.

14.3.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

14.3.3 SOFTWARE INTERRUPT MODE

When the Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the corresponding CCPx pin is not affected. Only a CCP interrupt is generated, if enabled and the CCPxIE bit is set.

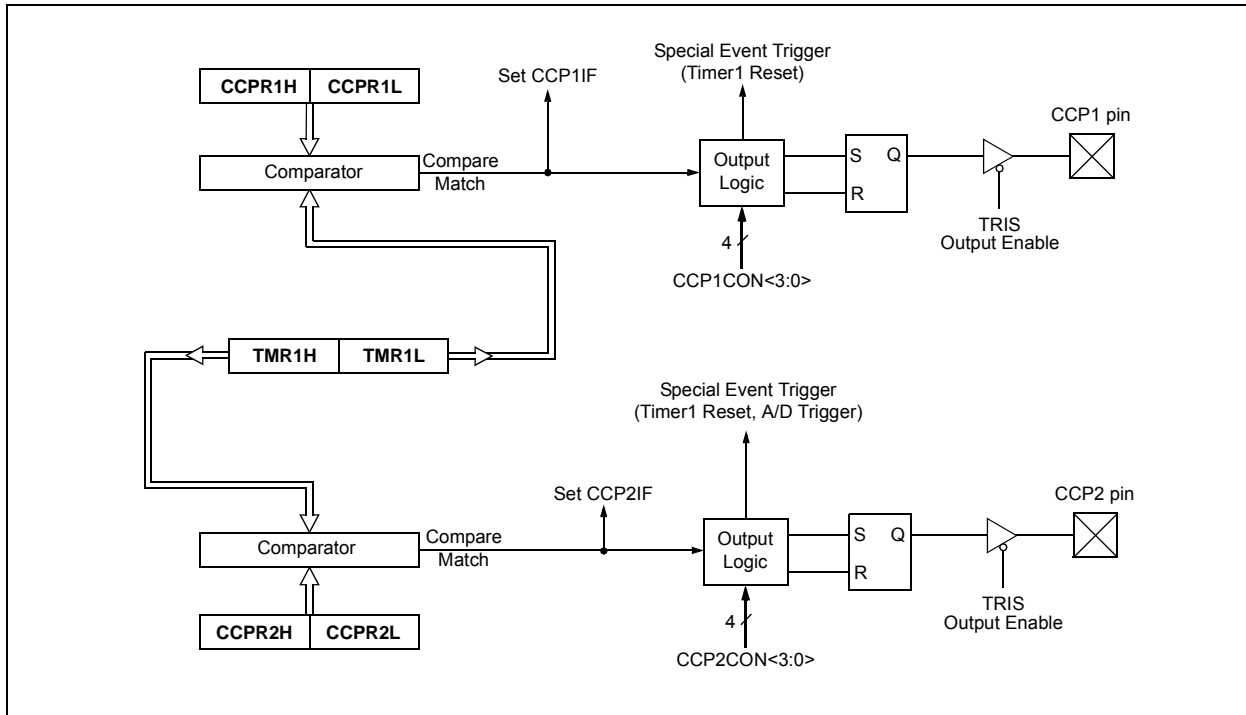
14.3.4 SPECIAL EVENT TRIGGER

Both CCP modules are equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCPxM<3:0> = 1011).

For either CCP module, the Special Event Trigger resets the Timer register pair for whichever timer resource is currently assigned as the module's time base. This allows the CCPRx registers to serve as a Programmable Period register for either timer.

The Special Event Trigger for CCP2 can also start an A/D conversion. In order to do this, the A/D converter must already be enabled.

FIGURE 14-2: COMPARE MODE OPERATION BLOCK DIAGRAM



PIC18F45J10 FAMILY

In addition to the expanded range of modes available through the CCP1CON register and ECCP1AS register, the ECCP module has an additional register associated with Enhanced PWM operation and auto-shutdown features. It is:

- ECCP1DEL (PWM Dead-Band Delay)

15.1 ECCP Outputs and Configuration

The Enhanced CCP module may have up to four PWM outputs, depending on the selected operating mode. These outputs, designated P1A through P1D, are multiplexed with I/O pins on PORTC and PORTD. The outputs that are active depend on the ECCP operating mode selected. The pin assignments are summarized in Table 15-1.

To configure the I/O pins as PWM outputs, the proper PWM mode must be selected by setting the P1M<1:0> and CCP1M<3:0> bits. The appropriate TRISC and TRISD direction bits for the port pins must also be set as outputs.

15.1.1 ECCP MODULES AND TIMER RESOURCES

Like the standard CCP modules, the ECCP module can utilize Timers 1 or 2, depending on the mode selected. Timer1 is available for modules in Capture or Compare modes, while Timer2 is available for modules in PWM mode. Interactions between the standard and Enhanced CCP modules are identical to those described for standard CCP modules. Additional details on timer resources are provided in **Section 14.1.1 “CCP Modules and Timer Resources”**.

15.2 Capture and Compare Modes

Except for the operation of the Special Event Trigger discussed below, the Capture and Compare modes of the ECCP module are identical in operation to that of CCP2. These are discussed in detail in **Section 14.2 “Capture Mode”** and **Section 14.3 “Compare Mode”**. No changes are required when moving between 28-pin and 40/44-pin devices.

15.2.1 SPECIAL EVENT TRIGGER

The Special Event Trigger output of ECCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

15.3 Standard PWM Mode

When configured in Single Output mode, the ECCP module functions identically to the standard CCP module in PWM mode, as described in **Section 14.4 “PWM Mode”**. This is also sometimes referred to as “Compatible CCP” mode, as in Table 15-1.

Note: When setting up single output PWM operations, users are free to use either of the processes described in **Section 14.4.4 “Setup for PWM Operation”** or **Section 15.4.9 “Setup for PWM Operation”**. The latter is more generic and will work for either single or multi-output PWM.

TABLE 15-1: PIN ASSIGNMENTS FOR VARIOUS ECCP1 MODES

ECCP Mode	CCP1CON Configuration	RC2	RD5	RD6	RD7
All 40/44-pin Devices:					
Compatible CCP	00xx 11xx	CCP1	RD5/PSP5	RD6/PSP6	RD7/PSP7
Dual PWM	10xx 11xx	P1A	P1B	RD6/PSP6	RD7/PSP7
Quad PWM	x1xx 11xx	P1A	P1B	P1C	P1D

Legend: x = Don't care. Shaded cells indicate pin assignments not used by ECCP1 in a given mode.

PIC18F45J10 FAMILY

16.4.2 OPERATION

The MSSP module functions are enabled by setting the MSSP Enable bit, SSPEN (SSPxCON1<5>).

The SSPxCON1 register allows control of the I²C operation. Four mode selection bits (SSPxCON1<3:0>) allow one of the following I²C modes to be selected:

- I²C Master mode,
clock = (Fosc/4) x (SSPxADD + 1)
- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address) with Start and Stop bit interrupts enabled
- I²C Slave mode (10-bit address) with Start and Stop bit interrupts enabled
- I²C Firmware Controlled Master mode,
slave is Idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCLx and SDAx pins to be open-drain, provided these pins are programmed to inputs by setting the appropriate TRISC or TRISD bits. To ensure proper operation of the module, pull-up resistors must be provided externally to the SCLx and SDAx pins.

16.4.3 SLAVE MODE

In Slave mode, the SCLx and SDAx pins must be configured as inputs (TRISC<4:3> set). The MSSP module will override the input state with the output data when required (slave-transmitter).

The I²C Slave mode hardware will always generate an interrupt on an exact address match. In addition, address masking will also allow the hardware to generate an interrupt for more than one address (up to 31 in 7-bit addressing and up to 63 in 10-bit addressing). Through the mode select bits, the user can also choose to interrupt on Start and Stop bits.

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge ($\overline{\text{ACK}}$) pulse and load the SSPxBUF register with the received value currently in the SSPxSR register.

Any combination of the following conditions will cause the MSSP module not to give this $\overline{\text{ACK}}$ pulse:

- The Buffer Full bit, BF (SSPxSTAT<0>), was set before the transfer was received.
- The MSSP Overflow bit, SSPOV (SSPxCON1<6>), was set before the transfer was received.

In this case, the SSPxSR register value is not loaded into the SSPxBUF, but the SSPxIF bit is set. The BF bit is cleared by reading the SSPxBUF register, while the SSPOV bit is cleared through software.

The SCLx clock input must have a minimum high and low for proper operation. The high and low times of the I²C specification, as well as the requirement of the MSSP module, are shown in timing parameter 100 and parameter 101.

16.4.3.1 Addressing

Once the MSSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the 8 bits are shifted into the SSPxSR register. All incoming bits are sampled with the rising edge of the clock (SCLx) line. The value of register SSPxSR<7:1> is compared to the value of the SSPxADD register. The address is compared on the falling edge of the eighth clock (SCLx) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

1. The SSPxSR register value is loaded into the SSPxBUF register.
2. The Buffer Full bit, BF, is set.
3. An $\overline{\text{ACK}}$ pulse is generated.
4. The MSSP Interrupt Flag bit, SSPxIF, is set (and interrupt is generated, if enabled) on the falling edge of the ninth SCLx pulse.

In 10-Bit Addressing mode, two address bytes need to be received by the slave. The five Most Significant bits (MSBs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPxSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '11110 A₉ A₈ 0', where 'A₉' and 'A₈' are the two MSBs of the address. The sequence of events for 10-Bit Addressing mode is as follows, with steps 7 through 9 for the slave-transmitter:

1. Receive first (high) byte of address (bits, SSPxIF, BF and UA (SSPxSTAT<1>), are set).
2. Update the SSPxADD register with second (low) byte of address (clears bit, UA, and releases the SCLx line).
3. Read the SSPxBUF register (clears bit, BF) and clear flag bit, SSPxIF.
4. Receive second (low) byte of address (bits, SSPxIF, BF and UA, are set).
5. Update the SSPxADD register with the first (high) byte of address. If match releases SCLx line, this will clear bit, UA.
6. Read the SSPxBUF register (clears bit, BF) and clear flag bit, SSPxIF.
7. Receive Repeated Start condition.
8. Receive first (high) byte of address (bits, SSPxIF and BF, are set).
9. Read the SSPxBUF register (clears bit, BF) and clear flag bit, SSPxIF.

PIC18F45J10 FAMILY

TABLE 17-3: BAUD RATES FOR ASYNCHRONOUS MODES

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	—	—	—
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	—	—	—
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 0								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12
2.4	2.404	0.16	25	2.403	-0.16	12	—	—	—
9.6	8.929	-6.99	6	—	—	—	—	—	—
19.2	20.833	8.51	2	—	—	—	—	—	—
57.6	62.500	8.51	0	—	—	—	—	—	—
115.2	62.500	-45.75	0	—	—	—	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	—	—	—	—	—	—	—	—	—
2.4	—	—	—	—	—	—	2.441	1.73	255	2.403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	0.300	-0.16	207
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25
9.6	9.615	0.16	25	9.615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

PIC18F45J10 FAMILY

FIGURE 17-4: ASYNCHRONOUS TRANSMISSION

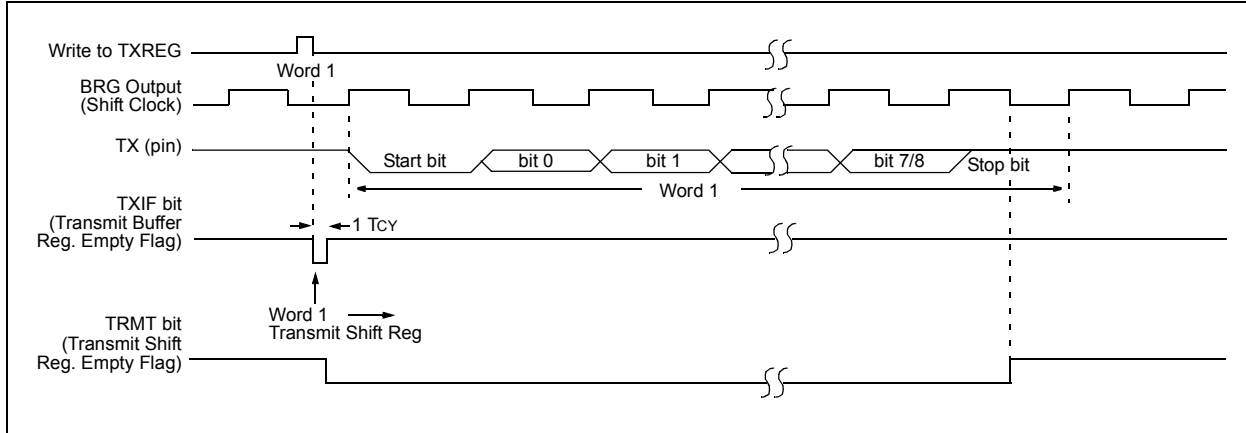


FIGURE 17-5: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)

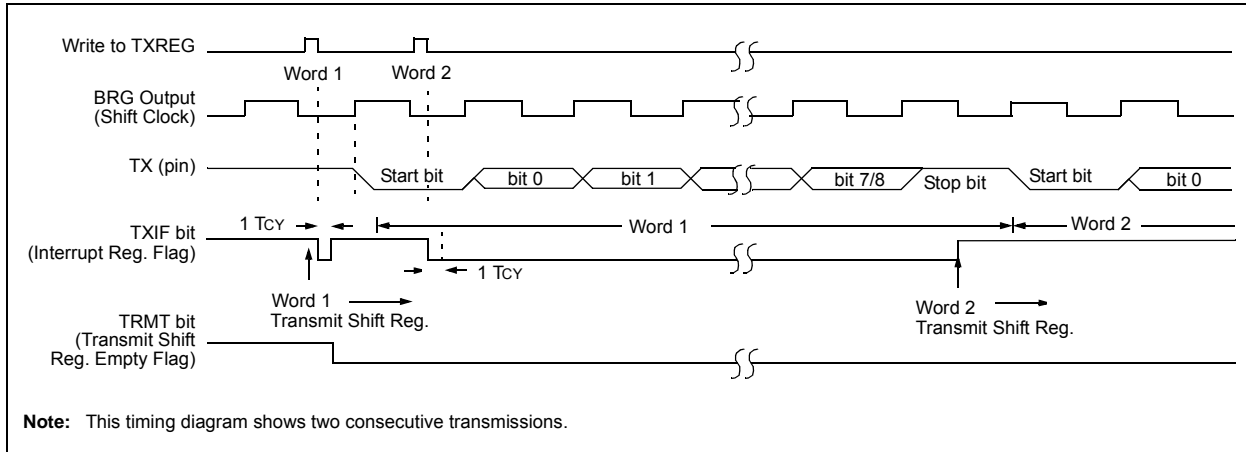


TABLE 17-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	47
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	49
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	49
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	49
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	49
TXREG	EUSART Transmit Register								49
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	49
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	49
SPBRGH	EUSART Baud Rate Generator Register High Byte								49
SPBRG	EUSART Baud Rate Generator Register Low Byte								49

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: These bits are not implemented on 28-pin devices and should be read as '0'.

18.2 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000') and is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQT bits can be set to select a programmable acquisition time for the A/D module. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

18.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD (see parameter 130 in Table 24-25 for more information).

Table 18-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 18-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS<2:0>	
2 TOSC	000	2.86 MHz
4 TOSC	100	5.71 MHz
8 TOSC	001	11.43 MHz
16 TOSC	101	22.86 MHz
32 TOSC	010	40.0 MHz
64 TOSC	110	40.0 MHz
RC ⁽²⁾	x11	1.00 MHz ⁽¹⁾

- Note 1:** The RC source has a typical TAD time of 4 μ s.
- 2:** For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

18.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

- Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.
- 2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

PIC18F45J10 FAMILY

REGISTER 21-1: CONFIG1L: CONFIGURATION REGISTER 1 LOW (BYTE ADDRESS 300000h)

R/WO-1	R/WO-1	R/WO-1	U-0	U-0	U-0	U-0	R/WO-1
<u>DEBUG</u>	XINST	STVREN	—	—	—	—	WDTEN
bit 7							bit 0

Legend:

R = Readable bit WO = Write Once bit U = Unimplemented bit, read as '0'
 -n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

- bit 7 **DEBUG:** Background Debugger Enable bit
 1 = Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins
 0 = Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
- bit 6 **XINST:** Extended Instruction Set Enable bit
 1 = Instruction set extension and Indexed Addressing mode enabled
 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
- bit 5 **STVREN:** Stack Overflow/Underflow Reset Enable bit
 1 = Reset on stack overflow/underflow enabled
 0 = Reset on stack overflow/underflow disabled
- bit 4-1 **Unimplemented:** Read as '0'
- bit 0 **WDTEN:** Watchdog Timer Enable bit
 1 = WDT enabled
 0 = WDT disabled (control is placed on SWDTEN bit)

REGISTER 21-2: CONFIG1H: CONFIGURATION REGISTER 1 HIGH (BYTE ADDRESS 300001h)

U-0	U-0	U-0	U-0	U-0	R/WO-1	U-0	U-0
— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽²⁾	CP0	—	—
bit 7							bit 0

Legend:

R = Readable bit WO = Write Once bit U = Unimplemented bit, read as '0'
 -n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

- bit 7-4 **Unimplemented:** Read as '1'⁽¹⁾
- bit 3 **Unimplemented:** Read as '0'⁽²⁾
- bit 2 **CP0:** Code Protection bit
 1 = Program memory is not code-protected
 0 = Program memory is code-protected
- bit 1-0 **Unimplemented:** Read as '0'

- Note 1:** The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.
- 2:** This bit should always be maintained as '0'.

PIC18F45J10 FAMILY

TBLWT Table Write

Syntax: TBLWT (*, *+, *-, +*)

Operands: None

Operation: if TBLWT *,
(TABLAT) → Holding Register,
TBLPTR – No Change;
if TBLWT *+,
(TABLAT) → Holding Register,
(TBLPTR) + 1 → TBLPTR;
if TBLWT *-,
(TABLAT) → Holding Register,
(TBLPTR) – 1 → TBLPTR;
if TBLWT +*,
(TBLPTR) + 1 → TBLPTR,
(TABLAT) → Holding Register

Status Affected: None

Encoding:

0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*
------	------	------	---

Description: This instruction uses the 3 LSBs of TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to **Section 7.0 “Flash Program Memory”** for additional details on programming Flash memory.) The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-MByte address range. The LSB of the TBLPTR selects which byte of the program memory location to access.

- TBLPTR[0] = 0: Least Significant Byte of Program Memory Word
- TBLPTR[0] = 1: Most Significant Byte of Program Memory Word

The TBLWT instruction can modify the value of TBLPTR as follows:

- no change
- post-increment
- post-decrement
- pre-increment

Words: 1

Cycles: 2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation	No operation
	No operation	No operation (Read TABLAT)	No operation	No operation (Write to Holding Register)

TBLWT Table Write (Continued)

Example 1: TBLWT *+;

Before Instruction

TABLAT	=	55h
TBLPTR	=	00A356h
HOLDING REGISTER (00A356h)	=	FFh

After Instructions (table write completion)

TABLAT	=	55h
TBLPTR	=	00A357h
HOLDING REGISTER (00A356h)	=	55h

Example 2: TBLWT +*;

Before Instruction

TABLAT	=	34h
TBLPTR	=	01389Ah
HOLDING REGISTER (01389Ah)	=	FFh
HOLDING REGISTER (01389Bh)	=	FFh

After Instruction (table write completion)

TABLAT	=	34h
TBLPTR	=	01389Bh
HOLDING REGISTER (01389Ah)	=	FFh
HOLDING REGISTER (01389Bh)	=	34h

PIC18F45J10 FAMILY

22.2.2 EXTENDED INSTRUCTION SET

ADDFSR **Add Literal to FSR**

Syntax: `ADDFSR f, k`
 Operands: $0 \leq k \leq 63$
 $f \in [0, 1, 2]$
 Operation: $FSR(f) + k \rightarrow FSR(f)$
 Status Affected: None
 Encoding:

1110	1000	ffkk	kkkk
------	------	------	------

 Description: The 6-bit literal 'k' is added to the contents of the FSR specified by 'f'.
 Words: 1
 Cycles: 1
 Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to FSR

Example: `ADDFSR 2, 23h`

Before Instruction
 FSR2 = 03FFh
 After Instruction
 FSR2 = 0422h

ADDULNK **Add Literal to FSR2 and Return**

Syntax: `ADDULNK k`
 Operands: $0 \leq k \leq 63$
 Operation: $FSR2 + k \rightarrow FSR2,$
 $(TOS) \rightarrow PC$
 Status Affected: None
 Encoding:

1110	1000	11kk	kkkk
------	------	------	------

 Description: The 6-bit literal 'k' is added to the contents of FSR2. A `RETURN` is then executed by loading the PC with the TOS.

The instruction takes two cycles to execute; a `NOP` is performed during the second cycle. This may be thought of as a special case of the `ADDFSR` instruction, where $f = 3$ (binary '11'); it operates only on FSR2.

Words: 1
 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to FSR
No Operation	No Operation	No Operation	No Operation

Example: `ADDULNK 23h`

Before Instruction
 FSR2 = 03FFh
 PC = 0100h
 After Instruction
 FSR2 = 0422h
 PC = (TOS)

Note: All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction syntax then becomes: {label} instruction argument(s).

PIC18F45J10 FAMILY

ADDWF ADD W to Indexed (Indexed Literal Offset mode)

Syntax: ADDWF [k] {,d}

Operands: $0 \leq k \leq 95$
 $d \in [0, 1]$

Operation: $(W) + ((FSR2) + k) \rightarrow \text{dest}$

Status Affected: N, OV, C, DC, Z

Encoding:

0010	01d0	kkkk	kkkk
------	------	------	------

Description: The contents of W are added to the contents of the register indicated by FSR2, offset by the value 'k'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process Data	Write to destination

Example: ADDWF [OFST], 0

Before Instruction

W	=	17h
OFST	=	2Ch
FSR2	=	0A00h
Contents of 0A2Ch	=	20h

After Instruction

W	=	37h
Contents of 0A2Ch	=	20h

BSF Bit Set Indexed (Indexed Literal Offset mode)

Syntax: BSF [k], b

Operands: $0 \leq f \leq 95$
 $0 \leq b \leq 7$

Operation: $1 \rightarrow ((FSR2) + k) < b >$

Status Affected: None

Encoding:

1000	bbb0	kkkk	kkkk
------	------	------	------

Description: Bit 'b' of the register indicated by FSR2, offset by the value 'k', is set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: BSF [FLAG_OFST], 7

Before Instruction

FLAG_OFST	=	0Ah
FSR2	=	0A00h
Contents of 0A0Ah	=	55h

After Instruction

Contents of 0A0Ah	=	D5h
-------------------	---	-----

SETF Set Indexed (Indexed Literal Offset mode)

Syntax: SETF [k]

Operands: $0 \leq k \leq 95$

Operation: $FFh \rightarrow ((FSR2) + k)$

Status Affected: None

Encoding:

0110	1000	kkkk	kkkk
------	------	------	------

Description: The contents of the register indicated by FSR2, offset by 'k', are set to FFh.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process Data	Write register

Example: SETF [OFST]

Before Instruction

OFST	=	2Ch
FSR2	=	0A00h
Contents of 0A2Ch	=	00h

After Instruction

Contents of 0A2Ch	=	FFh
-------------------	---	-----

PIC18F45J10 FAMILY

24.2 DC Characteristics: Power-Down and Supply Current PIC18F24J10/25J10/44J10/45J10 (Industrial) PIC18LF24J10/25J10/44J10/45J10 (Industrial) (Continued)

PIC18F45J10 Family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device	Typ	Max	Units	Conditions		
Supply Current (I_{DD})⁽²⁾							
	All devices	4.2	8.5	mA	-40°C	V _{DD} = 2.5V F _{OSC} = 1 MHz (PRI_RUN mode, EC oscillator)	
		3.9	8.0	mA	$+25^{\circ}\text{C}$		
		3.6	7.3	mA	$+85^{\circ}\text{C}$		
	All devices	4.3	8.6	mA	-40°C		V _{DD} = 3.3V
		4.0	8.1	mA	$+25^{\circ}\text{C}$		
		3.7	7.6	mA	$+85^{\circ}\text{C}$		
	All devices	4.6	9.3	mA	-40°C	V _{DD} = 2.5V	F _{OSC} = 4 MHz (PRI_RUN mode, EC oscillator)
		4.3	8.7	mA	$+25^{\circ}\text{C}$		
		4.0	8.1	mA	$+85^{\circ}\text{C}$		
All devices	4.7	9.4	mA	-40°C	V _{DD} = 3.3V		
	4.4	8.8	mA	$+25^{\circ}\text{C}$			
	4.1	8.2	mA	$+85^{\circ}\text{C}$			
All devices	11.0	22.0	mA	-40°C	V _{DD} = 2.5V	F _{OSC} = 40 MHz (PRI_RUN mode, EC oscillator)	
	10.5	21.0	mA	$+25^{\circ}\text{C}$			
	10.0	20.0	mA	$+85^{\circ}\text{C}$			
All devices	12.0	24.0	mA	-40°C	V _{DD} = 3.3V		
	11.5	23.0	mA	$+25^{\circ}\text{C}$			
	11.0	22.0	mA	$+85^{\circ}\text{C}$			

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 oscillator, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 $\overline{\text{OSC1}}$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
 $\overline{\text{MCLR}}$ = V_{DD}; WDT enabled/disabled as specified.
- 3:** Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.

PIC18F45J10 FAMILY

FIGURE 24-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

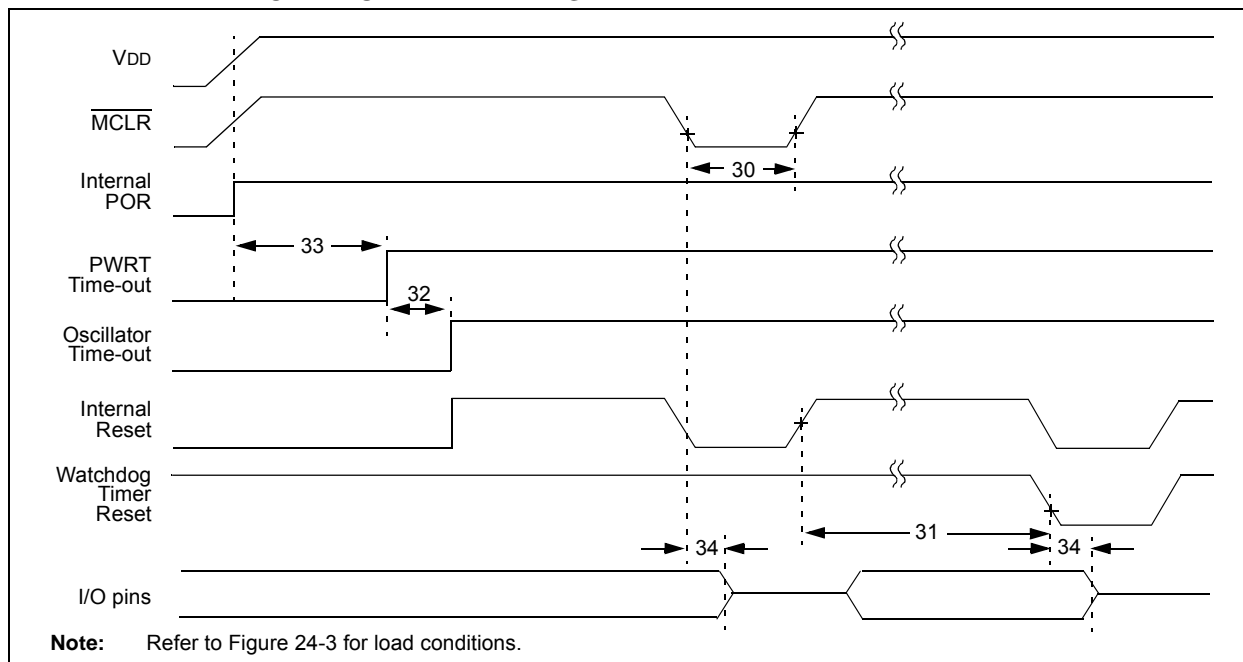


FIGURE 24-7: BROWN-OUT RESET TIMING

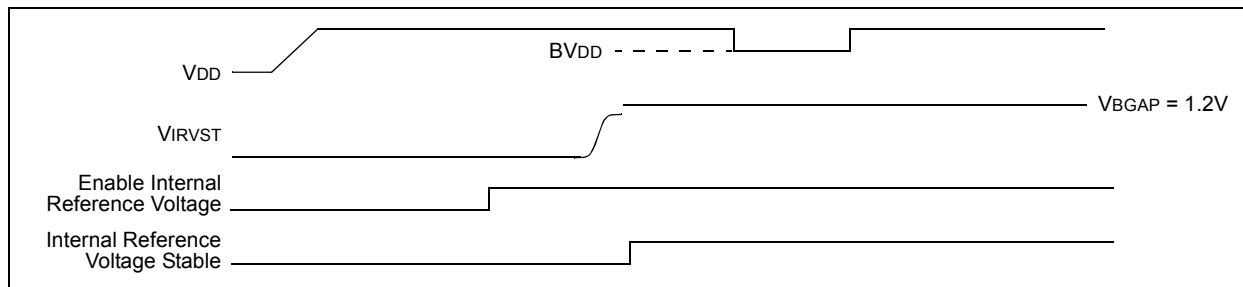


TABLE 24-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	—	μs	
31	TWDT	Watchdog Timer Time-out Period (no postscaler)	2.8	4.1	5.4	ms	
32	TOST	Oscillation Start-up Timer Period	1024 T _{osc}	—	1024 T _{osc}	—	T _{osc} = OSC1 period
33	TPWRT	Power-up Timer Period	46.2	66	85.8	ms	
34	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μs	
38	TcSD	CPU Start-up Time	—	200	—	μs	

PIC18F45J10 FAMILY

FIGURE 24-14: I²C™ BUS START/STOP BITS TIMING

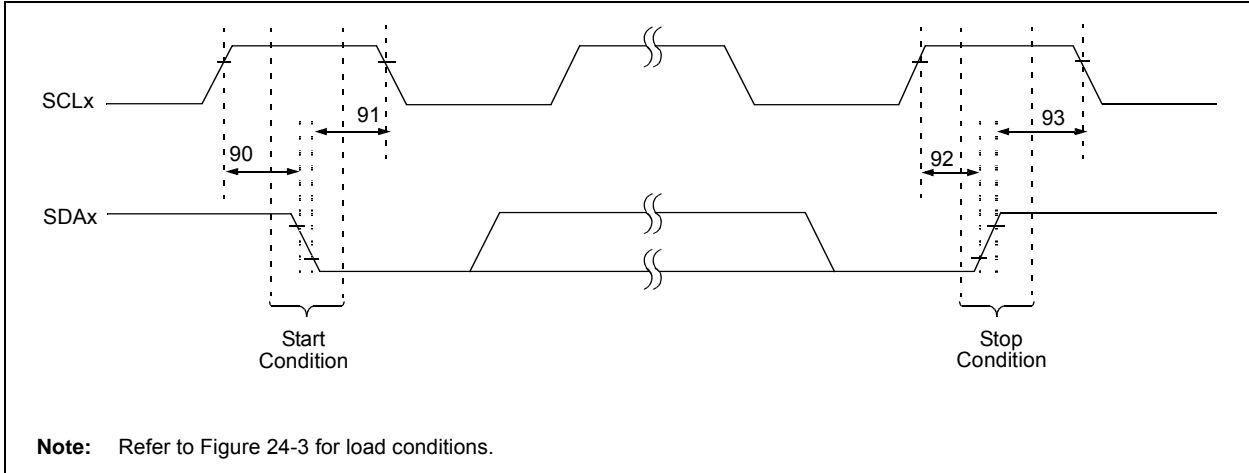
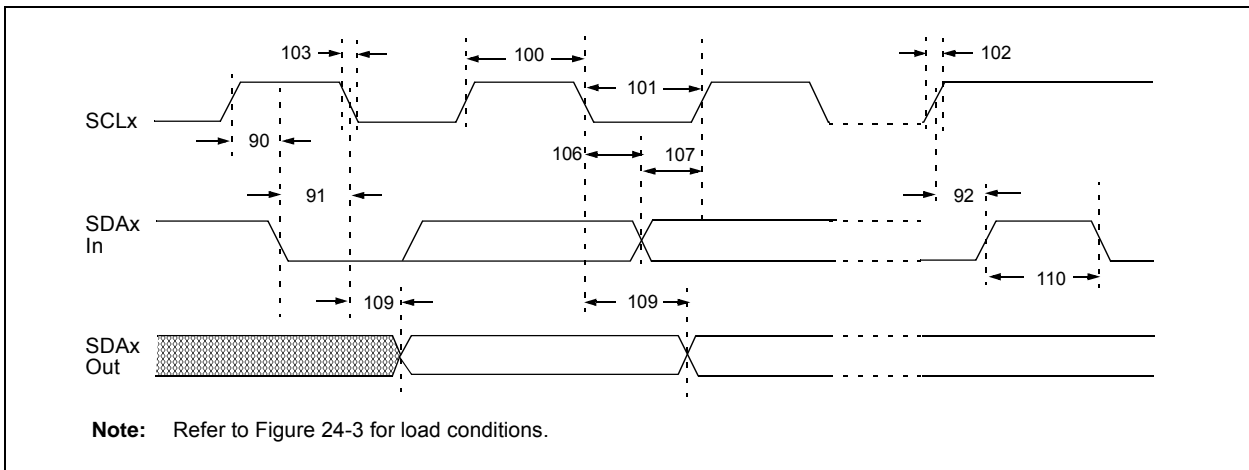


TABLE 24-18: I²C™ BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions	
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4700	—	ns	
			400 kHz mode	600	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—		

FIGURE 24-15: I²C™ BUS DATA TIMING

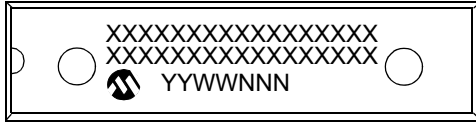


PIC18F45J10 FAMILY

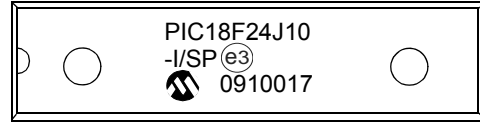
25.0 PACKAGING INFORMATION

25.1 Package Marking Information

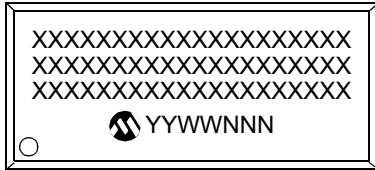
28-Lead SPDIP



Example



28-Lead SOIC



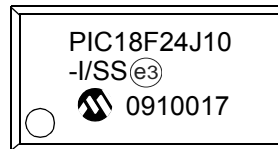
Example



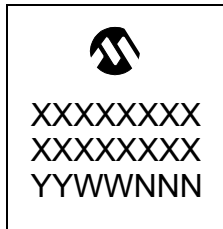
28-Lead SSOP



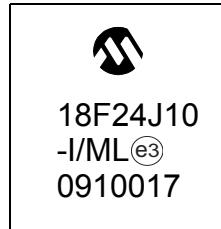
Example



28-Lead QFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

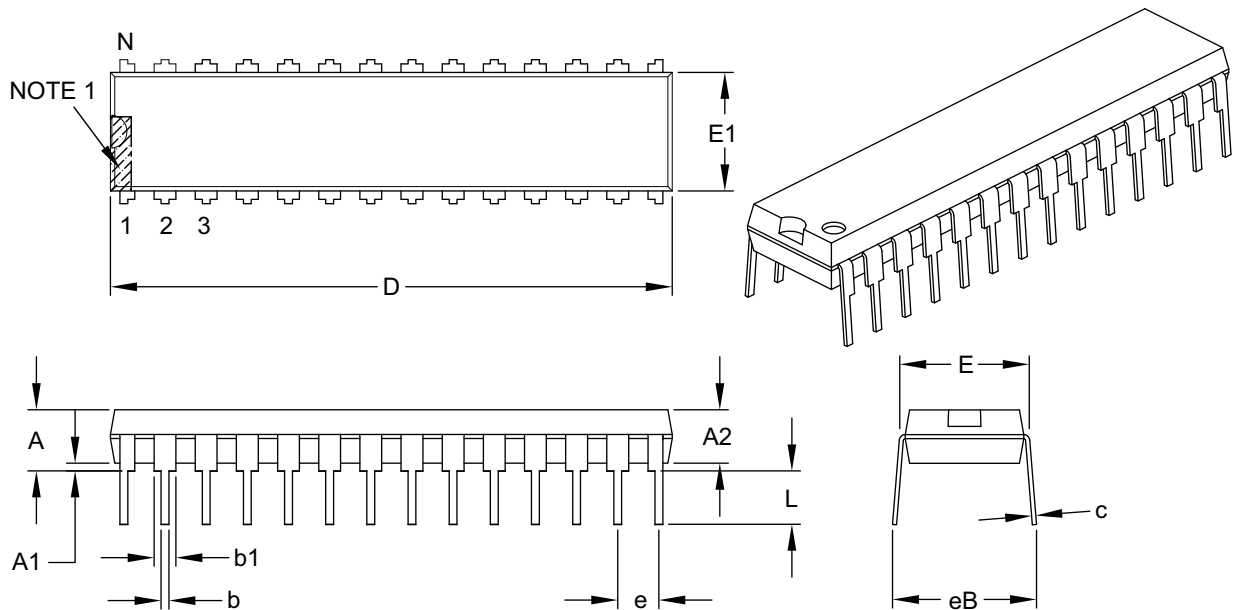
PIC18F45J10 FAMILY

25.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	INCHES		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		.100 BSC		
Top to Seating Plane	A	–	–		.200
Molded Package Thickness	A2	.120	.135		.150
Base to Seating Plane	A1	.015	–		–
Shoulder to Shoulder Width	E	.290	.310		.335
Molded Package Width	E1	.240	.285		.295
Overall Length	D	1.345	1.365		1.400
Tip to Seating Plane	L	.110	.130		.150
Lead Thickness	c	.008	.010		.015
Upper Lead Width	b1	.040	.050		.070
Lower Lead Width	b	.014	.018		.022
Overall Row Spacing §	eB	–	–		.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

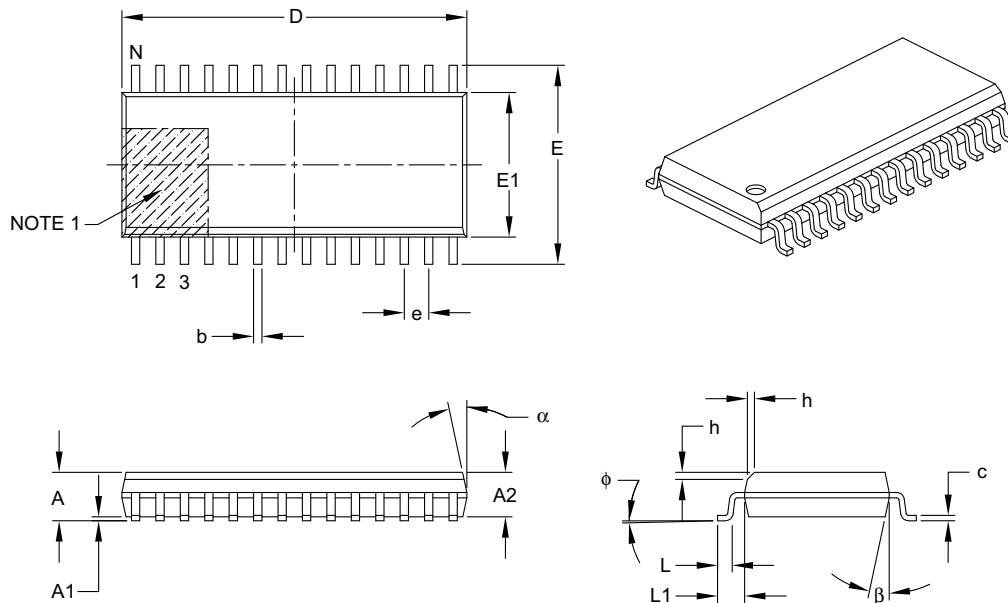
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

PIC18F45J10 FAMILY

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	ϕ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B