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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf45j10t-i-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

	Pin Nu	ımber			
Pin Name	SPDIP, SOIC, SSOP	QFN	Pin Type	Buffer Type	Description
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	11	8	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 ⁽²⁾	12	9	I/O I I/O	ST Analog ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1 RC2 CCP1	13	10	I/O I/O	ST ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output.
RC3/SCK1/SCL1 RC3 SCK1 SCL1	14	11	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI1/SDA1 RC4 SDI1 SDA1	15	12	I/O I I/O	ST ST ST	Digital I/O. SPI data in. I ² C data I/O.
RC5/SDO1 RC5 SDO1	16	13	I/O O	ST —	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	17	14	I/O O I/O	ST — ST	Digital I/O. EUSART asynchronous transmit. EUSART synchronous clock (see related RX/DT).
RC7/RX/DT RC7 RX DT	18	15	I/O I I/O	ST ST ST	Digital I/O. EUSART asynchronous receive. EUSART synchronous data (see related TX/CK).
Vss	8, 19	5, 16	Р		Ground reference for logic and I/O pins.
Vdd	20	17	Р	—	Positive supply for logic and I/O pins.
VDDCORE/VCAP VDDCORE VCAP	6	3	P P		Positive supply for logic and I/O pins. Ground reference for logic and I/O pins.
Legend: TTL = TTL co ST = Schmit O = Output	ompatible tt Trigger	input input v	with CI	MOS lev	CMOS = CMOS compatible input or output rels I = Input P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

O = Output

Din Nome	Pin Number			Pin	Buffer	Description	
Pin Name	PDIP	QFN	TQFP	Туре	Туре	Description	
MCLR MCLR	1	18	18	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.	
OSC1/CLKI OSC1 CLKI	13	32	30	 	смоз	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. External clock source input. Always associated with pin function OSC1. See related OSC2/CLKO pins.	
OSC2/CLKO OSC2 CLKO	14	33	31	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.	
Legend: TTL = TTL co	ompatibl	e input			C	CMOS = CMOS compatible input or output	

TABLE 1-3:PIC18F44J10/45J10 PINOUT I/O DESCRIPTIONS

ST = Schmitt Trigger input with CMOS levels I = Input O = Output P = Power

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F45J10 FAMILY

R/W-0	U-0	R/W-1	R/W-1	R-1	R-1	R/W-0	R/W-0	
IPEN	—	CM	RI	TO	PD	POR	BOR ⁽¹⁾	
bit 7				·	·		bit 0	
								
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	ad as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown	
bit 7	IPEN: Interrup 1 = Enable pr 0 = Disable p	ot Priority Enab riority levels on riority levels or	le bit interrupts interrupts (F	PIC16CXXX Co	ompatibility mo	de)		
bit 6	Unimplement	ted: Read as '	D'					
bit 5	CM: Configura	ation Mismatch	Flag bit					
bit 4	 1 = A Configuration Mismatch Reset has not occurred 0 = A Configuration Mismatch Reset has occurred (must be set in software after a Configuration Mismatch Reset occurs) it 4 RI: RESET Instruction Flag bit 1 = The RESET instruction was not executed (set by firmware only) 0 = The RESET instruction was executed causing a device Reset (must be set in software after 							
bit 3	TO: Watchdog	it Reset occurs g Time-out Flag	;) g bit					
	1 = Set by po 0 = A WDT til	wer-up, CLRWI me-out occurre	o⊤ instruction ed	or SLEEP inst	ruction			
bit 2	PD: Power-Do	own Detection	Flag bit					
	1 = Set by po 0 = Set by ex	wer-up or by the secution of the	ne CLRWDT in SLEEP instrue	struction ction				
bit 1	POR: Power-o	on Reset Statu	s bit					
	1 = A Power- 0 = A Power-	on Reset has r on Reset occu	not occurred (rred (must be	(set by firmwar set in softwar	e only) e after a Powe	r-on Reset occu	rs)	
bit 0	BOR: Brown-	out Reset Statu	us bit ⁽¹⁾					
	1 = A Brown 0 = A Brown	-out Reset has -out Reset occ	not occurred urred (must b	(set by firmwa e set in softwa	are only) are after a Brow	vn-out Reset occ	curs)	
Note 1: BO	R is not availab	le on PIC18LF	2XJ10/4XJ10	devices.				

REGISTER 5-1: RCON: RESET CONTROL REGISTER

Note 1:	It is recommended that the POR bit be set after a Power-on Reset has been detected, so that subsequent Power-on Resets may be detected.
2:	If the on-chip voltage regulator is disabled, BOR remains '0' at all times. See Section 5.4.1 "Detecting BOR" for more information.
3:	Brown-out Reset is said to have occurred when $\overline{\text{BOR}}$ is '0' and $\overline{\text{POR}}$ is '1' (assuming that $\overline{\text{POR}}$ was set to '1' by software immediately after a Power-on Reset).

5.5 Configuration Mismatch (CM)

The Configuration Mismatch (CM) Reset is designed to detect and attempt to recover from random, memory corrupting events. These include Electrostatic Discharge (ESD) events, which can cause widespread, single-bit changes throughout the device and result in catastrophic failure.

In PIC18FXXJ Flash devices, the device Configuration registers (located in the configuration memory space) are continuously monitored during operation by comparing their values to complimentary shadow registers. If a mismatch is detected between the two sets of registers, a CM Reset automatically occurs. These events are captured by the CM bit (RCON<5>). The state of the bit is set to '0' whenever a CM event occurs; it does not change for any other Reset event.

A CM Reset behaves similarly to a Master Clear Reset, RESET instruction, WDT time-out or Stack Event Resets. As with all hard and power Reset events, the device Configuration Words are reloaded from the Flash Configuration Words in program memory as the device restarts.

5.6 Power-up Timer (PWRT)

PIC18F45J10 family devices incorporate an on-chip Power-up Timer (PWRT) to help regulate the Power-on Reset process. The PWRT is always enabled. The main function is to ensure that the device voltage is stable before code is executed.

The Power-up Timer (PWRT) of the PIC18F45J10 family devices is an 11-bit counter which uses the INTRC source as the clock input. This yields an approximate time interval of 2048 x 32 μ s = 65.6 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC clock and will vary from chip to chip due to temperature and process variation. See DC parameter 33 for details.

5.6.1 TIME-OUT SEQUENCE

If enabled, the PWRT time-out is invoked after the POR pulse has cleared. The total time-out will vary based on the status of the PWRT. Figure 5-3, Figure 5-4, Figure 5-5 and Figure 5-6 all depict time-out sequences on power-up with the Power-up Timer enabled.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the PWRT will expire. Bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 5-5). This is useful for testing purposes, or to synchronize more than one PIC18F device operating in parallel.



FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD, VDD RISE < TPWRT)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	50
LATC	PORTC Data Latch Register (Read and Write to Data Latch)							50	
TRISC	PORTC Da	PORTC Data Direction Control Register							50

TABLE 10-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	47
RCON	IPEN	—	CM	RI	TO	PD	POR	BOR	46
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	49
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	49
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	49
TRISB	PORTB Da	ata Direction	Control Regi	ster					50
TRISC	PORTC Da	ata Direction	Control Reg	ister					50
TMR2	Timer2 Reg	gister							48
PR2	Timer2 Per	riod Register							48
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	48
CCPR1L	Capture/Co	ompare/PWN	I Register 1	Low Byte					49
CCPR1H	Capture/Co	ompare/PWN	1 Register 1	High Byte					49
CCP1CON	P1M1 ⁽¹⁾	P1M0 ⁽¹⁾	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	49
CCPR2L	Capture/Co	ompare/PWN	I Register 2	Low Byte					49
CCPR2H	Capture/Co	ompare/PWN	1 Register 2	High Byte					49
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	49
ECCP1AS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1 ⁽¹⁾	PSSBD0 ⁽¹⁾	49
ECCP1DEL	PRSEN	PDC6 ⁽¹⁾	PDC5 ⁽¹⁾	PDC4 ⁽¹⁾	PDC3 ⁽¹⁾	PDC2 ⁽¹⁾	PDC1 ⁽¹⁾	PDC0 ⁽¹⁾	49

TABLE 14-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PWM or Timer2.

Note 1: These bits are not implemented on 28-pin devices and should be read as '0'.

15.4.5 FULL-BRIDGE MODE

In Full-Bridge Output mode, four pins are used as outputs; however, only two outputs are active at a time. In the Forward mode, pin P1A is continuously active and pin P1D is modulated. In the Reverse mode, pin P1C is continuously active and pin P1B is modulated. These are illustrated in Figure 15-6. P1A, P1B, P1C and P1D outputs are multiplexed with the PORTC<2> and PORTD<7:5> data latches. The TRISC<2> and TRISD<7:5> bits must be cleared to make the P1A, P1B, P1C and P1D pins outputs.





16.4.3.3 Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and the SDAx line is held low (ACK).

When the address byte overflow condition exists, then the no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit, BF (SSPxSTAT<0>), is set, or bit, SSPOV (SSPxCON1<6>), is set.

An MSSP interrupt is generated for each data transfer byte. The interrupt flag bit, SSPxIF, must be cleared in software. The SSPxSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPxCON2<0> = 1), SCKx/SCLx (RC3 or RD0) will be held low (clock stretch) following each data transfer. The clock must be released by setting bit, CKP (SSPxCON1<4>). See **Section 16.4.4** "**Clock Stretching**" for more details.

16.4.3.4 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPxSTAT register is set. The received address is loaded into the SSPxBUF register. The ACK pulse will be sent on the ninth bit and pin RC3 or RD6 is held low, regardless of SEN (see Section 16.4.4 "Clock Stretching" for more details). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPxBUF register which also loads the SSPxSR register. Then pin RC3 or RD0 should be enabled by setting bit, CKP (SSPxCON1<4>). The eight data bits are shifted out on the falling edge of the SCLx input. This ensures that the SDAx signal is valid during the SCLx high time (Figure 16-9).

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCLx input pulse. If the SDAx line is high (not ACK), then the data transfer is complete. In this case, when the ACK is latched by the slave, the slave logic is reset (resets SSPxSTAT register) and the slave monitors for another occurrence of the Start bit. If the SDAx line was low (ACK), the next transmit data must be loaded into the SSPxBUF register. Again, pin RC3 or RD0 must be enabled by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPxIF bit must be cleared in software and the SSPxSTAT register is used to determine the status of the byte. The SSPxIF bit is set on the falling edge of the ninth clock pulse.

17.1.3 AUTO-BAUD RATE DETECT

The Enhanced USART module supports the automatic detection and calibration of baud rate. This feature is active only in Asynchronous mode and while the WUE bit is clear.

The automatic baud rate measurement sequence (Figure 17-1) begins whenever a Start bit is received and the ABDEN bit is set. The calculation is self-averaging.

In the Auto-Baud Rate Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. In ABD mode, the internal Baud Rate Generator is used as a counter to time the bit period of the incoming serial byte stream.

Once the ABDEN bit is set, the state machine will clear the BRG and look for a Start bit. The Auto-Baud Rate Detect must receive a byte with the value 55h (ASCII "U", which is also the LIN/J2602 bus Sync character) in order to calculate the proper bit rate. The measurement is taken over both a low and a high bit time in order to minimize any effects caused by asymmetry of the incoming signal. After a Start bit, the SPBRG begins counting up, using the preselected clock source on the first rising edge of RX. After eight bits on the RX pin or the fifth rising edge, an accumulated value totalling the proper BRG period is left in the SPBRGH:SPBRG register pair. Once the 5th edge is seen (this should correspond to the Stop bit), the ABDEN bit is automatically cleared.

If a rollover of the BRG occurs (an overflow from FFFFh to 0000h), the event is trapped by the ABDOVF status bit (BAUDCON<7>). It is set in hardware by BRG rollovers and can be set or cleared by the user in software. ABD mode remains active after rollover events and the ABDEN bit remains set (Figure 17-2).

While calibrating the baud rate period, the BRG registers are clocked at 1/8th the preconfigured clock rate. Note that the BRG clock will be configured by the BRG16 and BRGH bits. Independent of the BRG16 bit setting, both the SPBRG and SPBRGH will be used as a 16-bit counter. This allows the user to verify that no carry occurred for 8-bit modes by checking for 00h in the SPBRGH register. Refer to Table 17-4 for counter clock rates to the BRG.

While the ABD sequence takes place, the EUSART state machine is held in Idle. The RCIF interrupt is set once the fifth rising edge on RX is detected. The value in the RCREG needs to be read to clear the RCIF interrupt. The contents of RCREG should be discarded.

- Note 1: If the WUE bit is set with the ABDEN bit, Auto-Baud Rate Detection will occur on the byte *following* the Break character.
 - 2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible due to bit error rates. Overall system timing and communication baud rates must be taken into consideration when using the Auto-Baud Rate Detection feature.

TABLE 17-4:BRG COUNTERCLOCK RATES

BRG16	BRGH	BRG Counter Clock
0	0	Fosc/512
0	1	Fosc/128
1	0	Fosc/128
1	1	Fosc/32

Note: During the ABD sequence, SPBRG and SPBRGH are both used as a 16-bit counter, independent of BRG16 setting.

17.1.3.1 ABD and EUSART Transmission

Since the BRG clock is reversed during ABD acquisition, the EUSART transmitter cannot be used during ABD. This means that whenever the ABDEN bit is set, TXREG cannot be written to. Users should also ensure that ABDEN does not become set during a transmit sequence. Failing to do this may result in unpredictable EUSART operation.

19.1 Comparator Configuration

There are eight modes of operation for the comparators, shown in Figure 19-1. Bits, CM<2:0> of the CMCON register, are used to select these modes. The TRISA register controls the data direction of the comparator pins for each mode. If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in **Section 24.0 "Electrical Characteristics"**.

Note: Comparator interrupts should be disabled during a Comparator mode change; otherwise, a false interrupt may occur.



19.2 Comparator Operation

A single comparator is shown in Figure 19-2, along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input, VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input, VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 19-2 represent the uncertainty due to input offsets and response time.

19.3 Comparator Reference

Depending on the comparator operating mode, either an external or internal voltage reference may be used. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly (Figure 19-2).





19.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between Vss and VDD and can be applied to either pin of the comparator(s).

19.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference from the comparator voltage reference module. This module is described in more detail in **Section 20.0 "Comparator Voltage Reference Module"**.

The internal reference is only available in the mode where four inputs are multiplexed to two comparators (CM<2:0> = 110). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

19.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (see Section 24.0 "Electrical Characteristics").

19.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RB5 and RA5 I/O pins. When enabled, multiplexors in the output path of the RB5 and RA5 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 19-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/ disable for the RB5 and RA5 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<5:4>).

- Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
 - 2: Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

PIC18F45J10 FAMILY

	LW	Multiply	Multiply Literal with W							
Synt	ax:	MULLW	MULLW k							
Oper	ands:	$0 \le k \le 255$	$0 \le k \le 255$							
Oper	ation:	(W) x k \rightarrow	(W) x k \rightarrow PRODH:PRODL							
Statu	is Affected:	None	None							
Enco	oding:	0000	1101	kkkk	kkkk					
Desc	cription:	An unsigne out betwee 8-bit literal placed in ti pair. PROD W is uncha None of th Note that r possible in is possible	An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in the PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged. None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.							
Word	ds:	1								
Cycle	es:	1								
00	ycle Activity:									
<u>a</u> 0										
QU	Q1	Q2	Q3		Q4					
	Q1 Decode	Q2 Read literal 'k'	Q3 Proces Data	ss P F	Q4 Write egisters RODH: PRODL					
Exar	Q1 Decode	Q2 Read literal 'k'	Q3 Proces Data	ss re P F	Q4 Write egisters RODH: PRODL					
Exar	Q1 Decode nple: Before Instruc	Q2 Read literal 'k' ^{MULLW}	Q3 Proces Data	ss P F	Q4 Write egisters RODH: PRODL					

MULWF	Multiply	W with f						
Syntax:	MULWF	f {,a}						
Operands:	0 ≤ f ≤ 255 a ∈ [0 , 1]	$\begin{array}{l} 0 \leq f \leq 255 \\ a \in \left[0 , 1 \right] \end{array}$						
Operation:	(W) x (f) –	(W) x (f) \rightarrow PRODH:PRODL						
Status Affected:	None	None						
Encoding:	0000	001a f	fff	ffff				
Description:	An unsign out betwee register file result is st register pa high byte. unchange None of th Note that 1 possible ir result is pr If 'a' is '0', selected. I to select th If 'a' is '0' a set is enal operates i Addressin $f \le 95$ (5FH ''Byte-Oric Instructio Mode'' for	An unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged. None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (SFh). See Section 22.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset						
Words:	1	uctans.						
Cycles:	1							
	I							
	02	03		04				
Decode	Read	Process		Write				
	register 'f'	Data	re P F	egisters RODH: PRODL				
Example:	MULWF	REG, 1						
Before Instruc	tion							
W REG PRODH PRODL After Instructio	= C4 = B5 = ? = ?	łh ih						

W	=	C4h
REG	=	B5h
PRODH	=	8Ah
PRODL	=	94h

23.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft[®] Windows[®] 32-bit operating system were chosen to best make these features available in a simple, unified application.

23.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

23.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers costeffective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

23.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

24.1 DC Characteristics: Supply Voltage PIC18F24J10/25J10/44J10/45J10 (Industrial) PIC18LF24J10/25J10/44J10/45J10 (Industrial)

PIC18F45J10 Family (Industrial)			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial				
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
D001	Vdd	Supply Voltage	VDDCORE	—	3.6	V	PIC18LF4XJ10, PIC18LF2XJ10
D001	Vdd	Supply Voltage	2.7 ⁽¹⁾	_	3.6	V	PIC18F4X/2XJ10
D001B	VDDCORE	External Supply for Microcontroller Core	2.0	_	2.7	V	Valid only in parts designated "LF". See Section 21.3 "On-Chip Voltage Regulator" for details.
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	1.5	_	_	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	—	0.15	V	SeeSection 5.3 "Power-on Reset (POR)" for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	_	_	V/ms	See Section 5.3 "Power-on Reset (POR)" for details
D005	VBOR	Brown-out Reset (BOR) Voltage	2.35	2.5	2.7	V	

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C \leq TA \leq +85°C for industrial					
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
		Program Flash Memory						
D130	Ер	Cell Endurance	100	1K	—	E/W	-40°C to +85°C	
D131	Vpr	VDD for Read	VMIN	_	3.6	V	Vмın = Minimum operating voltage	
D132B	Vpew	Voltage for Self-Timed Erase or Write:						
		VDD	2.7	—	3.6	V	PIC18FXXJ10	
		VDDCORE	2.25	—	2.7	V	PIC18LFXXJ10	
D133A	Tiw	Self-Timed Write Cycle Time	—	2.8	—	ms		
D133B	TIE	Self-Timed Page Erased Cycle Time	—	33.0	—	ms		
D134	Tretd	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated	
D135	IDDP	Supply Current during Programming	_	10	—	mA		

TABLE 24-1: MEMORY PROGRAMMING REQUIREMENTS

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

24.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 24-5 apply to all timing specifications unless otherwise noted. Figure 24-3 specifies the load conditions for the timing specifications.

TABLE 24-5: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions (unless otherwise stated)						
	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial						
AC CHARACTERISTICS	Operating voltage VDD range as described in DC spec Section 24.1 and						
	Section 24.3.						

FIGURE 24-3: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS





FIGURE 24-11: EXAMPLE SPI[™] MASTER MODE TIMING (CKE = 1)

TABLE 24-15: EXAMPLE SPI™ MODE REQUIREMENTS (CKE = 1)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
73	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	ns	
73A	Тв2в	Last Clock Edge of Byte 1 to the 1st Clock Edge of Byte 2	1.5 Tcy + 40		ns	(Note 1)
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	40	_	ns	
75	TDOR	SDOx Data Output Rise Time	—	25	ns	
76	TDOF	SDOx Data Output Fall Time	—	25	ns	
78	TscR	SCKx Output Rise Time (Master mode)	—	25	ns	
79	TscF	SCKx Output Fall Time (Master mode)	_	25	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	50	ns	
81	TDOV2SCH, TDOV2SCL	SDOx Data Output Setup to SCKx Edge	Тсү	_	ns	

Note 1: Only if Parameter #71A and #72A are used.



FIGURE 24-13: EXAMPLE SPI[™] SLAVE MODE TIMING (CKE = 1)

TABLE 24-17: EXAMPLE SPI™ SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input		Тсү		ns	
71	TscH	SCKx Input High Time	Continuous	1.25 Tcy + 30	—	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCKx Input Low Time	Continuous	1.25 Tcy + 30		ns	
72A		(Slave mode)	Single Byte	40		ns	(Note 1)
73A	Тв2в	Last Clock Edge of Byte 1 to the First	Clock Edge of Byte 2	1.5 Tcy + 40	_	ns	(Note 2)
74	TscH2DIL, TscL2DIL	Hold Time of SDIx Data Input to SCKx Edge		20	_	ns	
75	TDOR	SDOx Data Output Rise Time	Data Output Rise Time		25	ns	
76	TDOF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	SSx ↑ to SDOx Output High-Impedance		10	50	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx	Edge	—	50	ns	
82	TssL2doV	SDOx Data Output Valid after $\overline{\text{SSx}}$ \downarrow	after SSx ↓ Edge		50	ns	
83	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge		1.5 Tcy + 40		ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.



TABLE 24-18: I²C[™] BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characte	Min	Мах	Units	Conditions		
90	TSU:STA	Start Condition	100 kHz mode	4700		ns	Only relevant for Repeated	
		Setup Time	400 kHz mode	600			Start condition	
91	THD:STA	Start Condition	100 kHz mode	4000	—	ns	After this period, the first	
		Hold Time	400 kHz mode	600	—		clock pulse is generated	
92	Tsu:sto	Stop Condition	100 kHz mode	4700	—	ns		
		Setup Time	400 kHz mode	600	—			
93	THD:STO	Stop Condition	100 kHz mode	4000	—	ns		
		Hold Time	400 kHz mode	600	—			

FIGURE 24-15: I²C[™]

I²C[™] BUS DATA TIMING



Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	Thigh	Clock High Time	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			400 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	
101	TLOW	Clock Low Time	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			400 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	
102	TR	SDAx and SCLx	100 kHz mode	_	1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	_	300	ns	
103	TF	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾		100	ns	
90	Tsu:sta	Start Condition Setup Time	100 kHz mode	2(Tosc)(BRG + 1)	—	ms	Only relevant for
			400 kHz mode	2(Tosc)(BRG + 1)	_	ms	Repeated Start
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	condition
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	After this period, the first
			400 kHz mode	2(Tosc)(BRG + 1)	_	ms	clock pulse is generated
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	_	ns	
			400 kHz mode	0	0.9	ms	
			1 MHz mode ⁽¹⁾	_	_	ns	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	_	ns	(Note 2)
			400 kHz mode	100	_	ns	
				1 MHz mode ⁽¹⁾	_	_	ns
92	Tsu:sto	Stop Condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	
		Setup Time	400 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	
109	ΤΑΑ	Output Valid	100 kHz mode	_	3500	ns	
		from Clock	400 kHz mode	_	1000	ns	
			1 MHz mode ⁽¹⁾	_	_	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	_	ms	Time the bus must be free
			400 kHz mode	1.3	—	ms	before a new transmission
			1 MHz mode ⁽¹⁾	—	_	ms	can start
D102	Св	Bus Capacitive L	oading	—	400	pF	

TABLE 24-21: MASTER SSP I²C[™] BUS DATA REQUIREMENTS

Note 1: Maximum pin capacitance = 10 pF for all I^2C^{TM} pins.

2: A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but parameter #107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, parameter #102 + parameter #107 = 1000 + 250 = 1250 ns (for 100 kHz mode), before the SCLx line is released.