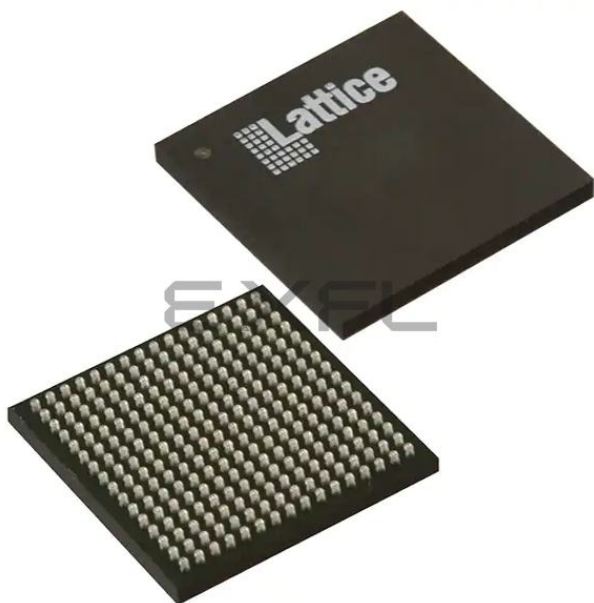




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

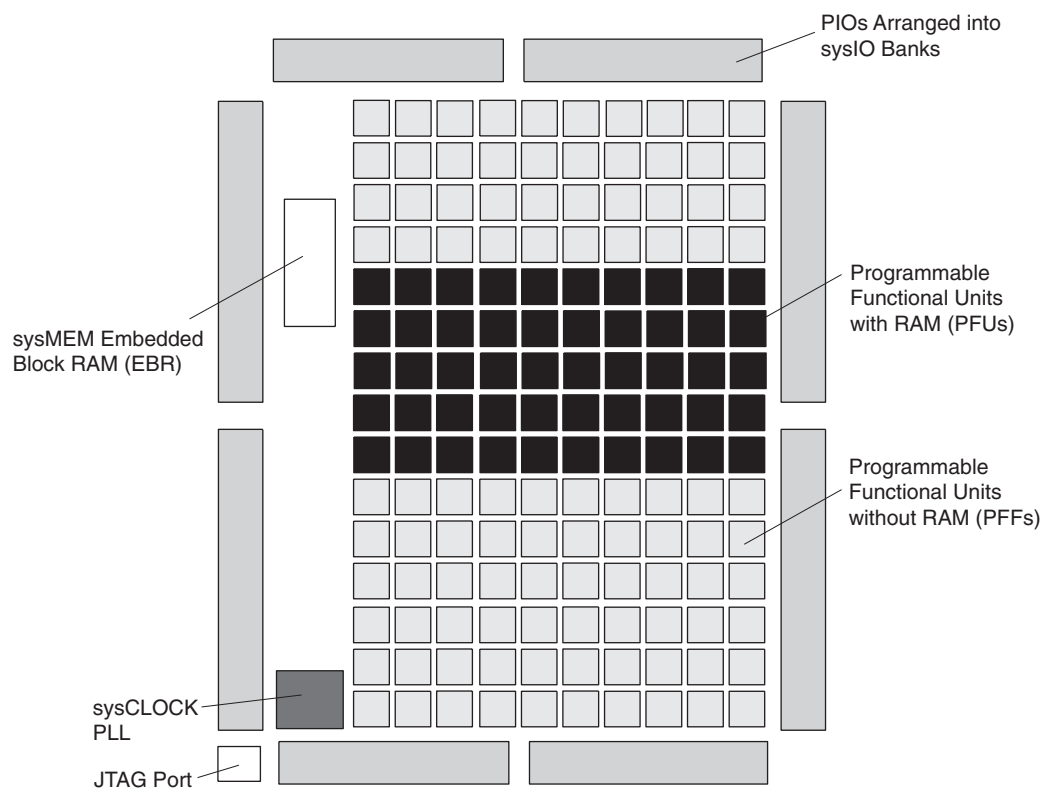
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

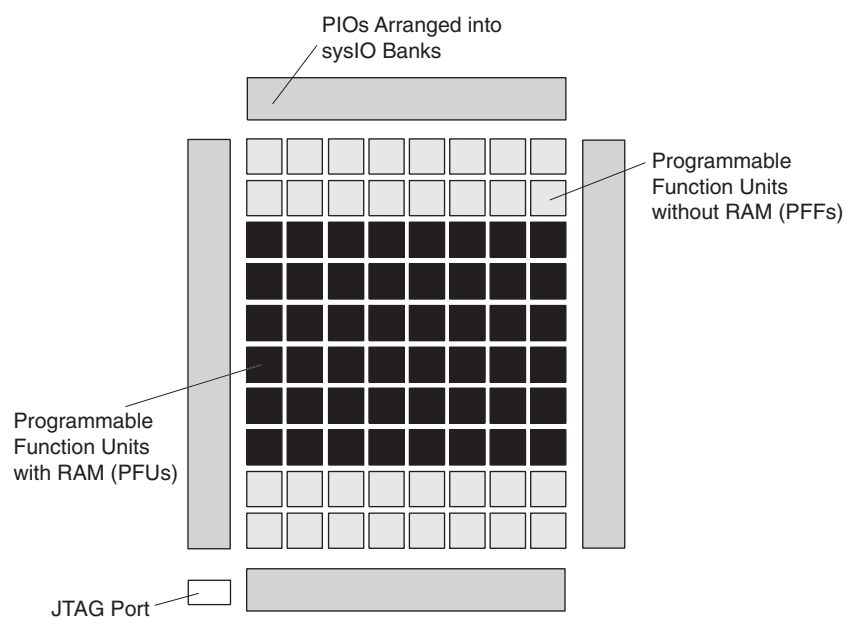
Product Status	Active
Number of LABs/CLBs	150
Number of Logic Elements/Cells	1200
Total RAM Bits	9421
Number of I/O	211
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA, CSPBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200c-3bn256c

Figure 2-1. Top View of the MachXO1200 Device¹



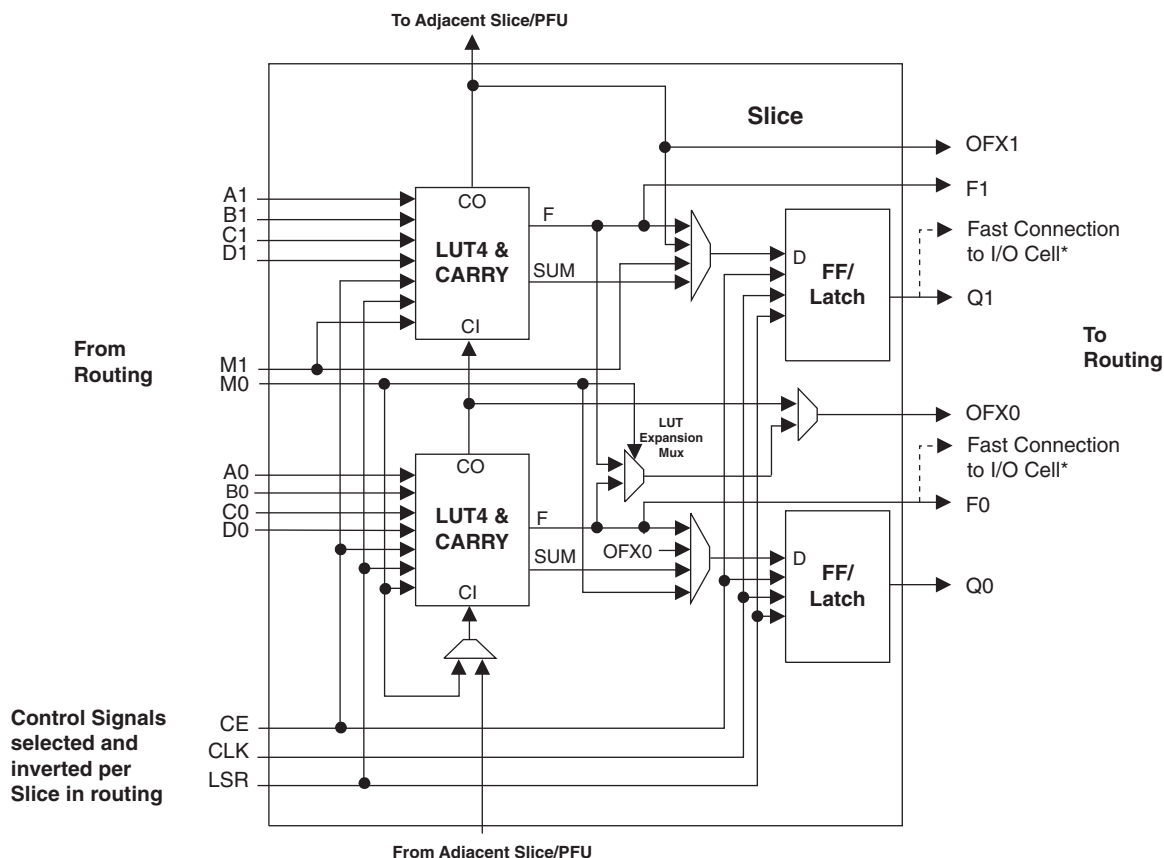
1. Top view of the MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the MachXO640 Device



There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2-1 lists the signals associated with each Slice.

Figure 2-5. Slice Diagram



Notes:

Some inter-Slice signals are not shown.

* Only PFUs at the edges have fast connections to the I/O cell.

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the Slice
Output	Inter-PFU signal	FCO	Fast Carry Out ¹

1. See Figure 2-4 for connection details.

2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

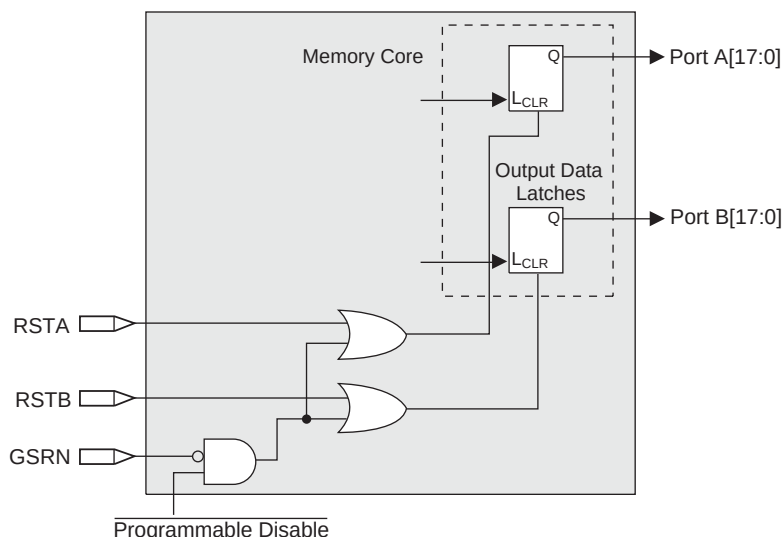
The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-13. Memory Core Reset

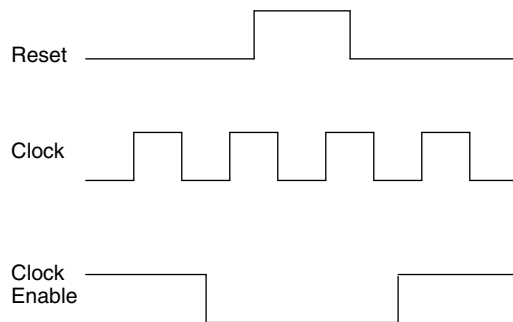


For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPRreset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs.

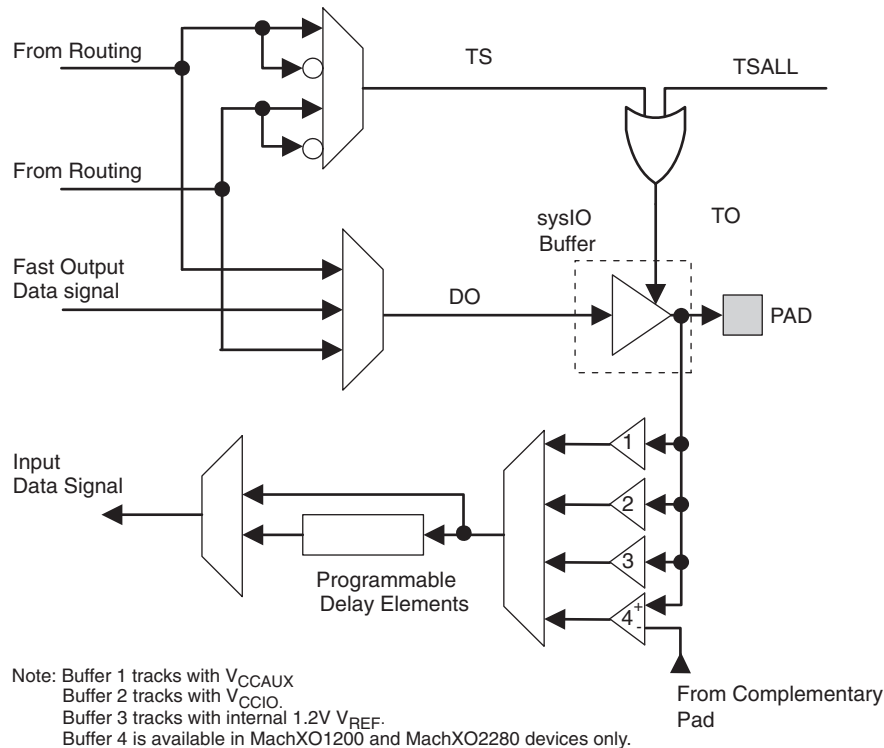
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled

output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 2-17 shows the MachXO PIO logic.

The tristate control signal is multiplexed from the output data signals and their complements. In addition a global signal (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the device. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

Figure 2-17. MachXO PIO Block Diagram



sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the MachXO devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . In addition to the Bank V_{CCIO} supplies, the MachXO devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

MachXO256 and MachXO640 devices contain single-ended input buffers and single-ended output buffers with complementary outputs on all the I/O Banks.

MachXO1200 and MachXO2280 devices contain two types of sysIO buffer pairs.

1. Top and Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the top and bottom Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom

Figure 2-18. MachXO2280 Banks

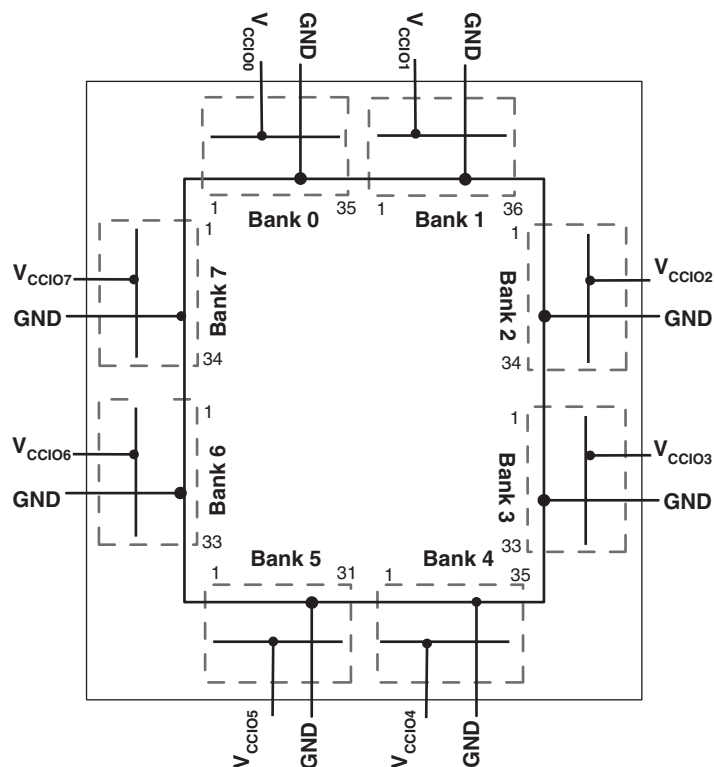
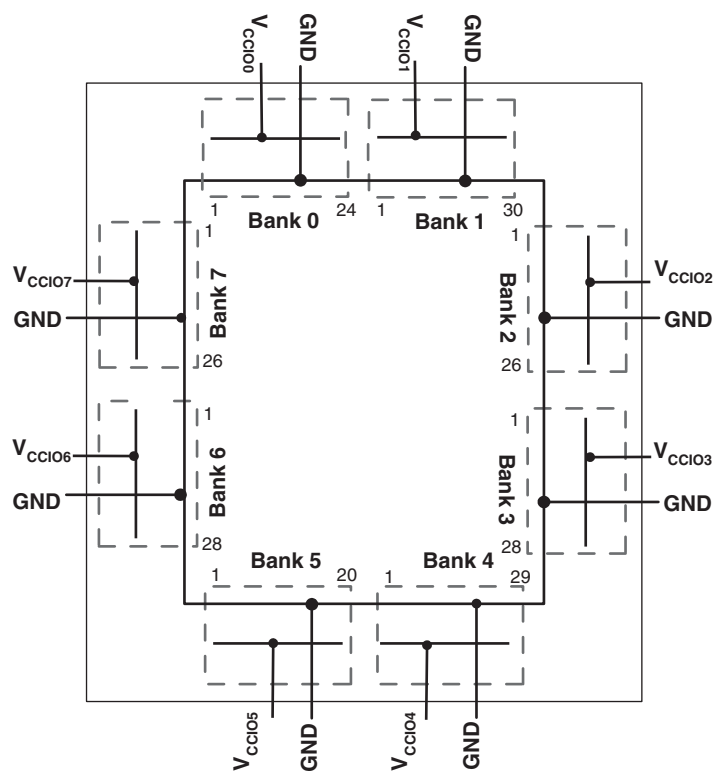


Figure 2-19. MachXO1200 Banks



the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The MachXO “C” devices ($V_{CC} = 1.8/2.5/3.3V$) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

Table 2-11. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <10mA	0	Typical <100uA
I/O Leakage	<10μA	<1mA	<10μA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1} ; MachXO640: V_{CCIO2} ; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-22 provides a pictorial representation of the different programming modes available in the MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

Leave Alone I/O

When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

Security

The MachXO devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Initialization Supply Current^{1, 2, 3, 4}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMXO256C	13	mA
		LCMXO640C	17	mA
		LCMXO1200C	21	mA
		LCMXO2280C	23	mA
		LCMXO256E	10	mA
		LCMXO640E	14	mA
		LCMXO1200E	18	mA
		LCMXO2280E	20	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LCMXO256E/C	10	mA
		LCMXO640E/C	13	mA
		LCMXO1200E/C	24	mA
		LCMXO2280E/C	25	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all I/O pins are held at V_{CCIO} or GND.

3. Frequency = 0MHz.

4. Typical user pattern.

5. $T_J = 25^\circ C$, power supplies at nominal voltage.

6. Per Bank, $V_{CCIO} = 2.5V$. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMXO256C	9	mA
		LCMXO640C	11	mA
		LCMXO1200C	16	mA
		LCMXO2280C	22	mA
		LCMXO256E	6	mA
		LCMXO640E	8	mA
		LCMXO1200E	12	mA
		LCMXO2280E	14	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LCMXO256C/E	8	mA
		LCMXO640C/E	10	mA
		LCMXO1200E	15	mA
		LCMXO2280C/E	16	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all I/O pins are held at V_{CCIO} or GND.

3. Typical user pattern.

4. JTAG programming is at 25MHz.

5. $T_J = 25^\circ C$, power supplies at nominal voltage.

6. Per Bank, $V_{CCIO} = 2.5V$. Does not include pull-up/pull-down.

sysIO Differential Electrical Characteristics

LVDS

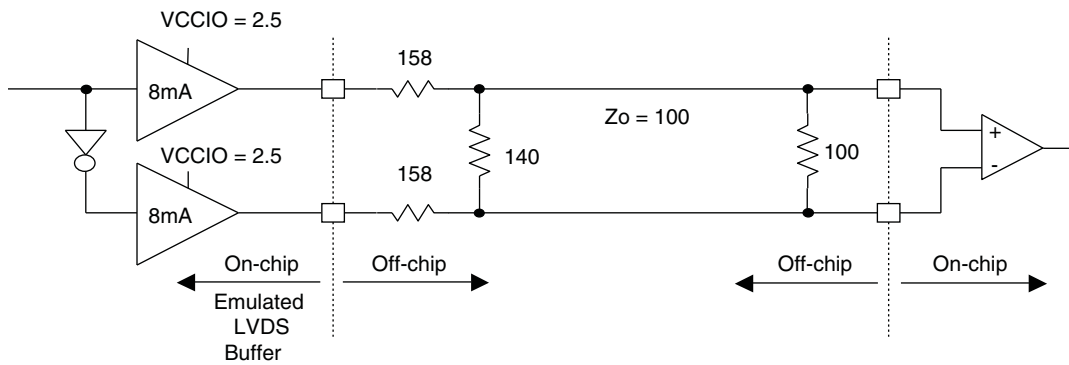
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{THD}	Differential Input Threshold		+/-100	—	—	mV
V_{CM}	Input Common Mode Voltage	$100\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	1.8	V
		$200\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	1.9	V
		$350\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	2.0	V
I_{IN}	Input current	Power on	—	—	+/-10	μA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100 \text{ Ohm}$	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100 \text{ Ohm}$	0.9V	1.03	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM})$, $R_T = 100 \text{ Ohm}$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} - V_{OM})/2$, $R_T = 100 \text{ Ohm}$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0\text{V}$ Driver outputs shorted	—	—	6	mA

LVDS Emulation

MachXO devices can support LVDS outputs via emulation (LVDS25E), in addition to the LVDS support that is available on-chip on certain devices. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are $\pm 1\%$.

The LVDS differential input buffers are available on certain devices in the MachXO family.

Table 3-2. BLVDS DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Z _o = 45	Z _o = 90	
Z _{OUT}	Output impedance	100	100	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

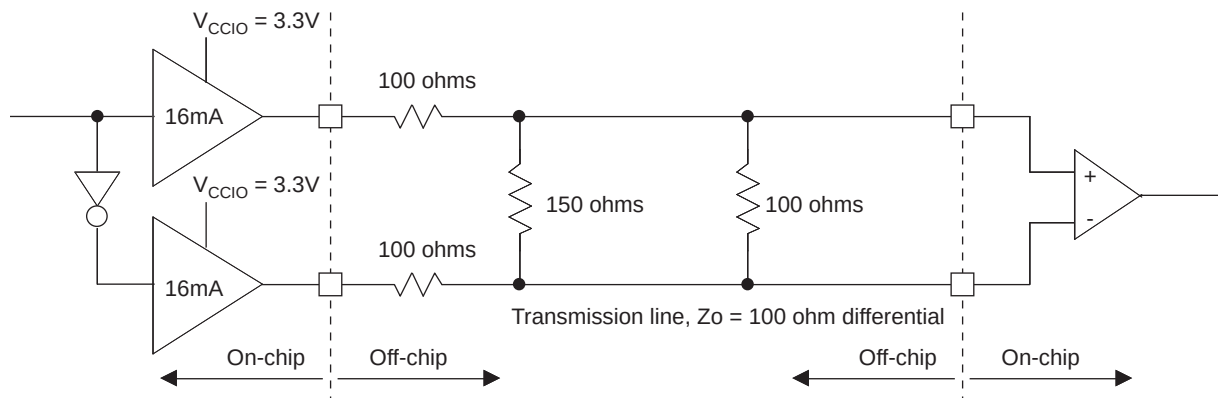


Table 3-3. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	100	Ohms
R _P	Driver parallel resistor	150	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	2.03	V
V _{OL}	Output low voltage	1.27	V
V _{OD}	Output differential voltage	0.76	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	85.7	Ohms
I _{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

LCMX0256 and LCMX0640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMX0256				LCMX0640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
43	PB4A	1		T	PB8B	2		
44	PB4B	1		C	PB8C	2		T
45	PB4C	1		T	PB8D	2		C
46	PB4D	1		C	PB9A	2		
47	PB5A	1			PB9C	2		T
48*	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
49	PB5C	1		T	PB9D	2		C
50	PB5D	1		C	PB9F	2		
51	PR9B	0		C	PR11D	1		C
52	PR9A	0		T	PR11B	1		C
53	PR8B	0		C	PR11C	1		T
54	PR8A	0		T	PR11A	1		T
55	PR7D	0		C	PR10D	1		C
56	PR7C	0		T	PR10C	1		T
57	PR7B	0		C	PR10B	1		C
58	PR7A	0		T	PR10A	1		T
59	PR6B	0		C	PR9D	1		
60	VCCIO0	0			VCCIO1	1		
61	PR6A	0		T	PR9B	1		
62	GNDIO0	0			GNDIO1	1		
63	PR5D	0		C	PR7B	1		
64	PR5C	0		T	PR6C	1		
65	PR5B	0		C	PR6B	1		
66	PR5A	0		T	PR5D	1		
67	PR4B	0		C	PR5B	1		
68	PR4A	0		T	PR4D	1		
69	PR3D	0		C	PR4B	1		
70	PR3C	0		T	PR3D	1		
71	PR3B	0		C	PR3B	1		
72	PR3A	0		T	PR2D	1		
73	PR2B	0		C	PR2B	1		
74	VCCIO0	0			VCCIO1	1		
75	GNDIO0	0			GNDIO1	1		
76	PR2A	0		T	PT9F	0		C
77	PT5C	0			PT9E	0		T
78	PT5B	0		C	PT9C	0		
79	PT5A	0		T	PT9A	0		
80	PT4F	0		C	VCCIO0	0		
81	PT4E	0		T	GNDIO0	0		
82	PT4D	0		C	PT7E	0		
83	PT4C	0		T	PT7A	0		
84	GND	-			GND	-		

LCMX01200 and LCMX02280 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMX01200				LCMX02280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
42	PB9A	4		T	PB12A	4		T
43	PB9B	4		C	PB12B	4		C
44	VCCIO4	4			VCCIO4	4		
45	PB10A	4		T	PB13A	4		T
46	PB10B	4		C	PB13B	4		C
47***	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
48	PB11A	4		T	PB16A	4		T
49	PB11B	4		C	PB16B	4		C
50**	GNDIO3 GNDIO4	-			GNDIO3 GNDIO4	-		
51	PR16B	3			PR19B	3		
52	PR15B	3		C*	PR18B	3		C*
53	PR15A	3		T*	PR18A	3		T*
54	PR14B	3		C*	PR17B	3		C*
55	PR14A	3		T*	PR17A	3		T*
56	VCCIO3	3			VCCIO3	3		
57	PR12B	3		C*	PR15B	3		C*
58	PR12A	3		T*	PR15A	3		T*
59	GND	-			GND	-		
60	PR10B	3		C*	PR13B	3		C*
61	PR10A	3		T*	PR13A	3		T*
62	PR9B	3		C*	PR11B	3		C*
63	PR9A	3		T*	PR11A	3		T*
64	PR8B	2		C*	PR10B	2		C*
65	PR8A	2		T*	PR10A	2		T*
66	VCC	-			VCC	-		
67	PR6C	2			PR8C	2		
68	PR6B	2		C*	PR8B	2		C*
69	PR6A	2		T*	PR8A	2		T*
70	VCCIO2	2			VCCIO2	2		
71	PR4D	2			PR5D	2		
72	PR4B	2		C*	PR5B	2		C*
73	PR4A	2		T*	PR5A	2		T*
74	PR2B	2		C	PR3B	2		C*
75	PR2A	2		T	PR3A	2		T*
76**	GNDIO1 GNDIO2	-			GNDIO1 GNDIO2	-		
77	PT11C	1			PT15C	1		
78	PT11B	1		C	PT14B	1		C
79	PT11A	1		T	PT14A	1		T
80	VCCIO1	1			VCCIO1	1		
81	PT9E	1			PT12D	1		C

LCMX0256 and LCMX0640 Logic Signal Connections: 100 csBGA

LCMX0256					LCMX0640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
B1	PL2A	1		T	B1	PL2A	3		T
C1	PL2B	1		C	C1	PL2C	3		T
D2	PL3A	1		T	D2	PL2B	3		C
D1	PL3B	1		C	D1	PL2D	3		C
C2	PL3C	1		T	C2	PL3A	3		T
E1	PL3D	1		C	E1	PL3B	3		C
E2	PL4A	1		T	E2	PL3C	3		T
F1	PL4B	1		C	F1	PL3D	3		C
F2	PL5A	1		T	F2	PL4A	3		
G2	PL5B	1		C	G2	PL4C	3		T
H1	GNDIO1	1			H1	GNDIO3	3		
H2	PL5C	1		T	H2	PL4D	3		C
J1	PL5D	1	GSRN	C	J1	PL5B	3	GSRN	
J2	PL6A	1		T	J2	PL7B	3		
K1	PL6B	1	TSALL	C	K1	PL8C	3	TSALL	T
K2	PL7A	1		T	K2	PL8D	3		C
L1	PL7B	1		C	L1	PL9A	3		
L2	PL7C	1		T	L2	PL9C	3		
M1	PL7D	1		C	M1	PL10A	3		
M2	PL8A	1		T	M2	PL10C	3		
N1	PL8B	1		C	N1	PL11A	3		
M3	PL9A	1		T	M3	PL11C	3		
N2	GNDIO1	1			N2	GNDIO3	3		
P2	TMS	1	TMS		P2	TMS	2	TMS	
P3	PL9B	1		C	P3	PB2C	2		
N4	TCK	1	TCK		N4	TCK	2	TCK	
P4	PB2A	1		T	P4	VCCIO2	2		
N3	PB2B	1		C	N3	GNDIO2	2		
P5	TDO	1	TDO		P5	TDO	2	TDO	
N5	PB2C	1		T	N5	PB4C	2		
P6	TDI	1	TDI		P6	TDI	2	TDI	
N6	PB2D	1		C	N6	PB4E	2		
P7	VCC	-			P7	VCC	-		
N7	PB3A	1	PCLK1_1**	T	N7	PB5B	2	PCLK2_1**	
P8	PB3B	1		C	P8	PB5D	2		
N8	PB3C	1	PCLK1_0**	T	N8	PB6B	2	PCLK2_0**	
P9	PB3D	1		C	P9	PB6C	2		
N10	GNDIO1	1			N10	GNDIO2	2		
P11	PB4A	1		T	P11	PB8B	2		
N11	PB4B	1		C	N11	PB8C	2		T
P12	PB4C	1		T	P12	PB8D	2		C
N12	PB4D	1		C	N12	PB9A	2		

LCMX0256 and LCMX0640 Logic Signal Connections: 100 csBGA (Cont.)

LCMX0256					LCMX0640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A4	GNDIO0	0			A4	GNDIO0	0		
B4	PT3A	0		T	B4	PT3B	0		C
A3	PT2F	0		C	A3	PT3A	0		T
B3	PT2E	0		T	B3	PT2F	0		C
A2	PT2D	0		C	A2	PT2E	0		T
C3	PT2C	0		T	C3	PT2B	0		C
A1	PT2B	0		C	A1	PT2C	0		
B2	PT2A	0		T	B2	PT2A	0		T
N9	GND	-			N9	GND	-		
B9	GND	-			B9	GND	-		
B5	VCCIO0	0			B5	VCCIO0	0		
A14	VCCIO0	0			A14	VCCIO1	1		
H14	VCCIO0	0			H14	VCCIO1	1		
P10	VCCIO1	1			P10	VCCIO2	2		
G1	VCCIO1	1			G1	VCCIO3	3		
P1	VCCIO1	1			P1	VCCIO3	3		

*NC for "E" devices.

**Primary clock inputs are single-ended.

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1***	C	A8	PT7D	1	PCLK1_1***		A8	PT10B	1	PCLK1_1***	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0***	C	C8	PT6F	0	PCLK1_0***		C8	PT9B	1	PCLK1_0***	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	-			A7	VCCAUX	-			A7	VCCAUX	-		
C7	VCC	-			C7	VCC	-			C7	VCC	-		
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	-			F1	GND	-			F1	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
C9	GND	-			C9	GND	-			C9	GND	-		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

LCMX02280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMX02280				
Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO3	3		
VCCIO3	VCCIO3	3		
P15	PR20B	3		C
N14	PR20A	3		T
N15	PR19B	3		C
M13	PR19A	3		T
R15	PR18B	3		C*
T16	PR18A	3		T*
N16	PR17D	3		C
M14	PR17C	3		T
U17	PR17B	3		C*
VCC	VCC	-		
U18	PR17A	3		T*
R17	PR16D	3		C
R16	PR16C	3		T
P16	PR16B	3		C*
VCCIO3	VCCIO3	3		
GND	GNDIO3	3		
P17	PR16A	3		T*
L13	PR15D	3		C
M15	PR15C	3		T
T17	PR15B	3		C*
T18	PR15A	3		T*
L14	PR14D	3		C
L15	PR14C	3		T
R18	PR14B	3		C*
P18	PR14A	3		T*
GND	GND	-		
K15	PR13D	3		C
K13	PR13C	3		T
N17	PR13B	3		C*
N18	PR13A	3		T*
K16	PR12D	3		C
K14	PR12C	3		T
M16	PR12B	3		C*
L16	PR12A	3		T*
GND	GNDIO3	3		
VCCIO3	VCCIO3	3		
J16	PR11D	3		C
J14	PR11C	3		T
M17	PR11B	3		C*
L17	PR11A	3		T*
J15	PR10D	2		C

Conventional Packaging
Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM
LCMXO256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM
LCMXO256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM
LCMXO256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM
LCMXO256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM
LCMXO256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMXO640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMXO640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMXO640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMXO640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMXO640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMXO640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMXO640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMXO640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMXO640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMXO640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMXO640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMXO1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMXO1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMXO1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMXO1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMXO1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMXO1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMXO1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMXO1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM

Conventional Packaging
Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMX0256C-3T100I	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	IND
LCMX0256C-4T100I	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	IND
LCMX0256C-3M100I	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	IND
LCMX0256C-4M100I	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMX0640C-3T100I	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	IND
LCMX0640C-4T100I	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	IND
LCMX0640C-3M100I	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	IND
LCMX0640C-4M100I	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	IND
LCMX0640C-3T144I	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMX0640C-4T144I	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMX0640C-3M132I	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMX0640C-4M132I	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMX0640C-3B256I	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	IND
LCMX0640C-4B256I	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	IND
LCMX0640C-3FT256I	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	IND
LCMX0640C-4FT256I	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMX01200C-3T100I	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMX01200C-4T100I	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMX01200C-3T144I	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMX01200C-4T144I	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMX01200C-3M132I	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMX01200C-4M132I	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMX01200C-3B256I	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMX01200C-4B256I	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMX01200C-3FT256I	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMX01200C-4FT256I	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMX02280C-3T100I	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMX02280C-4T100I	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMX02280C-3T144I	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMX02280C-4T144I	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMX02280C-3M132I	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMX02280C-4M132I	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMX02280C-3B256I	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMX02280C-4B256I	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMX02280C-3FT256I	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMX02280C-4FT256I	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND
LCMX02280C-3FT324I	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	IND
LCMX02280C-4FT324I	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100C	1200	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200E-4TN100C	1200	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200E-5TN100C	1200	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200E-3TN144C	1200	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200E-4TN144C	1200	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200E-5TN144C	1200	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200E-3MN132C	1200	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200E-4MN132C	1200	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200E-5MN132C	1200	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200E-3BN256C	1200	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200E-4BN256C	1200	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200E-5BN256C	1200	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200E-3FTN256C	1200	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200E-4FTN256C	1200	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200E-5FTN256C	1200	1.2V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100C	2280	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280E-4TN100C	2280	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280E-5TN100C	2280	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280E-3TN144C	2280	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO2280E-4TN144C	2280	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO2280E-5TN144C	2280	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO2280E-3MN132C	2280	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280E-4MN132C	2280	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280E-5MN132C	2280	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280E-3BN256C	2280	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280E-4BN256C	2280	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280E-5BN256C	2280	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280E-3FTN256C	2280	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280E-4FTN256C	2280	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280E-5FTN256C	2280	1.2V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280E-3FTN324C	2280	1.2V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280E-4FTN324C	2280	1.2V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280E-5FTN324C	2280	1.2V	271	-5	Lead-Free ftBGA	324	COM