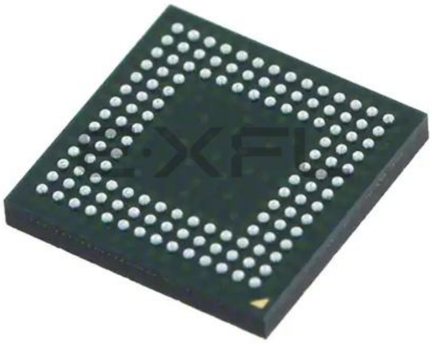
Lattice Semiconductor Corporation - LCMXO1200C-3M132I Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	150
Number of Logic Elements/Cells	1200
Total RAM Bits	9421
Number of I/O	101
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200c-3m132i

MachXO Family Data Sheet
Architecture

June 2013 **Data Sheet DS1002**

Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

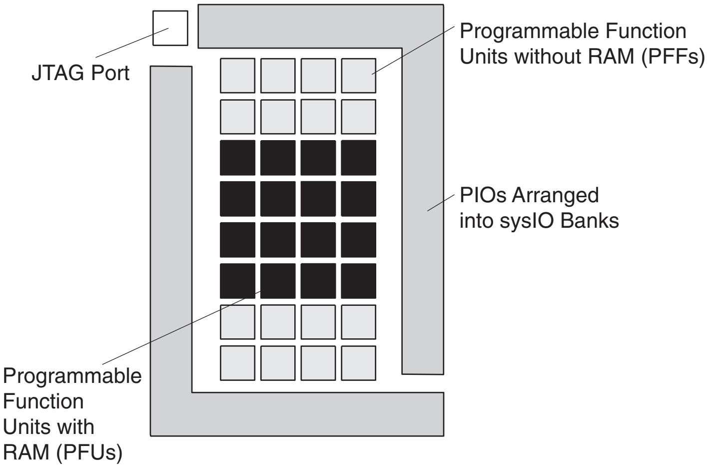
In the MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT use.

The MachXO registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

Figure 2-3. Top View of the MachXO256 Device

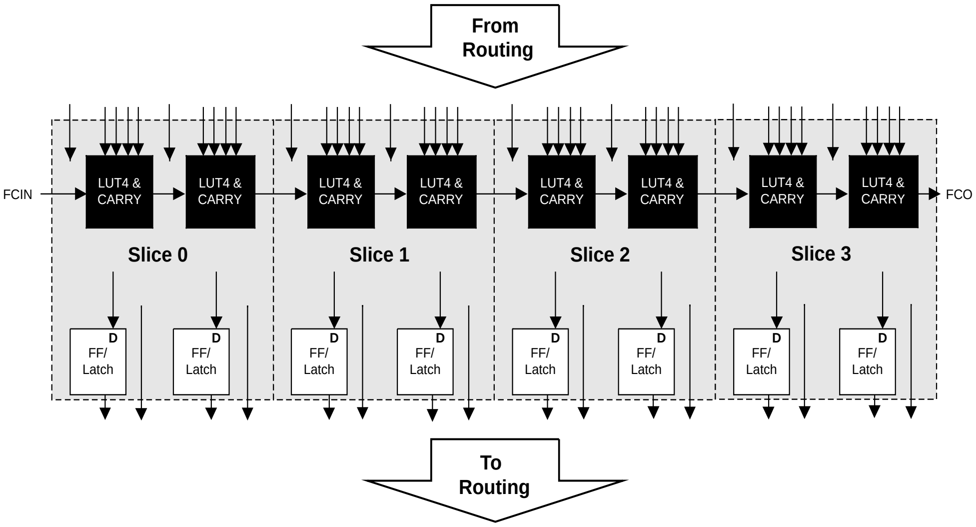


PFU Blocks

The core of the MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected Slices, numbered 0-3 as shown in Figure 2-4. There are 53 inputs and 25 outputs associated with each PFU block.

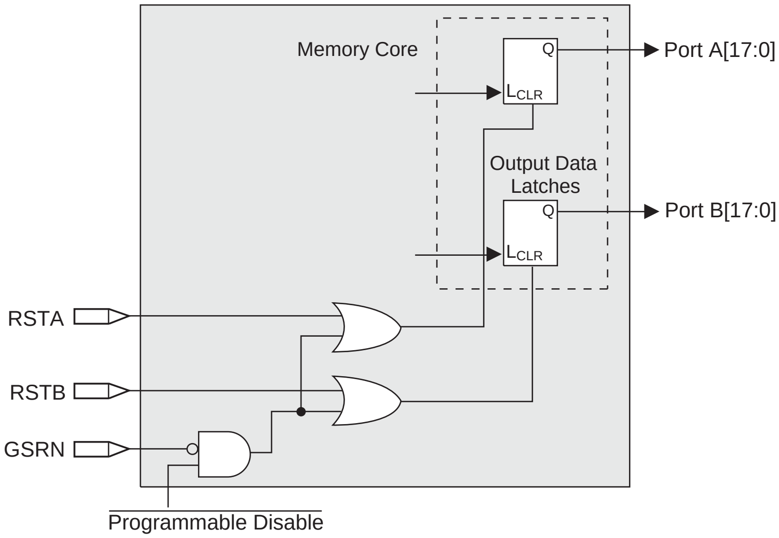
Figure 2-4. PFU Diagram



Slice

Each Slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 2-5 shows an overview of the internal logic of the Slice. The registers in the Slice can be configured for positive/negative and edge/level clocks.

Figure 2-13. Memory Core Reset

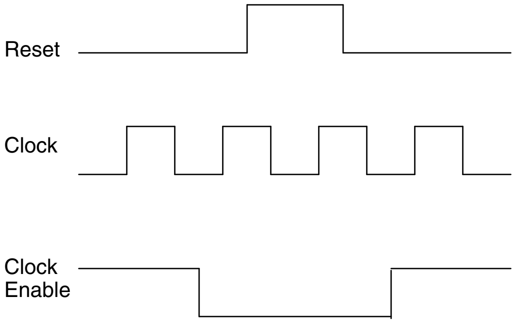


For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPReset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled

PIO Groups

On the MachXO devices, PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four IOs are placed on the left and right sides of the device while PIO groups with six IOs are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and PADs.

On all MachXO devices, two adjacent PIOs can be joined to provide a complementary Output driver pair. The I/O pin pairs are labeled as "T" and "C" to distinguish between the true and complement pins.

The MachXO1200 and MachXO2280 devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. In addition, half of the PIO pairs on the left and right sides of these devices can be configured as LVDS transmit/receive pairs. PIOs on the top of these larger devices also provide PCI support.

Figure 2-15. Group of Four Programmable I/O Cells

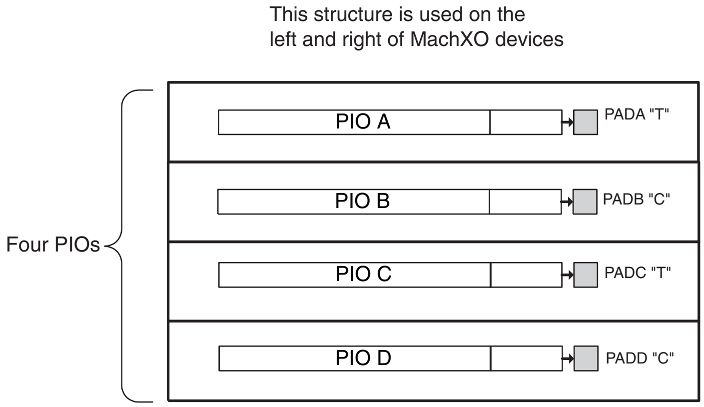
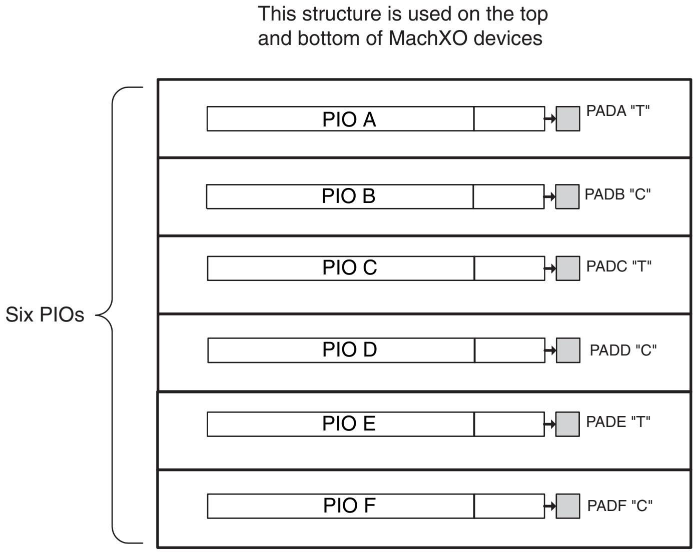


Figure 2-16. Group ofþSix Programmable I/O Cells



PIO

The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The MachXO "C" devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

Table 2-11. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <10mA	0	Typical <100uA
I/O Leakage	<10µA	<1mA	<10µA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1}; MachXO640: V_{CCIO2}; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-22 provides a pictorial representation of the different programming modes available in the MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

Leave Alone I/O

When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

Security

The MachXO devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

MachXO256 and MachXO640 Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX}, and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) and $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

MachXO1200 and MachXO2280 Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Non-LVDS General Purpose sysIOs						
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX.)	—	—	+/-1000	µA
LVDS General Purpose sysIOs						
I_{DK_LVDS}	Input or I/O Leakage Current	$V_{IN} \leq V_{CCIO}$	—	—	+/-1000	µA
		$V_{IN} > V_{CCIO}$	—	35	—	mA

1. Insensitive to sequence of V_{CC}, V_{CCAUX}, and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX), and $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4, 5]	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7\ V_{CCIO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}[3]	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Not applicable to SLEEPN pin.
5. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For MachXO1200 and MachXO2280 true LVDS output pins, V_{IH} must be less than or equal to V_{CCIO}.

Supply Current (Sleep Mode)[1, 2]

Symbol	Parameter	Device	Typ.[3]	Max.	Units
I_{CC}	Core Power Supply	LCMXO256C	12	25	µA
		LCMXO640C	12	25	µA
		LCMXO1200C	12	25	µA
		LCMXO2280C	12	25	µA
I_{CCAUX}	Auxiliary Power Supply	LCMXO256C	1	15	µA
		LCMXO640C	1	25	µA
		LCMXO1200C	1	45	µA
		LCMXO2280C	1	85	µA
I_{CCIO}	Bank Power Supply[4]	All LCMXO 'C' Devices	2	30	µA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency = 0MHz.
3. T_A = 25°C, power supplies at nominal voltage.
4. Per Bank.

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	7	mA
		LCMXO640C	9	mA
		LCMXO1200C	14	mA
		LCMXO2280C	20	mA
		LCMXO256E	4	mA
		LCMXO640E	6	mA
		LCMXO1200E	10	mA
		LCMXO2280E	12	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LCMXO256E/C	5	mA
		LCMXO640E/C	7	mA
		LCMXO1200E/C	12	mA
		LCMXO2280E/C	13	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND.
3. Frequency = 0MHz.
4. User pattern = blank.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.7	ns
4:1 MUX	4.5	ns
16:1 MUX	5.1	ns

Register-to-Register Performance

Function	-5 Timing	Units
Basic Functions		
16:1 MUX	487	MHz
16-bit adder	292	MHz
16-bit counter	388	MHz
64-bit counter	200	MHz
Embedded Memory Functions (1200 and 2280 Devices Only)		
256x36 Single Port RAM	284	MHz
512x18 True-Dual Port RAM	284	MHz
Distributed Memory Functions		
16x2 Single Port RAM	434	MHz
64x2 Single Port RAM	320	MHz
128x4 Single Port RAM	261	MHz
32x2 Pseudo-Dual Port RAM	314	MHz
64x4 Pseudo-Dual Port RAM	271	MHz

1. The above timing numbers are generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Rev. A 0.19

Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays may be much faster. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

Pin Information Summary

Pin Type		LCMXO256C/E		LCMXO640C/E				
		100 TQFP	**100 csBGA**	**100 TQFP**	**144 TQFP**	**100 csBGA**	**132 csBGA**	**256 caBGA / 256 ftBGA**
Single Ended User I/O		78	78	74	113	74	101	159
Differential Pair User I/O[1]		38	38	17	43	17	42	79
Muxed		6	6	6	6	6	6	6
TAP		4	4	4	4	4	4	4
Dedicated (Total Without Supplies)		5	5	5	5	5	5	5
VCC		2	2	2	4	2	4	4
VCCAUX		1	1	1	2	1	2	2
VCCIO	Bank0	3	3	2	2	2	2	4
	Bank1	3	3	2	2	2	2	4
	Bank2	—	—	2	2	2	2	4
	Bank3	—	—	2	2	2	2	4
GND		8	8	10	12	10	12	18
NC		0	0	0	0	0	0	52
Single Ended/Differential I/O per Bank	Bank0	41/20	41/20	18/5	29/10	18/5	26/11	42/21
	Bank1	37/18	37/18	21/4	30/11	21/4	27/12	40/20
	Bank2	—	—	14/2	24/9	14/2	21/9	36/18
	Bank3	—	—	21/6	30/13	21/6	27/10	40/20

1. These devices support emulated LVDS outputs.þLVDS inputs are not supported.

Pin Type		LCMXO1200C/E				LCMXO2280C/E				
		100 TQFP	**144 TQFP**	**132 csBGA**	**256 caBGA / 256 ftBGA**	**100 TQFP**	**144 TQFP**	**132 csBGA**	**256 caBGA / 256 ftBGA**	**324 ftBGA**
Single Ended User I/O		73	113	101	211	73	113	101	211	271
Differential Pair User I/O[1]		27	48	42	105	30	47	41	105	134
Muxed		6	6	6	6	6	6	6	6	6
TAP		4	4	4	4	4	4	4	4	4
Dedicated (Total Without Supplies)		5	5	5	5	5	5	5	5	5
VCC		4	4	4	4	2	4	4	4	6
VCCAUX		2	2	2	2	2	2	2	2	2
VCCIO	Bank0	1	1	1	2	1	1	1	2	2
	Bank1	1	1	1	2	1	1	1	2	2
	Bank2	1	1	1	2	1	1	1	2	2
	Bank3	1	1	1	2	1	1	1	2	2
	Bank4	1	1	1	2	1	1	1	2	2
	Bank5	1	1	1	2	1	1	1	2	2
	Bank6	1	1	1	2	1	1	1	2	2
	Bank7	1	1	1	2	1	1	1	2	2
GND		8	12	12	18	8	12	12	18	24
NC		0	0	0	0	0	0	0	0	0
Single Ended/Differential I/O per Bank	Bank0	10/3	14/6	13/5	26/13	9/3	13/6	12/5	24/12	34/17
	Bank1	8/2	15/7	13/5	28/14	9/3	16/7	14/5	30/15	36/18
	Bank2	10/4	15/7	13/6	26/13	10/4	15/7	13/6	26/13	34/17
	Bank3	11/5	15/7	14/7	28/14	11/5	15/7	14/7	28/14	34/17
	Bank4	8/3	14/5	13/5	27/13	8/3	14/4	13/4	29/14	35/17
	Bank5	5/2	10/4	8/2	22/11	5/2	10/4	8/2	20/10	30/15
	Bank6	10/3	15/6	13/6	28/14	10/4	15/6	13/6	28/14	34/17
	Bank7	11/5	15/6	14/6	26/13	11/5	15/6	14/6	26/13	34/17

1. These devices support on-chip LVDS buffers for left and right I/O Banks.

LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
43	PB4A	1		T	PB8B	2		
44	PB4B	1		C	PB8C	2		T
45	PB4C	1		T	PB8D	2		C
46	PB4D	1		C	PB9A	2		
47	PB5A	1			PB9C	2		T
48*	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
49	PB5C	1		T	PB9D	2		C
50	PB5D	1		C	PB9F	2		
51	PR9B	0		C	PR11D	1		C
52	PR9A	0		T	PR11B	1		C
53	PR8B	0		C	PR11C	1		T
54	PR8A	0		T	PR11A	1		T
55	PR7D	0		C	PR10D	1		C
56	PR7C	0		T	PR10C	1		T
57	PR7B	0		C	PR10B	1		C
58	PR7A	0		T	PR10A	1		T
59	PR6B	0		C	PR9D	1		
60	VCCIO0	0			VCCIO1	1		
61	PR6A	0		T	PR9B	1		
62	GNDIO0	0			GNDIO1	1		
63	PR5D	0		C	PR7B	1		
64	PR5C	0		T	PR6C	1		
65	PR5B	0		C	PR6B	1		
66	PR5A	0		T	PR5D	1		
67	PR4B	0		C	PR5B	1		
68	PR4A	0		T	PR4D	1		
69	PR3D	0		C	PR4B	1		
70	PR3C	0		T	PR3D	1		
71	PR3B	0		C	PR3B	1		
72	PR3A	0		T	PR2D	1		
73	PR2B	0		C	PR2B	1		
74	VCCIO0	0			VCCIO1	1		
75	GNDIO0	0			GNDIO1	1		
76	PR2A	0		T	PT9F	0		C
77	PT5C	0			PT9E	0		T
78	PT5B	0		C	PT9C	0		
79	PT5A	0		T	PT9A	0		
80	PT4F	0		C	VCCIO0	0		
81	PT4E	0		T	GNDIO0	0		
82	PT4D	0		C	PT7E	0		
83	PT4C	0		T	PT7A	0		
84	GND	-			GND	-		

LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for “E” devices.

** Primary clock inputs are single-ended.

LCMXO1200 and LCMXO2280 Logic Signal Connections: 100 TQFP

Pin Number	LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
4	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
5	PL4B	7			PL4B	7		
6	VCCIO7	7			VCCIO7	7		
7	PL6A	7		T*	PL7A	7		T*
8	PL6B	7	GSRN	C*	PL7B	7	GSRN	C*
9	GND	-			GND	-		
10	PL7C	7		T	PL9C	7		T
11	PL7D	7		C	PL9D	7		C
12	PL8C	7		T	PL10C	7		T
13	PL8D	7		C	PL10D	7		C
14	PL9C	6			PL11C	6		
15	PL10A	6		T*	PL13A	6		T*
16	PL10B	6		C*	PL13B	6		C*
17	VCC	-			VCC	-		
18	PL11B	6			PL14D	6		C
19	PL11C	6	TSALL		PL14C	6	TSALL	T
20	VCCIO6	6			VCCIO6	6		
21	PL13C	6			PL16C	6		
22	PL14A	6	LLM0_PLLT_FB_A	T*	PL17A	6	LLM0_PLLT_FB_A	T*
23	PL14B	6	LLM0_PLLC_FB_A	C*	PL17B	6	LLM0_PLLC_FB_A	C*
24	PL15A	6	LLM0_PLLT_IN_A	T*	PL18A	6	LLM0_PLLT_IN_A	T*
25	PL15B	6	LLM0_PLLC_IN_A	C*	PL18B	6	LLM0_PLLC_IN_A	C*
26**	GNDIO6 GNDIO5	-			GNDIO6 GNDIO5	-		
27	VCCIO5	5			VCCIO5	5		
28	TMS	5	TMS		TMS	5	TMS	
29	TCK	5	TCK		TCK	5	TCK	
30	PB3B	5			PB3B	5		
31	PB4A	5		T	PB4A	5		T
32	PB4B	5		C	PB4B	5		C
33	TDO	5	TDO		TDO	5	TDO	
34	TDI	5	TDI		TDI	5	TDI	
35	VCC	-			VCC	-		
36	VCCAUX	-			VCCAUX	-		
37	PB6E	5		T	PB8E	5		T
38	PB6F	5		C	PB8F	5		C
39	PB7B	4	PCLK4_1****		PB10F	4	PCLK4_1****	
40	PB7F	4	PCLK4_0****		PB10B	4	PCLK4_0****	
41	GND	-			GND	-		

LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA

LCMXO256					LCMXO640				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differen-tial**	**Ball Number**	**Ball Function**	**Bank**	**Dual Function**	**Differen-tial**
B1	PL2A	1		T	B1	PL2A	3		T
C1	PL2B	1		C	C1	PL2C	3		T
D2	PL3A	1		T	D2	PL2B	3		C
D1	PL3B	1		C	D1	PL2D	3		C
C2	PL3C	1		T	C2	PL3A	3		T
E1	PL3D	1		C	E1	PL3B	3		C
E2	PL4A	1		T	E2	PL3C	3		T
F1	PL4B	1		C	F1	PL3D	3		C
F2	PL5A	1		T	F2	PL4A	3		
G2	PL5B	1		C	G2	PL4C	3		T
H1	GNDIO1	1			H1	GNDIO3	3		
H2	PL5C	1		T	H2	PL4D	3		C
J1	PL5D	1	GSRN	C	J1	PL5B	3	GSRN	
J2	PL6A	1		T	J2	PL7B	3		
K1	PL6B	1	TSALL	C	K1	PL8C	3	TSALL	T
K2	PL7A	1		T	K2	PL8D	3		C
L1	PL7B	1		C	L1	PL9A	3		
L2	PL7C	1		T	L2	PL9C	3		
M1	PL7D	1		C	M1	PL10A	3		
M2	PL8A	1		T	M2	PL10C	3		
N1	PL8B	1		C	N1	PL11A	3		
M3	PL9A	1		T	M3	PL11C	3		
N2	GNDIO1	1			N2	GNDIO3	3		
P2	TMS	1	TMS		P2	TMS	2	TMS	
P3	PL9B	1		C	P3	PB2C	2		
N4	TCK	1	TCK		N4	TCK	2	TCK	
P4	PB2A	1		T	P4	VCCIO2	2		
N3	PB2B	1		C	N3	GNDIO2	2		
P5	TDO	1	TDO		P5	TDO	2	TDO	
N5	PB2C	1		T	N5	PB4C	2		
P6	TDI	1	TDI		P6	TDI	2	TDI	
N6	PB2D	1		C	N6	PB4E	2		
P7	VCC	-			P7	VCC	-		
N7	PB3A	1	PCLK1_1**	T	N7	PB5B	2	PCLK2_1**	
P8	PB3B	1		C	P8	PB5D	2		
N8	PB3C	1	PCLK1_0**	T	N8	PB6B	2	PCLK2_0**	
P9	PB3D	1		C	P9	PB6C	2		
N10	GNDIO1	1			N10	GNDIO2	2		
P11	PB4A	1		T	P11	PB8B	2		
N11	PB4B	1		C	N11	PB8C	2		T
P12	PB4C	1		T	P12	PB8D	2		C
N12	PB4D	1		C	N12	PB9A	2		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T
A3	PT2B	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2A	0		T	A2	PT3A	0		T	A2	PT3A	0		T
B3	NC				B3	PT2B	0		C	B3	PT2D	0		C
B2	NC				B2	PT2A	0		T	B2	PT2C	0		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A16	GND	-			A16	GND	-			A16	GND	-		
F11	GND	-			F11	GND	-			F11	GND	-		
G8	GND	-			G8	GND	-			G8	GND	-		
G9	GND	-			G9	GND	-			G9	GND	-		
H7	GND	-			H7	GND	-			H7	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
H9	GND	-			H9	GND	-			H9	GND	-		
H10	GND	-			H10	GND	-			H10	GND	-		
J7	GND	-			J7	GND	-			J7	GND	-		
J8	GND	-			J8	GND	-			J8	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
K8	GND	-			K8	GND	-			K8	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L6	GND	-			L6	GND	-			L6	GND	-		
T1	GND	-			T1	GND	-			T1	GND	-		
T16	GND	-			T16	GND	-			T16	GND	-		
G7	VCC	-			G7	VCC	-			G7	VCC	-		
G10	VCC	-			G10	VCC	-			G10	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
K10	VCC	-			K10	VCC	-			K10	VCC	-		
H6	VCCIO3	3			H6	VCCIO7	7			H6	VCCIO7	7		
G6	VCCIO3	3			G6	VCCIO7	7			G6	VCCIO7	7		
K6	VCCIO3	3			K6	VCCIO6	6			K6	VCCIO6	6		
J6	VCCIO3	3			J6	VCCIO6	6			J6	VCCIO6	6		
L8	VCCIO2	2			L8	VCCIO5	5			L8	VCCIO5	5		
L7	VCCIO2	2			L7	VCCIO5	5			L7	VCCIO5	5		
L9	VCCIO2	2			L9	VCCIO4	4			L9	VCCIO4	4		
L10	VCCIO2	2			L10	VCCIO4	4			L10	VCCIO4	4		
K11	VCCIO1	1			K11	VCCIO3	3			K11	VCCIO3	3		
J11	VCCIO1	1			J11	VCCIO3	3			J11	VCCIO3	3		
H11	VCCIO1	1			H11	VCCIO2	2			H11	VCCIO2	2		
G11	VCCIO1	1			G11	VCCIO2	2			G11	VCCIO2	2		
F9	VCCIO0	0			F9	VCCIO1	1			F9	VCCIO1	1		
F10	VCCIO0	0			F10	VCCIO1	1			F10	VCCIO1	1		
F8	VCCIO0	0			F8	VCCIO0	0			F8	VCCIO0	0		
F7	VCCIO0	0			F7	VCCIO0	0			F7	VCCIO0	0		

* Supports true LVDS outputs.
** NC for "E" devices.
*** Primary clock inputs are single-ended.

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
GND	GNDIO3	3		
VCCIO3	VCCIO3	3		
P15	PR20B	3		C
N14	PR20A	3		T
N15	PR19B	3		C
M13	PR19A	3		T
R15	PR18B	3		C*
T16	PR18A	3		T*
N16	PR17D	3		C
M14	PR17C	3		T
U17	PR17B	3		C*
VCC	VCC	-		
U18	PR17A	3		T*
R17	PR16D	3		C
R16	PR16C	3		T
P16	PR16B	3		C*
VCCIO3	VCCIO3	3		
GND	GNDIO3	3		
P17	PR16A	3		T*
L13	PR15D	3		C
M15	PR15C	3		T
T17	PR15B	3		C*
T18	PR15A	3		T*
L14	PR14D	3		C
L15	PR14C	3		T
R18	PR14B	3		C*
P18	PR14A	3		T*
GND	GND	-		
K15	PR13D	3		C
K13	PR13C	3		T
N17	PR13B	3		C*
N18	PR13A	3		T*
K16	PR12D	3		C
K14	PR12C	3		T
M16	PR12B	3		C*
L16	PR12A	3		T*
GND	GNDIO3	3		
VCCIO3	VCCIO3	3		
J16	PR11D	3		C
J14	PR11C	3		T
M17	PR11B	3		C*
L17	PR11A	3		T*
J15	PR10D	2		C

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
E13	PT16D	1		C
C15	PT16C	1		T
F13	PT16B	1		C
D14	PT16A	1		T
A18	PT15D	1		C
B17	PT15C	1		T
A16	PT15B	1		C
A17	PT15A	1		T
VCC	VCC	-		
D13	PT14D	1		C
F12	PT14C	1		T
C14	PT14B	1		C
E12	PT14A	1		T
C13	PT13D	1		C
B16	PT13C	1		T
B15	PT13B	1		C
A15	PT13A	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
B14	PT12F	1		C
A14	PT12E	1		T
D12	PT12D	1		C
F11	PT12C	1		T
B13	PT12B	1		C
A13	PT12A	1		T
C12	PT11D	1		C
GND	GND	-		
B12	PT11C	1		T
E11	PT11B	1		C
D11	PT11A	1		T
C11	PT10F	1		C
A12	PT10E	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
F10	PT10D	1		C
D10	PT10C	1		T
B11	PT10B	1	PCLK1_1***	C
A11	PT10A	1		T
E10	PT9D	1		C
C10	PT9C	1		T
D9	PT9B	1	PCLK1_0***	C
E9	PT9A	1		T
B10	PT8F	0		C

Conventional Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM
LCMXO256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM
LCMXO256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM
LCMXO256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM
LCMXO256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM
LCMXO256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMXO640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMXO640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMXO640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMXO640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMXO640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMXO640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMXO640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMXO640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMXO640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMXO640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMXO640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMXO1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMXO1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMXO1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMXO1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMXO1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMXO1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMXO1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMXO1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100C	1200	1.2V	73	-3	TQFP	100	COM
LCMXO1200E-4T100C	1200	1.2V	73	-4	TQFP	100	COM
LCMXO1200E-5T100C	1200	1.2V	73	-5	TQFP	100	COM
LCMXO1200E-3T144C	1200	1.2V	113	-3	TQFP	144	COM
LCMXO1200E-4T144C	1200	1.2V	113	-4	TQFP	144	COM
LCMXO1200E-5T144C	1200	1.2V	113	-5	TQFP	144	COM
LCMXO1200E-3M132C	1200	1.2V	101	-3	csBGA	132	COM
LCMXO1200E-4M132C	1200	1.2V	101	-4	csBGA	132	COM
LCMXO1200E-5M132C	1200	1.2V	101	-5	csBGA	132	COM
LCMXO1200E-3B256C	1200	1.2V	211	-3	caBGA	256	COM
LCMXO1200E-4B256C	1200	1.2V	211	-4	caBGA	256	COM
LCMXO1200E-5B256C	1200	1.2V	211	-5	caBGA	256	COM
LCMXO1200E-3FT256C	1200	1.2V	211	-3	ftBGA	256	COM
LCMXO1200E-4FT256C	1200	1.2V	211	-4	ftBGA	256	COM
LCMXO1200E-5FT256C	1200	1.2V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100C	2280	1.2V	73	-3	TQFP	100	COM
LCMXO2280E-4T100C	2280	1.2V	73	-4	TQFP	100	COM
LCMXO2280E-5T100C	2280	1.2V	73	-5	TQFP	100	COM
LCMXO2280E-3T144C	2280	1.2V	113	-3	TQFP	144	COM
LCMXO2280E-4T144C	2280	1.2V	113	-4	TQFP	144	COM
LCMXO2280E-5T144C	2280	1.2V	113	-5	TQFP	144	COM
LCMXO2280E-3M132C	2280	1.2V	101	-3	csBGA	132	COM
LCMXO2280E-4M132C	2280	1.2V	101	-4	csBGA	132	COM
LCMXO2280E-5M132C	2280	1.2V	101	-5	csBGA	132	COM
LCMXO2280E-3B256C	2280	1.2V	211	-3	caBGA	256	COM
LCMXO2280E-4B256C	2280	1.2V	211	-4	caBGA	256	COM
LCMXO2280E-5B256C	2280	1.2V	211	-5	caBGA	256	COM
LCMXO2280E-3FT256C	2280	1.2V	211	-3	ftBGA	256	COM
LCMXO2280E-4FT256C	2280	1.2V	211	-4	ftBGA	256	COM
LCMXO2280E-5FT256C	2280	1.2V	211	-5	ftBGA	256	COM
LCMXO2280E-3FT324C	2280	1.2V	271	-3	ftBGA	324	COM
LCMXO2280E-4FT324C	2280	1.2V	271	-4	ftBGA	324	COM
LCMXO2280E-5FT324C	2280	1.2V	271	-5	ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3T100I	256	1.2V	78	-3	TQFP	100	IND
LCMXO256E-4T100I	256	1.2V	78	-4	TQFP	100	IND
LCMXO256E-3M100I	256	1.2V	78	-3	csBGA	100	IND
LCMXO256E-4M100I	256	1.2V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3T100I	640	1.2V	74	-3	TQFP	100	IND
LCMXO640E-4T100I	640	1.2V	74	-4	TQFP	100	IND
LCMXO640E-3M100I	640	1.2V	74	-3	csBGA	100	IND
LCMXO640E-4M100I	640	1.2V	74	-4	csBGA	100	IND
LCMXO640E-3T144I	640	1.2V	113	-3	TQFP	144	IND
LCMXO640E-4T144I	640	1.2V	113	-4	TQFP	144	IND
LCMXO640E-3M132I	640	1.2V	101	-3	csBGA	132	IND
LCMXO640E-4M132I	640	1.2V	101	-4	csBGA	132	IND
LCMXO640E-3B256I	640	1.2V	159	-3	caBGA	256	IND
LCMXO640E-4B256I	640	1.2V	159	-4	caBGA	256	IND
LCMXO640E-3FT256I	640	1.2V	159	-3	ftBGA	256	IND
LCMXO640E-4FT256I	640	1.2V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100I	1200	1.2V	73	-3	TQFP	100	IND
LCMXO1200E-4T100I	1200	1.2V	73	-4	TQFP	100	IND
LCMXO1200E-3T144I	1200	1.2V	113	-3	TQFP	144	IND
LCMXO1200E-4T144I	1200	1.2V	113	-4	TQFP	144	IND
LCMXO1200E-3M132I	1200	1.2V	101	-3	csBGA	132	IND
LCMXO1200E-4M132I	1200	1.2V	101	-4	csBGA	132	IND
LCMXO1200E-3B256I	1200	1.2V	211	-3	caBGA	256	IND
LCMXO1200E-4B256I	1200	1.2V	211	-4	caBGA	256	IND
LCMXO1200E-3FT256I	1200	1.2V	211	-3	ftBGA	256	IND
LCMXO1200E-4FT256I	1200	1.2V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100I	2280	1.2V	73	-3	TQFP	100	IND
LCMXO2280E-4T100I	2280	1.2V	73	-4	TQFP	100	IND
LCMXO2280E-3T144I	2280	1.2V	113	-3	TQFP	144	IND
LCMXO2280E-4T144I	2280	1.2V	113	-4	TQFP	144	IND
LCMXO2280E-3M132I	2280	1.2V	101	-3	csBGA	132	IND
LCMXO2280E-4M132I	2280	1.2V	101	-4	csBGA	132	IND
LCMXO2280E-3B256I	2280	1.2V	211	-3	caBGA	256	IND
LCMXO2280E-4B256I	2280	1.2V	211	-4	caBGA	256	IND
LCMXO2280E-3FT256I	2280	1.2V	211	-3	ftBGA	256	IND
LCMXO2280E-4FT256I	2280	1.2V	211	-4	ftBGA	256	IND
LCMXO2280E-3FT324I	2280	1.2V	271	-3	ftBGA	324	IND
LCMXO2280E-4FT324I	2280	1.2V	271	-4	ftBGA	324	IND