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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

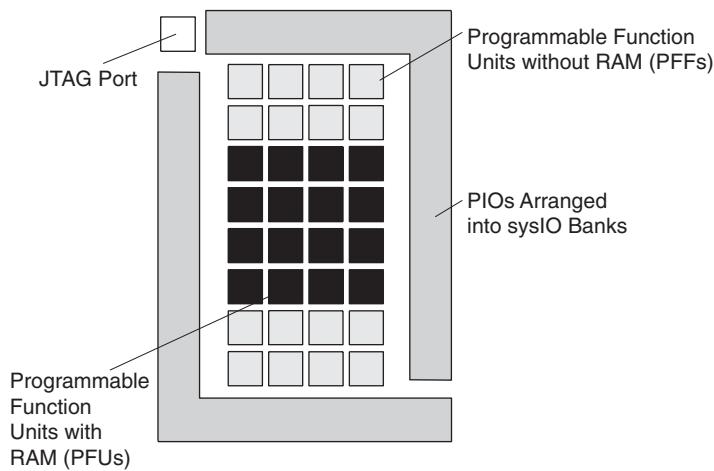
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	150
Number of Logic Elements/Cells	1200
Total RAM Bits	9421
Number of I/O	211
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200c-4ftn256c

Figure 2-3. Top View of the MachXO256 Device

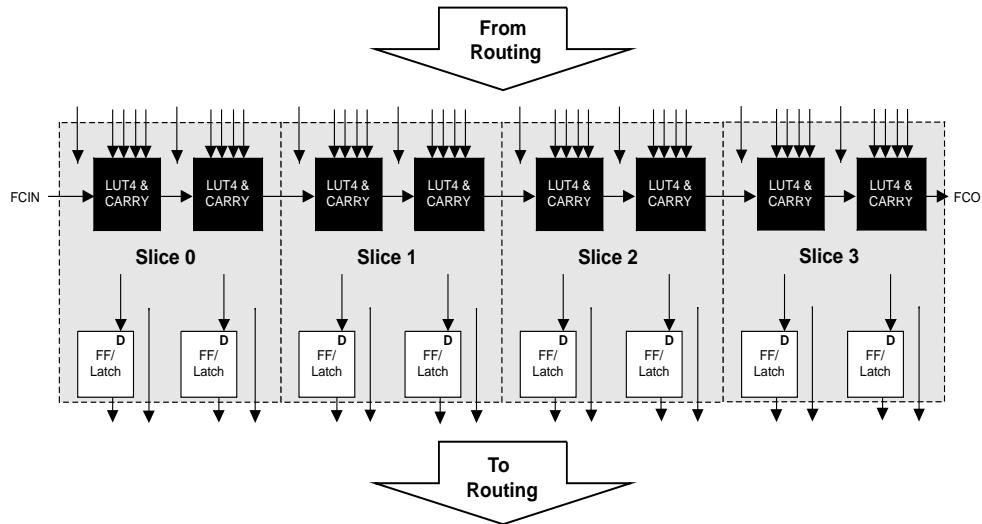


PFU Blocks

The core of the MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected Slices, numbered 0-3 as shown in Figure 2-4. There are 53 inputs and 25 outputs associated with each PFU block.

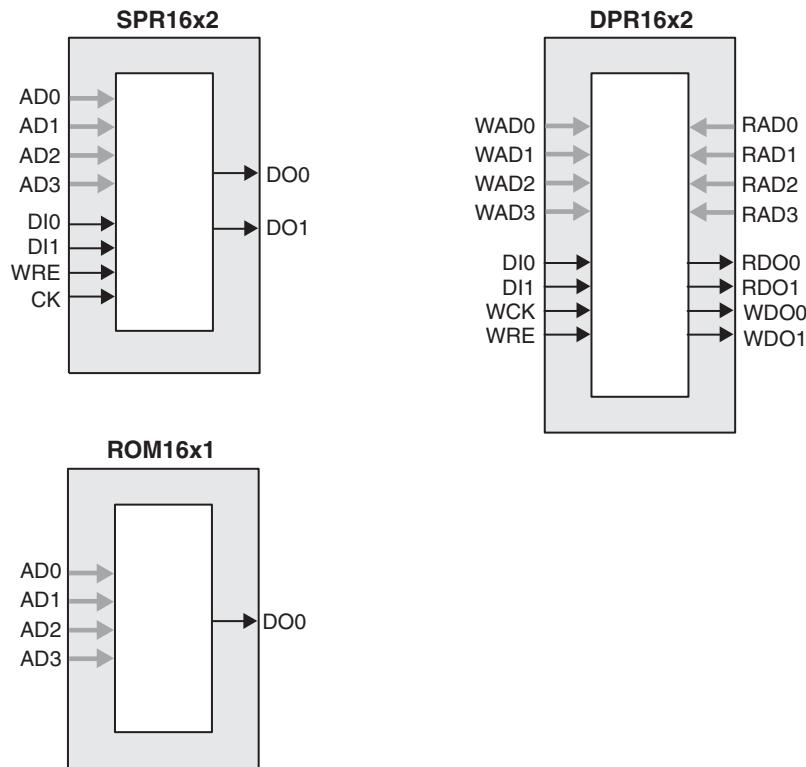
Figure 2-4. PFU Diagram



Slice

Each Slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 2-5 shows an overview of the internal logic of the Slice. The registers in the Slice can be configured for positive/negative and edge/level clocks.

Figure 2-6. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-10. PLL Diagram

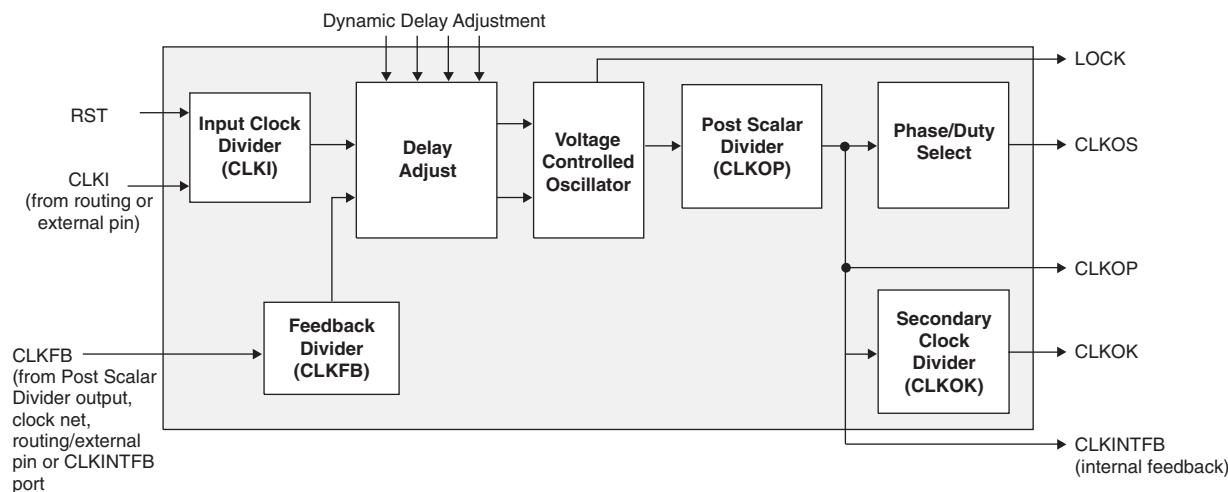
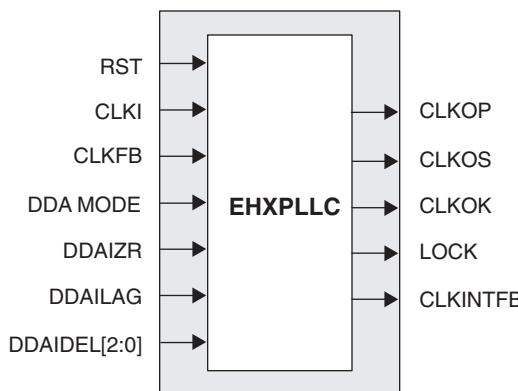


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive



PIO Groups

On the MachXO devices, PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four IOs are placed on the left and right sides of the device while PIO groups with six IOs are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and PADs.

On all MachXO devices, two adjacent PIOs can be joined to provide a complementary Output driver pair. The I/O pin pairs are labeled as "T" and "C" to distinguish between the true and complement pins.

The MachXO1200 and MachXO2280 devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. In addition, half of the PIO pairs on the left and right sides of these devices can be configured as LVDS transmit/receive pairs. PIOs on the top of these larger devices also provide PCI support.

Figure 2-15. Group of Four Programmable I/O Cells

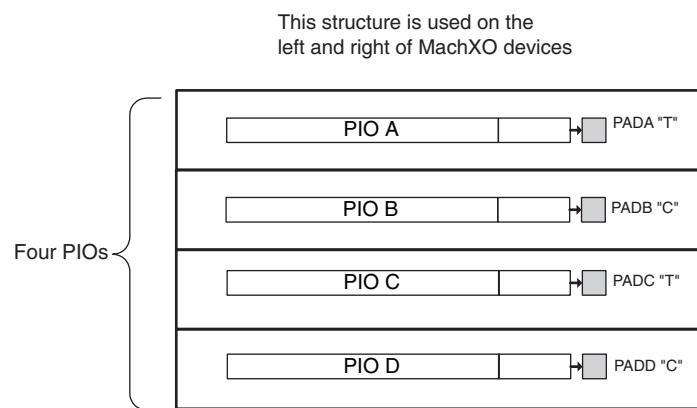
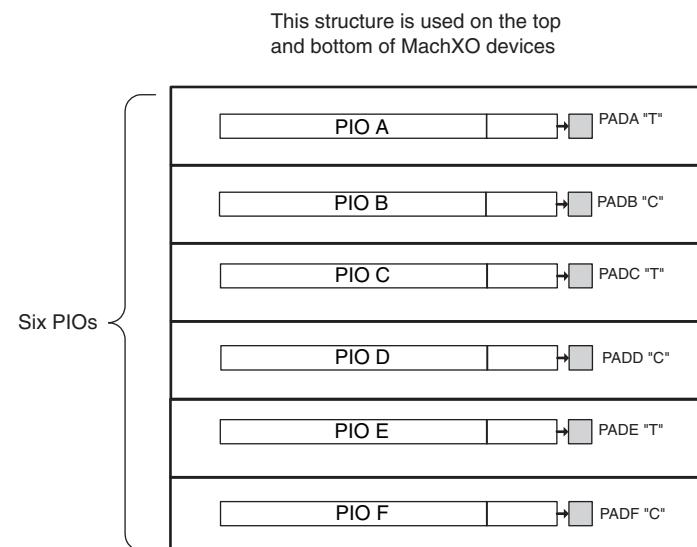


Figure 2-16. Group of Six Programmable I/O Cells



PIO

The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast

Figure 2-20. MachXO640 Banks

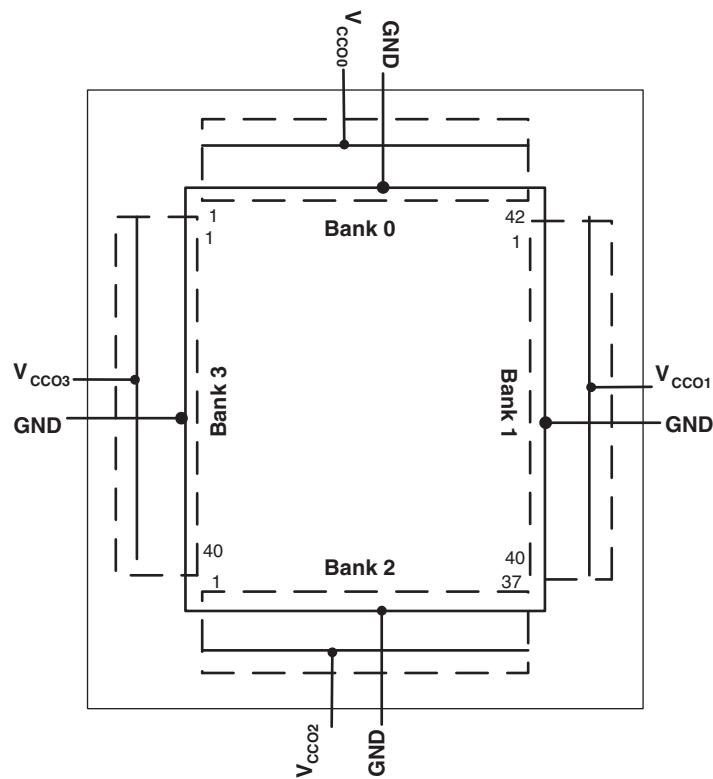
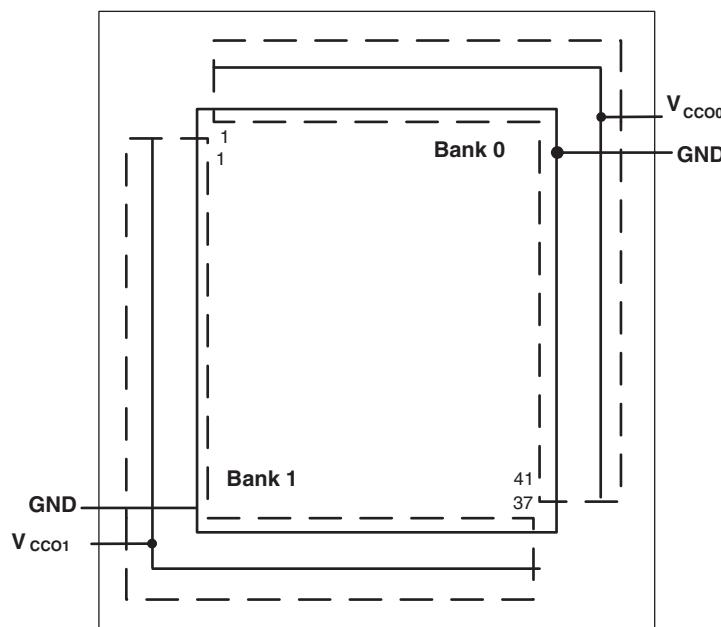


Figure 2-21. MachXO256 Banks



Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of



MachXO Family Data Sheet

DC and Switching Characteristics

June 2013

Data Sheet DS1002

Absolute Maximum Ratings^{1, 2, 3}

	LCMXO E (1.2V)	LCMXO C (1.8V/2.5V/3.3V)
Supply Voltage V _{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V _{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V _{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied ⁴	-0.5 to 3.75V	-0.5 to 3.75V
Dedicated Input Voltage Applied ⁴	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (ambient).....	-65 to 150°C	-65 to 150°C
Junction Temp. (T _j)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V _{CCAUX} ³	Auxiliary Supply Voltage	3.135	3.465	V
V _{CCIO} ²	I/O Driver Supply Voltage	1.14	3.465	V
t _{TJCOM}	Junction Temperature Commercial Operation	0	+85	°C
t _{TJIND}	Junction Temperature Industrial Operation	-40	100	°C
t _{TFLASHCOM}	Junction Temperature, Flash Programming, Commercial	0	+85	°C
t _{TFLASHIND}	Junction Temperature, Flash Programming, Industrial	-40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both 2.5V, they must also be the same supply. 3.3V V_{CCIO} and 1.2V V_{CCIO} should be tied to V_{CCAUX} or 1.2V V_{CC} respectively.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CC} must reach minimum V_{CC} value before V_{CCAUX} reaches 2.5V.

MachXO Programming/Erase Specifications

Symbol	Parameter	Min.	Max.	Units
N _{PROGCYC}	Flash Programming Cycles per t _{RETENTION}		1,000	Cycles
	Flash Functional Programming Cycles		10,000	Cycles
t _{RETENTION}	Data Retention at 125° Junction Temperature	10		Years

Supply Current (Sleep Mode)^{1,2}

Symbol	Parameter	Device	Typ. ³	Max.	Units
I_{CC}	Core Power Supply	LCMxo256C	12	25	μA
		LCMxo640C	12	25	μA
		LCMxo1200C	12	25	μA
		LCMxo2280C	12	25	μA
I_{CCAUX}	Auxiliary Power Supply	LCMxo256C	1	15	μA
		LCMxo640C	1	25	μA
		LCMxo1200C	1	45	μA
		LCMxo2280C	1	85	μA
I_{CCIO}	Bank Power Supply ⁴	All LCMxo 'C' Devices	2	30	μA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.

2. Frequency = 0MHz.

3. $T_A = 25^\circ C$, power supplies at nominal voltage.

4. Per Bank.

Supply Current (Standby)^{1, 2, 3, 4}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMxo256C	7	mA
		LCMxo640C	9	mA
		LCMxo1200C	14	mA
		LCMxo2280C	20	mA
		LCMxo256E	4	mA
		LCMxo640E	6	mA
		LCMxo1200E	10	mA
		LCMxo2280E	12	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LCMxo256E/C	5	mA
		LCMxo640E/C	7	mA
		LCMxo1200E/C	12	mA
		LCMxo2280E/C	13	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND.

3. Frequency = 0MHz.

4. User pattern = blank.

5. $T_J = 25^\circ C$, power supplies at nominal voltage.

6. Per Bank. $V_{CCIO} = 2.5V$. Does not include pull-up/pull-down.

MachXO External Switching Characteristics¹

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Global Clock without PLL)¹									
t _{PD}	Best Case t _{PD} Through 1 LUT	LCMxo256	—	3.5	—	4.2	—	4.9	ns
		LCMxo640	—	3.5	—	4.2	—	4.9	ns
		LCMxo1200	—	3.6	—	4.4	—	5.1	ns
		LCMxo2280	—	3.6	—	4.4	—	5.1	ns
t _{CO}	Best Case Clock to Output - From PFU	LCMxo256	—	4.0	—	4.8	—	5.6	ns
		LCMxo640	—	4.0	—	4.8	—	5.7	ns
		LCMxo1200	—	4.3	—	5.2	—	6.1	ns
		LCMxo2280	—	4.3	—	5.2	—	6.1	ns
t _{SU}	Clock to Data Setup - To PFU	LCMxo256	1.3	—	1.6	—	1.8	—	ns
		LCMxo640	1.1	—	1.3	—	1.5	—	ns
		LCMxo1200	1.1	—	1.3	—	1.6	—	ns
		LCMxo2280	1.1	—	1.3	—	1.5	—	ns
t _H	Clock to Data Hold - To PFU	LCMxo256	-0.3	—	-0.3	—	-0.3	—	ns
		LCMxo640	-0.1	—	-0.1	—	-0.1	—	ns
		LCMxo1200	0.0	—	0.0	—	0.0	—	ns
		LCMxo2280	-0.4	—	-0.4	—	-0.4	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	LCMxo256	—	600	—	550	—	500	MHz
		LCMxo640	—	600	—	550	—	500	MHz
		LCMxo1200	—	600	—	550	—	500	MHz
		LCMxo2280	—	600	—	550	—	500	MHz
t _{SKEW_PRI}	Global Clock Skew Across Device	LCMxo256	—	200	—	220	—	240	ps
		LCMxo640	—	200	—	220	—	240	ps
		LCMxo1200	—	220	—	240	—	260	ps
		LCMxo2280	—	220	—	240	—	260	ps

1. General timing numbers based on LVCMS2.5V, 12 mA.

Rev. A 0.19

Power Supply and NC (Cont.)

Signal	132 csBGA ¹	256 caBGA / 256 ftBGA ¹	324 ftBGA ¹
VCC	H3, P6, G12, C7	G7, G10, K7, K10	F14, G11, G9, H7, L7, M9
VCCIO0	LCMxo640: B11, C5 LCMxo1200/2280: C5	LCMxo640: F8, F7, F9, F10 LCMxo1200/2280: F8, F7	G8, G7
VCCIO1	LCMxo640: L12, E12 LCMxo1200/2280: B11	LCMxo640: H11, G11, K11, J11 LCMxo1200/2280: F9, F10	G12, G10
VCCIO2	LCMxo640: N2, M10 LCMxo1200/2280: E12	LCMxo640: L9, L10, L8, L7 LCMxo1200/2280: H11, G11	J12, H12
VCCIO3	LCMxo640: D2, K3 LCMxo1200/2280: L12	LCMxo640: K6, J6, H6, G6 LCMxo1200/2280: K11, J11	L12, K12
VCCIO4	LCMxo640: None LCMxo1200/2280: M10	LCMxo640: None LCMxo1200/2280: L9, L10	M12, M11
VCCIO5	LCMxo640: None LCMxo1200/2280: N2	LCMxo640: None LCMxo1200/2280: L8, L7	M8, R9
VCCIO6	LCMxo640: None LCMxo1200/2280: K3	LCMxo640: None LCMxo1200/2280: K6, J6	M7, K7
VCCIO7	LCMxo640: None LCMxo1200/2280: D2	LCMxo640: None LCMxo1200/2280: H6, G6	H6, J7
VCCAUX	P7, A7	T9, A8	M10, F9
GND ²	F1, P9, J14, C9, A10, B4, L13, D13, P2, N11, E1, L2	A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16	E14, F16, H10, H11, H8, H9, J10, J11, J4, J8, J9, K10, K11, K17, K8, K9, L10, L11, L8, L9, N2, P14, P5, R7
NC ³	—	LCMxo640: E4, E5, F5, F6, C3, C2, G4, G5, H4, H5, K5, K4, M5, M4, P2, P3, N5, N6, M7, M8, N10, N11, R15, R16, P15, P16, M11, L11, N12, N13, M13, M12, K12, J12, F12, F13, E12, E13, D13, D14, B15, A15, C14, B14, E11, E10, E7, E6, D4, D3, B3, B2 LCMxo1200: None LCMxo2280: None	—

1. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
3. NC pins should not be connected to any active signals, VCC or GND.

LCMxo256 and LCMxo640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMxo256				LCMxo640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for "E" devices.

** Primary clock inputs are single-ended.

**LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections:
 132 csBGA (Cont.)**

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1***	C	A8	PT7D	1	PCLK1_1***		A8	PT10B	1	PCLK1_1***	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0***	C	C8	PT6F	0	PCLK1_0***		C8	PT9B	1	PCLK1_0***	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	-			A7	VCCAUX	-			A7	VCCAUX	-		
C7	VCC	-			C7	VCC	-			C7	VCC	-		
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	-			F1	GND	-			F1	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
C9	GND	-			C9	GND	-			C9	GND	-		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 144 TQFP (Cont.)**

Pin Number	LCMxo640				LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
51	TDI	2	TDI		TDI	5	TDI		TDI	5	TDI	
52	VCC	-			VCC	-			VCC	-		
53	VCCAUX	-			VCCAUX	-			VCCAUX	-		
54	PB5A	2		T	PB6F	5			PB8F	5		
55	PB5B	2	PCLKT2_1***	C	PB7B	4	PCLK4_1***		PB10F	4	PCLK4_1***	
56	PB5D	2			PB7C	4			PB10C	4		T
57	PB6A	2		T	PB7D	4			PB10D	4		C
58	PB6B	2	PCLKT2_0***	C	PB7F	4	PCLK4_0***		PB10B	4	PCLK4_0***	
59	GND	-			GND	-			GND	-		
60	PB7C	2			PB9A	4			PB12A	4		T
61	PB7E	2			PB9B	4			PB12B	4		C
62	PB8A	2			PB9E	4			PB12E	4		
63	VCCIO2	2			VCCIO4	4			VCCIO4	4		
64	GNDIO2	2			GNDIO4	4			GNDIO4	4		
65	PB8C	2		T	PB10A	4			PB13A	4		T
66	PB8D	2		C	PB10B	4			PB13B	4		C
67	PB9A	2		T	PB10C	4			PB13C	4		T
68	PB9C	2		T	PB10D	4			PB13D	4		C
69	PB9B	2		C	PB10F	4			PB14D	4		
70**	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
71	PB9D	2		C	PB11C	4			PB16C	4		T
72	PB9F	2			PB11D	4			PB16D	4		C
73	PR11D	1		C	PR16B	3			PR20B	3		C
74	PR11B	1		C	PR16A	3			PR20A	3		T
75	PR11C	1		T	PR15B	3			PR19B	3		C
76	PR10D	1		C	PR15A	3			PR19A	3		T
77	PR11A	1		T	PR14D	3			PR17D	3		C
78	PR10B	1		C	PR14C	3			PR17C	3		T
79	PR10C	1		T	PR14B	3			PR17B	3		C*
80	PR10A	1		T	PR14A	3			PR17A	3		T*
81	PR9D	1			PR13D	3			PR16D	3		
82	VCCIO1	1			VCCIO3	3			VCCIO3	3		
83	GNDIO1	1			GNDIO3	3			GNDIO3	3		
84	PR9A	1			PR12B	3			PR15B	3		C*
85	PR8C	1			PR12A	3			PR15A	3		T*
86	PR8A	1			PR11B	3			PR14B	3		C*
87	PR7D	1			PR11A	3			PR14A	3		T*
88	GND	-			GND	-			GND	-		
89	PR7B	1		C	PR10B	3			PR13B	3		C*
90	PR7A	1		T	PR10A	3			PR13A	3		T*
91	PR6D	1		C	PR8B	2			PR10B	2		C*
92	PR6C	1		T	PR8A	2			PR10A	2		T*
93	VCC	-			VCC	-			VCC	-		
94	PR5D	1			PR6B	2			PR8B	2		C*
95	PR5B	1			PR6A	2			PR8A	2		T*
96	PR4D	1			PR5B	2			PR7B	2		C*
97	PR4B	1		C	PR5A	2			PR7A	2		T*
98	VCCIO1	1			VCCIO2	2			VCCIO2	2		
99	GNDIO1	1			GNDIO2	2			GNDIO2	2		
100	PR4A	1		T	PR4C	2			PR5C	2		

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
-	-				VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
-	-				GND	GNDIO4	4			GND	GNDIO4	4		
M10	PB6A	2		T	M10	PB7E	4			M10	PB10A	4		T
R9	PB6C	2		T	R9	PB8A	4			R9	PB11C	4		T
R10	PB6D	2		C	R10	PB8B	4			R10	PB11D	4		C
T10	PB7C	2		T	T10	PB8C	4			T10	PB12A	4		T
T11	PB7D	2		C	T11	PB8D	4			T11	PB12B	4		C
N10	NC				N10	PB8E	4			N10	PB12C	4		T
N11	NC				N11	PB8F	4			N11	PB12D	4		C
VCCIO2	VCCIO2	2			VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
GND	GNDIO2	2			GND	GNDIO4	4			GND	GNDIO4	4		
R11	PB7E	2		T	R11	PB9A	4			R11	PB13A	4		T
R12	PB7F	2		C	R12	PB9B	4			R12	PB13B	4		C
P11	PB8A	2		T	P11	PB9C	4			P11	PB13C	4		T
P12	PB8B	2		C	P12	PB9D	4			P12	PB13D	4		C
T13	PB8C	2		T	T13	PB9E	4			T13	PB14A	4		T
T12	PB8D	2		C	T12	PB9F	4			T12	PB14B	4		C
R13	PB9A	2		T	R13	PB10A	4			R13	PB14C	4		T
R14	PB9B	2		C	R14	PB10B	4			R14	PB14D	4		C
GND	GND	-			GND	GND	-			GND	GND	-		
T14	PB9C	2		T	T14	PB10C	4			T14	PB15A	4		T
T15	PB9D	2		C	T15	PB10D	4			T15	PB15B	4		C
P13**	SLEEPN	-	SLEEPN		P13**	SLEEPN	-	SLEEPN		P13**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB10F	4			P14	PB15D	4		
R15	NC				R15	PB11A	4			R15	PB16A	4		T
R16	NC				R16	PB11B	4			R16	PB16B	4		C
P15	NC				P15	PB11C	4			P15	PB16C	4		T
P16	NC				P16	PB11D	4			P16	PB16D	4		C
VCCIO2	VCCIO2	2			VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
GND	GNDIO2	2			GND	GNDIO4	4			GND	GNDIO4	4		
GND	GNDIO1	1			GND	GNDIO3	3			GND	GNDIO3	3		
VCCIO1	VCCIO1	1			VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
M11	NC				M11	PR16B	3			M11	PR20B	3		C
L11	NC				L11	PR16A	3			L11	PR20A	3		T
N12	NC				N12	PR15B	3			N12	PR18B	3		C*
N13	NC				N13	PR15A	3			N13	PR18A	3		T*
M13	NC				M13	PR14D	3			M13	PR17D	3		C
M12	NC				M12	PR14C	3			M12	PR17C	3		T
N14	PR11D	1		C	N14	PR14B	3			N14	PR17B	3		C*
N15	PR11C	1		T	N15	PR14A	3			N15	PR17A	3		T*
L13	PR11B	1		C	L13	PR13D	3			L13	PR16D	3		C
L12	PR11A	1		T	L12	PR13C	3			L12	PR16C	3		T
M14	PR10B	1		C	M14	PR13B	3			M14	PR16B	3		C*
VCCIO1	VCCIO1	1			VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
GND	GNDIO1	1			GND	GNDIO3	3			GND	GNDIO3	3		
L14	PR10A	1		T	L14	PR13A	3			L14	PR16A	3		T*
N16	PR10D	1		C	N16	PR12D	3			N16	PR15D	3		C
M16	PR10C	1		T	M16	PR12C	3			M16	PR15C	3		T
M15	PR9D	1		C	M15	PR12B	3			M15	PR15B	3		C*
L15	PR9C	1		T	L15	PR12A	3			L15	PR15A	3		T*
L16	PR9B	1		C	L16	PR11D	3			L16	PR14D	3		C
K16	PR9A	1		T	K16	PR11C	3			K16	PR14C	3		T
K13	PR8D	1		C	K13	PR11B	3			K13	PR14B	3		C*

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR8C	1		T	J13	PR11A	3			J13	PR14A	3		T*
GND	GND	-			GND	GND	-			GND	GND	-		
K14	PR8B	1		C	K14	PR10D	3			K14	PR13D	3		C
J14	PR8A	1		T	J14	PR10C	3			J14	PR13C	3		T
K15	PR7D	1		C	K15	PR10B	3			K15	PR13B	3		C*
J15	PR7C	1		T	J15	PR10A	3			J15	PR13A	3		T*
-	-				GND	GNDIO3	3			GND	GNDIO3	3		
-	-				VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
K12	NC				K12	PR9D	3			K12	PR11D	3		C
J12	NC				J12	PR9C	3			J12	PR11C	3		T
J16	PR7B	1		C	J16	PR9B	3			J16	PR11B	3		C*
H16	PR7A	1		T	H16	PR9A	3			H16	PR11A	3		T*
H15	PR6B	1		C	H15	PR8D	2			H15	PR10D	2		C
G15	PR6A	1		T	G15	PR8C	2			G15	PR10C	2		T
H14	PR5D	1		C	H14	PR8B	2			H14	PR10B	2		C*
G14	PR5C	1		T	G14	PR8A	2			G14	PR10A	2		T*
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
H13	PR6D	1		C	H13	PR7D	2			H13	PR9D	2		C
H12	PR6C	1		T	H12	PR7C	2			H12	PR9C	2		T
G13	PR4D	1		C	G13	PR7B	2			G13	PR9B	2		C*
G12	PR4C	1		T	G12	PR7A	2			G12	PR9A	2		T*
G16	PR5B	1		C	G16	PR6D	2			G16	PR7D	2		C
F16	PR5A	1		T	F16	PR6C	2			F16	PR7C	2		T
F15	PR4B	1		C	F15	PR6B	2			F15	PR7B	2		C*
E15	PR4A	1		T	E15	PR6A	2			E15	PR7A	2		T*
E16	PR3B	1		C	E16	PR5D	2			E16	PR6D	2		C
D16	PR3A	1		T	D16	PR5C	2			D16	PR6C	2		T
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
D15	PR2D	1		C	D15	PR5B	2			D15	PR6B	2		C*
C15	PR2C	1		T	C15	PR5A	2			C15	PR6A	2		T*
C16	PR2B	1		C	C16	PR4D	2			C16	PR5D	2		C
B16	PR2A	1		T	B16	PR4C	2			B16	PR5C	2		T
F14	PR3D	1		C	F14	PR4B	2			F14	PR5B	2		C*
E14	PR3C	1		T	E14	PR4A	2			E14	PR5A	2		T*
-	-	-			-	-	-			GND	GND	-		
F12	NC				F12	PR3D	2			F12	PR4D	2		C
F13	NC				F13	PR3C	2			F13	PR4C	2		T
E12	NC				E12	PR3B	2			E12	PR4B	2		C*
E13	NC				E13	PR3A	2			E13	PR4A	2		T*
D13	NC				D13	PR2B	2			D13	PR3B	2		C*
D14	NC				D14	PR2A	2			D14	PR3A	2		T*
VCCIO0	VCCIO0	0			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO0	0			GND	GNDIO2	2			GND	GNDIO2	2		
GND	GNDIO0	0			GND	GNDIO1	1			GND	GNDIO1	1		
VCCIO0	VCCIO0	0			VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
B15	NC				B15	PT11D	1			B15	PT16D	1		C
A15	NC				A15	PT11C	1			A15	PT16C	1		T
C14	NC				C14	PT11B	1			C14	PT16B	1		C
B14	NC				B14	PT11A	1			B14	PT16A	1		T
C13	PT9F	0		C	C13	PT10F	1			C13	PT15D	1		C
B13	PT9E	0		T	B13	PT10E	1			B13	PT15C	1		T

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T
A3	PT2B	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2A	0		T	A2	PT3A	0		T	A2	PT3A	0		T
B3	NC				B3	PT2B	0		C	B3	PT2D	0		C
B2	NC				B2	PT2A	0		T	B2	PT2C	0		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A16	GND	-			A16	GND	-			A16	GND	-		
F11	GND	-			F11	GND	-			F11	GND	-		
G8	GND	-			G8	GND	-			G8	GND	-		
G9	GND	-			G9	GND	-			G9	GND	-		
H7	GND	-			H7	GND	-			H7	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
H9	GND	-			H9	GND	-			H9	GND	-		
H10	GND	-			H10	GND	-			H10	GND	-		
J7	GND	-			J7	GND	-			J7	GND	-		
J8	GND	-			J8	GND	-			J8	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
K8	GND	-			K8	GND	-			K8	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L6	GND	-			L6	GND	-			L6	GND	-		
T1	GND	-			T1	GND	-			T1	GND	-		
T16	GND	-			T16	GND	-			T16	GND	-		
G7	VCC	-			G7	VCC	-			G7	VCC	-		
G10	VCC	-			G10	VCC	-			G10	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
K10	VCC	-			K10	VCC	-			K10	VCC	-		
H6	VCCIO3	3			H6	VCCIO7	7			H6	VCCIO7	7		
G6	VCCIO3	3			G6	VCCIO7	7			G6	VCCIO7	7		
K6	VCCIO3	3			K6	VCCIO6	6			K6	VCCIO6	6		
J6	VCCIO3	3			J6	VCCIO6	6			J6	VCCIO6	6		
L8	VCCIO2	2			L8	VCCIO5	5			L8	VCCIO5	5		
L7	VCCIO2	2			L7	VCCIO5	5			L7	VCCIO5	5		
L9	VCCIO2	2			L9	VCCIO4	4			L9	VCCIO4	4		
L10	VCCIO2	2			L10	VCCIO4	4			L10	VCCIO4	4		
K11	VCCIO1	1			K11	VCCIO3	3			K11	VCCIO3	3		
J11	VCCIO1	1			J11	VCCIO3	3			J11	VCCIO3	3		
H11	VCCIO1	1			H11	VCCIO2	2			H11	VCCIO2	2		
G11	VCCIO1	1			G11	VCCIO2	2			G11	VCCIO2	2		
F9	VCCIO0	0			F9	VCCIO1	1			F9	VCCIO1	1		
F10	VCCIO0	0			F10	VCCIO1	1			F10	VCCIO1	1		
F8	VCCIO0	0			F8	VCCIO0	0			F8	VCCIO0	0		
F7	VCCIO0	0			F7	VCCIO0	0			F7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
V10	PB9B	4		C
N10	PB9C	4		T
R10	PB9D	4		C
P10	PB10F	4	PCLK4_1***	C
T10	PB10E	4		T
U10	PB10D	4		C
V11	PB10C	4		T
U11	PB10B	4	PCLK4_0***	C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
T11	PB10A	4		T
U12	PB11A	4		T
R11	PB11B	4		C
GND	GND	-		
T12	PB11C	4		T
P11	PB11D	4		C
V12	PB12A	4		T
V13	PB12B	4		C
R12	PB12C	4		T
N11	PB12D	4		C
U13	PB12E	4		T
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
V14	PB12F	4		C
T13	PB13A	4		T
P12	PB13B	4		C
R13	PB13C	4		T
N12	PB13D	4		C
V15	PB14A	4		T
U14	PB14B	4		C
V16	PB14C	4		T
GND	GND	-		
T14	PB14D	4		C
U15	PB15A	4		T
V17	PB15B	4		C
P13**	SLEEPN	-	SLEEPN	
T15	PB15D	4		
U16	PB16A	4		T
V18	PB16B	4		C
N13	PB16C	4		T
R14	PB16D	4		C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR10C	2		T
M18	PR10B	2		C*
L18	PR10A	2		T*
GND	GNDIO2	2		
VCCIO2	VCCIO2	2		
H16	PR9D	2		C
H14	PR9C	2		T
K18	PR9B	2		C*
J18	PR9A	2		T*
J17	PR8D	2		C
VCC	VCC	-		
H18	PR8C	2		T
H17	PR8B	2		C*
G17	PR8A	2		T*
H13	PR7D	2		C
H15	PR7C	2		T
G18	PR7B	2		C*
F18	PR7A	2		T*
G14	PR6D	2		C
G16	PR6C	2		T
VCCIO2	VCCIO2	2		
GND	GNDIO2	2		
E18	PR6B	2		C*
F17	PR6A	2		T*
G13	PR5D	2		C
G15	PR5C	2		T
E17	PR5B	2		C*
E16	PR5A	2		T*
GND	GND	-		
F15	PR4D	2		C
E15	PR4C	2		T
D17	PR4B	2		C*
D18	PR4A	2		T*
B18	PR3D	2		C
C18	PR3C	2		T
C16	PR3B	2		C*
D16	PR3A	2		T*
C17	PR2B	2		C
D15	PR2A	2		T
VCCIO2	VCCIO2	2		
GND	GNDIO2	2		
GND	GNDIO1	1		
VCCIO1	VCCIO1	1		

Conventional Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3T100I	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	IND
LCMxo256C-4T100I	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	IND
LCMxo256C-3M100I	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	IND
LCMxo256C-4M100I	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3T100I	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	IND
LCMxo640C-4T100I	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	IND
LCMxo640C-3M100I	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	IND
LCMxo640C-4M100I	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	IND
LCMxo640C-3T144I	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo640C-4T144I	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo640C-3M132I	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo640C-4M132I	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo640C-3B256I	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	IND
LCMxo640C-4B256I	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	IND
LCMxo640C-3FT256I	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	IND
LCMxo640C-4FT256I	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3T100I	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo1200C-4T100I	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo1200C-3T144I	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo1200C-4T144I	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo1200C-3M132I	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo1200C-4M132I	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo1200C-3B256I	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo1200C-4B256I	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo1200C-3FT256I	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo1200C-4FT256I	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280C-3T100I	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo2280C-4T100I	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo2280C-3T144I	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo2280C-4T144I	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo2280C-3M132I	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo2280C-4M132I	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo2280C-3B256I	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo2280C-4B256I	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo2280C-3FT256I	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo2280C-4FT256I	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND
LCMxo2280C-3FT324I	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	IND
LCMxo2280C-4FT324I	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200E-3TN100C	1200	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMxo1200E-4TN100C	1200	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMxo1200E-5TN100C	1200	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMxo1200E-3TN144C	1200	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMxo1200E-4TN144C	1200	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMxo1200E-5TN144C	1200	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMxo1200E-3MN132C	1200	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMxo1200E-4MN132C	1200	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMxo1200E-5MN132C	1200	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMxo1200E-3BN256C	1200	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMxo1200E-4BN256C	1200	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMxo1200E-5BN256C	1200	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMxo1200E-3FTN256C	1200	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMxo1200E-4FTN256C	1200	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMxo1200E-5FTN256C	1200	1.2V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280E-3TN100C	2280	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMxo2280E-4TN100C	2280	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMxo2280E-5TN100C	2280	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMxo2280E-3TN144C	2280	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMxo2280E-4TN144C	2280	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMxo2280E-5TN144C	2280	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMxo2280E-3MN132C	2280	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMxo2280E-4MN132C	2280	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMxo2280E-5MN132C	2280	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMxo2280E-3BN256C	2280	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMxo2280E-4BN256C	2280	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMxo2280E-5BN256C	2280	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMxo2280E-3FTN256C	2280	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMxo2280E-4FTN256C	2280	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMxo2280E-5FTN256C	2280	1.2V	211	-5	Lead-Free ftBGA	256	COM
LCMxo2280E-3FTN324C	2280	1.2V	271	-3	Lead-Free ftBGA	324	COM
LCMxo2280E-4FTN324C	2280	1.2V	271	-4	Lead-Free ftBGA	324	COM
LCMxo2280E-5FTN324C	2280	1.2V	271	-5	Lead-Free ftBGA	324	COM

Date	Version	Section	Change Summary
November 2006	02.3	DC and Switching Characteristics	Corrections to MachXO "C" Sleep Mode Timing table - value for $t_{WSLEEPN}$ (400ns) changed from max. to min. Value for t_{WAWAKE} (100ns) changed from min. to max.
			Added Flash Download Time table.
December 2006	02.4	Architecture	EBR Asynchronous Reset section added.
		Pinout Information	Power Supply and NC table: Pin/Ball orientation footnotes added.
February 2007	02.5	Architecture	Updated EBR Asynchronous Reset section.
August 2007	02.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table.
November 2007	02.7	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
June 2009	02.8	Introduction	Added 0.8-mm 256-pin caBGA package to MachXO Family Selection Guide table.
		Pinout Information	Added Logic Signal Connections table for 0.8-mm 256-pin caBGA package.
		Ordering Information	Updated Part Number Description diagram and Ordering Part Number tables with 0.8-mm 256-pin caBGA package information.
July 2010	02.9	DC and Switching Characteristics	Updated sysCLOCK PLL Timing table.
June 2013	03.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	MachXO1200 and MachXO2280 Hot Socketing Specifications table – Removed footnote 4.
			Added MachXO Programming/Erase Specifications table.