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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	150
Number of Logic Elements/Cells	1200
Total RAM Bits	9421
Number of I/O	113
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200c-5t144c

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip, high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

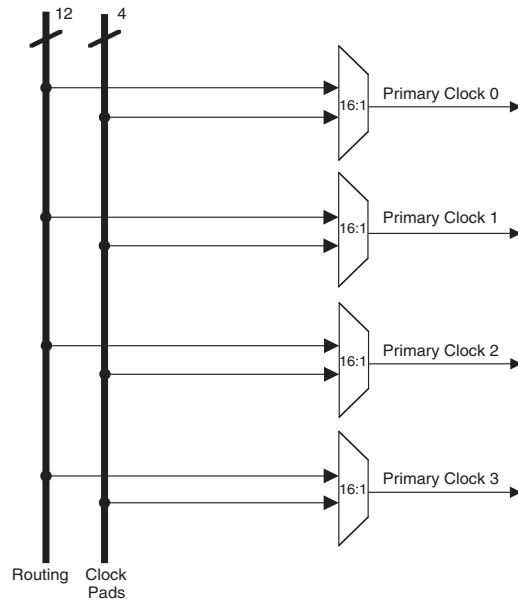
The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Popular logic synthesis tools provide synthesis library support for MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices



sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-10. PLL Diagram

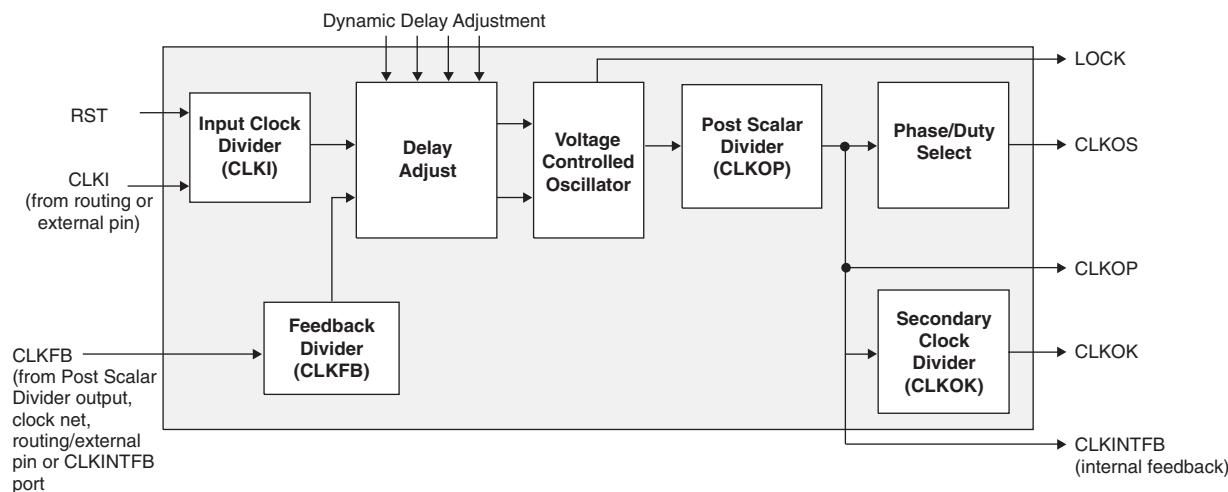
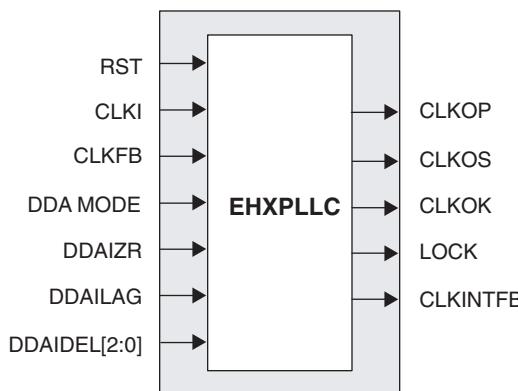


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive





MachXO Family Data Sheet

DC and Switching Characteristics

June 2013

Data Sheet DS1002

Absolute Maximum Ratings^{1, 2, 3}

	LCMXO E (1.2V)	LCMXO C (1.8V/2.5V/3.3V)
Supply Voltage V _{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V _{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V _{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied ⁴	-0.5 to 3.75V	-0.5 to 3.75V
Dedicated Input Voltage Applied ⁴	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (ambient).....	-65 to 150°C	-65 to 150°C
Junction Temp. (T _j)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V _{CCAUX} ³	Auxiliary Supply Voltage	3.135	3.465	V
V _{CCIO} ²	I/O Driver Supply Voltage	1.14	3.465	V
t _{TJCOM}	Junction Temperature Commercial Operation	0	+85	°C
t _{TJIND}	Junction Temperature Industrial Operation	-40	100	°C
t _{TFLASHCOM}	Junction Temperature, Flash Programming, Commercial	0	+85	°C
t _{TFLASHIND}	Junction Temperature, Flash Programming, Industrial	-40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both 2.5V, they must also be the same supply. 3.3V V_{CCIO} and 1.2V V_{CCIO} should be tied to V_{CCAUX} or 1.2V V_{CC} respectively.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CC} must reach minimum V_{CC} value before V_{CCAUX} reaches 2.5V.

MachXO Programming/Erase Specifications

Symbol	Parameter	Min.	Max.	Units
N _{PROGCYC}	Flash Programming Cycles per t _{RETENTION}		1,000	Cycles
	Flash Functional Programming Cycles		10,000	Cycles
t _{RETENTION}	Data Retention at 125° Junction Temperature	10		Years

MachXO256 and MachXO640 Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	+/-1000	μA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} , and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} , and V_{CCIO} .

2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) and $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).

3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

MachXO1200 and MachXO2280 Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Non-LVDS General Purpose sysIos						
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX.)	—	—	+/-1000	μA
LVDS General Purpose sysIos						
I_{DK_LVDS}	Input or I/O Leakage Current	$V_{IN} \leq V_{CCIO}$	—	—	+/-1000	μA
		$V_{IN} > V_{CCIO}$	—	35	—	mA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} , and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} , and V_{CCIO} .

2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX), and $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).

3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH} ^{1, 4, 5}	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{IH}$ (MAX)	30	—	150	μA
$I_{B HLS}$	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	μA
$I_{B HHS}$	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
$I_{B HLO}$	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	150	μA
$I_{B HHO}$	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	-150	μA
V_{BHT} ³	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = \text{Typ.}$, $V_{IO} = 0$ to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = \text{Typ.}$, $V_{IO} = 0$ to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25°C, $f = 1.0MHz$

3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.

4. Not applicable to SLEEPN pin.

5. When V_{IH} is higher than V_{CCIO} , a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For MachXO1200 and MachXO2280 true LVDS output pins, V_{IH} must be less than or equal to V_{CCIO} .

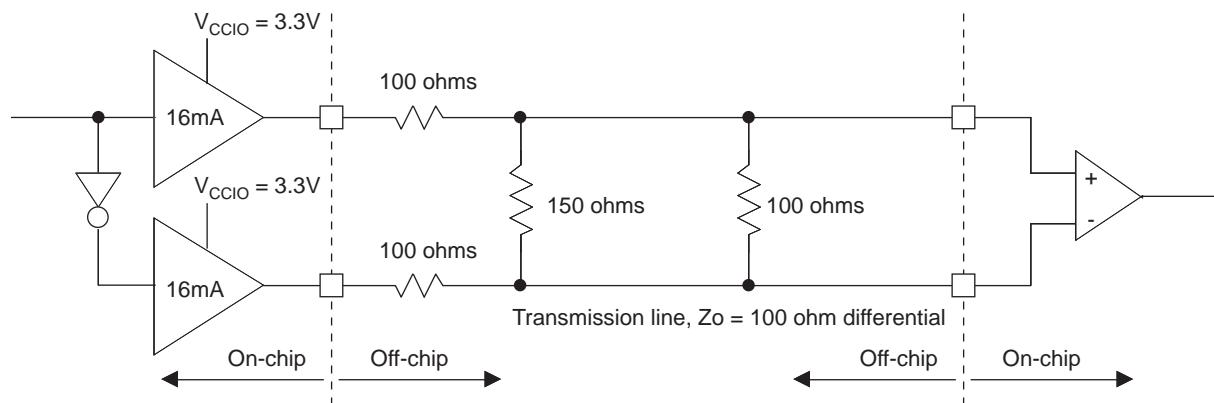
Table 3-2. BLVDS DC Conditions¹
Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	100	100	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

Table 3-3. LVPECL DC Conditions¹
Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	100	Ohms
R _P	Driver parallel resistor	150	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	2.03	V
V _{OL}	Output low voltage	1.27	V
V _{OD}	Output differential voltage	0.76	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	85.7	Ohms
I _{DC}	DC output current	12.7	mA

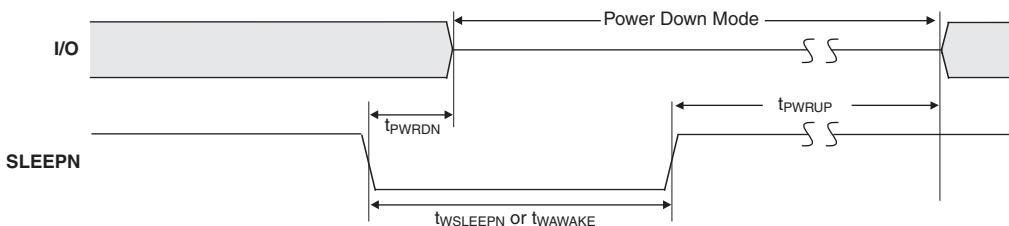
1. For input buffer, see LVDS table.

MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	SLEEPN Low to Power Down	All	—	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	LCMXO256	—	—	400	μs
		LCMXO640	—	—	600	μs
		LCMXO1200	—	—	800	μs
		LCMXO2280	—	—	1000	μs
$t_{WSLEEPN}$	SLEEPN Pulse Width	All	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	All	—	—	100	ns

Rev. A 0.19

Flash Download Time



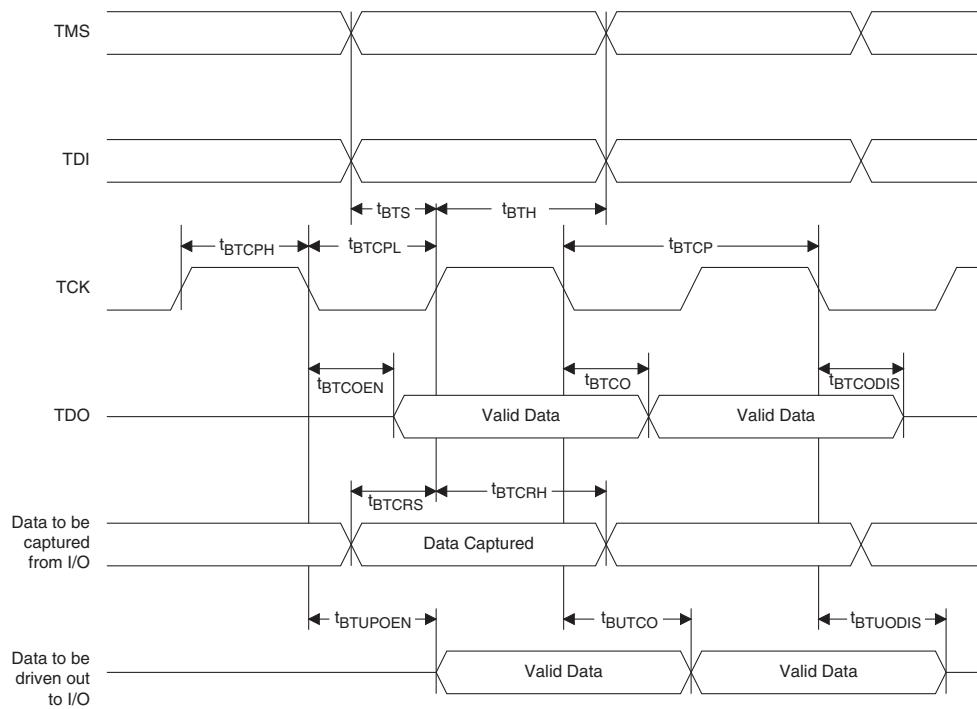
Symbol	Parameter	Min.	Typ.	Max.	Units	
$t_{REFRESH}$	Minimum V_{CC} or V_{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO256	—	—	0.4	ms
		LCMXO640	—	—	0.6	ms
		LCMXO1200	—	—	0.8	ms
		LCMXO2280	—	—	1.0	ms

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUOPEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

Rev. A 0.19

Figure 3-5. JTAG Port Timing Waveforms



Power Supply and NC (Cont.)

Signal	132 csBGA ¹	256 caBGA / 256 ftBGA ¹	324 ftBGA ¹
VCC	H3, P6, G12, C7	G7, G10, K7, K10	F14, G11, G9, H7, L7, M9
VCCIO0	LCMxo640: B11, C5 LCMxo1200/2280: C5	LCMxo640: F8, F7, F9, F10 LCMxo1200/2280: F8, F7	G8, G7
VCCIO1	LCMxo640: L12, E12 LCMxo1200/2280: B11	LCMxo640: H11, G11, K11, J11 LCMxo1200/2280: F9, F10	G12, G10
VCCIO2	LCMxo640: N2, M10 LCMxo1200/2280: E12	LCMxo640: L9, L10, L8, L7 LCMxo1200/2280: H11, G11	J12, H12
VCCIO3	LCMxo640: D2, K3 LCMxo1200/2280: L12	LCMxo640: K6, J6, H6, G6 LCMxo1200/2280: K11, J11	L12, K12
VCCIO4	LCMxo640: None LCMxo1200/2280: M10	LCMxo640: None LCMxo1200/2280: L9, L10	M12, M11
VCCIO5	LCMxo640: None LCMxo1200/2280: N2	LCMxo640: None LCMxo1200/2280: L8, L7	M8, R9
VCCIO6	LCMxo640: None LCMxo1200/2280: K3	LCMxo640: None LCMxo1200/2280: K6, J6	M7, K7
VCCIO7	LCMxo640: None LCMxo1200/2280: D2	LCMxo640: None LCMxo1200/2280: H6, G6	H6, J7
VCCAUX	P7, A7	T9, A8	M10, F9
GND ²	F1, P9, J14, C9, A10, B4, L13, D13, P2, N11, E1, L2	A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16	E14, F16, H10, H11, H8, H9, J10, J11, J4, J8, J9, K10, K11, K17, K8, K9, L10, L11, L8, L9, N2, P14, P5, R7
NC ³	—	LCMxo640: E4, E5, F5, F6, C3, C2, G4, G5, H4, H5, K5, K4, M5, M4, P2, P3, N5, N6, M7, M8, N10, N11, R15, R16, P15, P16, M11, L11, N12, N13, M13, M12, K12, J12, F12, F13, E12, E13, D13, D14, B15, A15, C14, B14, E11, E10, E7, E6, D4, D3, B3, B2 LCMxo1200: None LCMxo2280: None	—

1. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
3. NC pins should not be connected to any active signals, VCC or GND.

LCMxo1200 and LCMxo2280 Logic Signal Connections: 100 TQFP

Pin Number	LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
4	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
5	PL4B	7			PL4B	7		
6	VCCIO7	7			VCCIO7	7		
7	PL6A	7		T*	PL7A	7		T*
8	PL6B	7	GSRN	C*	PL7B	7	GSRN	C*
9	GND	-			GND	-		
10	PL7C	7		T	PL9C	7		T
11	PL7D	7		C	PL9D	7		C
12	PL8C	7		T	PL10C	7		T
13	PL8D	7		C	PL10D	7		C
14	PL9C	6			PL11C	6		
15	PL10A	6		T*	PL13A	6		T*
16	PL10B	6		C*	PL13B	6		C*
17	VCC	-			VCC	-		
18	PL11B	6			PL14D	6		C
19	PL11C	6	TSALL		PL14C	6	TSALL	T
20	VCCIO6	6			VCCIO6	6		
21	PL13C	6			PL16C	6		
22	PL14A	6	LLM0_PLLT_FB_A	T*	PL17A	6	LLM0_PLLT_FB_A	T*
23	PL14B	6	LLM0_PLLC_FB_A	C*	PL17B	6	LLM0_PLLC_FB_A	C*
24	PL15A	6	LLM0_PLLT_IN_A	T*	PL18A	6	LLM0_PLLT_IN_A	T*
25	PL15B	6	LLM0_PLLC_IN_A	C*	PL18B	6	LLM0_PLLC_IN_A	C*
26**	GNDIO6 GNDIO5	-			GNDIO6 GNDIO5	-		
27	VCCIO5	5			VCCIO5	5		
28	TMS	5	TMS		TMS	5	TMS	
29	TCK	5	TCK		TCK	5	TCK	
30	PB3B	5			PB3B	5		
31	PB4A	5		T	PB4A	5		T
32	PB4B	5		C	PB4B	5		C
33	TDO	5	TDO		TDO	5	TDO	
34	TDI	5	TDI		TDI	5	TDI	
35	VCC	-			VCC	-		
36	VCCAUX	-			VCCAUX	-		
37	PB6E	5		T	PB8E	5		T
38	PB6F	5		C	PB8F	5		C
39	PB7B	4	PCLK4_1****		PB10F	4	PCLK4_1****	
40	PB7F	4	PCLK4_0****		PB10B	4	PCLK4_0****	
41	GND	-			GND	-		

LCMxo1200 and LCMxo2280 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
82	PT9A	1			PT12C	1		T
83	GND	-			GND	-		
84	PT8B	1		C	PT11B	1		C
85	PT8A	1		T	PT11A	1		T
86	PT7D	1	PCLK1_1****		PT10B	1	PCLK1_1****	
87	PT6F	0	PCLK0_0****		PT9B	1	PCLK1_0****	
88	PT6D	0		C	PT8F	0		C
89	PT6C	0		T	PT8E	0		T
90	VCCAUX	-			VCCAUX	-		
91	VCC	-			VCC	-		
92	PT5B	0			PT6D	0		
93	PT4B	0			PT6F	0		
94	VCCIO0	0			VCCIO0	0		
95	PT3D	0		C	PT4B	0		C
96	PT3C	0		T	PT4A	0		T
97	PT3B	0			PT3B	0		
98	PT2B	0		C	PT2B	0		C
99	PT2A	0		T	PT2A	0		T
100**	GNDIO0 GNDIO7	-			GNDIO0 GNDIO7	-		

*Supports true LVDS outputs.

**Double bonded to the pin.

***NC for "E" devices.

****Primary clock inputs are single-ended.

LCMxo256 and LCMxo640 Logic Signal Connections: 100 csBGA (Cont.)

LCMxo256					LCMxo640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A4	GNDIO0	0			A4	GNDIO0	0		
B4	PT3A	0		T	B4	PT3B	0		C
A3	PT2F	0		C	A3	PT3A	0		T
B3	PT2E	0		T	B3	PT2F	0		C
A2	PT2D	0		C	A2	PT2E	0		T
C3	PT2C	0		T	C3	PT2B	0		C
A1	PT2B	0		C	A1	PT2C	0		
B2	PT2A	0		T	B2	PT2A	0		T
N9	GND	-			N9	GND	-		
B9	GND	-			B9	GND	-		
B5	VCCIO0	0			B5	VCCIO0	0		
A14	VCCIO0	0			A14	VCCIO1	1		
H14	VCCIO0	0			H14	VCCIO1	1		
P10	VCCIO1	1			P10	VCCIO2	2		
G1	VCCIO1	1			G1	VCCIO3	3		
P1	VCCIO1	1			P1	VCCIO3	3		

*NC for "E" devices.

**Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO3	VCCIO3	3			VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
E4	NC				E4	PL2A	7		T	E4	PL2A	7	LUM0_PLLT_FB_A	T
E5	NC				E5	PL2B	7		C	E5	PL2B	7	LUM0_PLLC_FB_A	C
F5	NC				F5	PL3A	7		T*	F5	PL3A	7		T*
F6	NC				F6	PL3B	7		C*	F6	PL3B	7		C*
F3	PL3A	3		T	F3	PL3C	7		T	F3	PL3C	7	LUM0_PLLT_IN_A	T
F4	PL3B	3		C	F4	PL3D	7		C	F4	PL3D	7	LUM0_PLLC_IN_A	C
E3	PL2C	3		T	E3	PL4A	7		T*	E3	PL4A	7		T*
E2	PL2D	3		C	E2	PL4B	7		C*	E2	PL4B	7		C*
C3	NC				C3	PL4C	7		T	C3	PL4C	7		T
C2	NC				C2	PL4D	7		C	C2	PL4D	7		C
B1	PL2A	3		T	B1	PL5A	7		T*	B1	PL5A	7		T*
C1	PL2B	3		C	C1	PL5B	7		C*	C1	PL5B	7		C*
VCCIO3	VCCIO3	3			VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
D2	PL3C	3		T	D2	PL5C	7		T	D2	PL6C	7		T
D1	PL3D	3		C	D1	PL5D	7		C	D1	PL6D	7		C
F2	PL5A	3		T	F2	PL6A	7		T*	F2	PL7A	7		T*
G2	PL5B	3	GSRN	C	G2	PL6B	7	GSRN	C*	G2	PL7B	7	GSRN	C*
E1	PL4A	3		T	E1	PL6C	7		T	E1	PL7C	7		T
F1	PL4B	3		C	F1	PL6D	7		C	F1	PL7D	7		C
G4	NC				G4	PL7A	7		T*	G4	PL8A	7		T*
G5	NC				G5	PL7B	7		C*	G5	PL8B	7		C*
GND	GND	-			GND	GND	-			GND	GND	-		
G3	PL4C	3		T	G3	PL7C	7		T	G3	PL8C	7		T
H3	PL4D	3		C	H3	PL7D	7		C	H3	PL8D	7		C
H4	NC				H4	PL8A	7		T*	H4	PL9A	7		T*
H5	NC				H5	PL8B	7		C*	H5	PL9B	7		C*
-	-				VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
-	-				GND	GNDIO7	7			GND	GNDIO7	7		
G1	PL5C	3		T	G1	PL8C	7		T	G1	PL10C	7		T
H1	PL5D	3		C	H1	PL8D	7		C	H1	PL10D	7		C
H2	PL6A	3		T	H2	PL9A	6		T*	H2	PL11A	6		T*
J2	PL6B	3		C	J2	PL9B	6		C*	J2	PL11B	6		C*
J3	PL7C	3		T	J3	PL9C	6		T	J3	PL11C	6		T
K3	PL7D	3		C	K3	PL9D	6		C	K3	PL11D	6		C
J1	PL6C	3		T	J1	PL10A	6		T*	J1	PL12A	6		T*
-	-				VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
-	-				GND	GNDIO6	6			GND	GNDIO6	6		
K1	PL6D	3		C	K1	PL10B	6		C*	K1	PL12B	6		C*
K2	PL9A	3		T	K2	PL10C	6		T	K2	PL12C	6		T
L2	PL9B	3		C	L2	PL10D	6		C	L2	PL12D	6		C
L1	PL7A	3		T	L1	PL11A	6		T*	L1	PL13A	6		T*
M1	PL7B	3		C	M1	PL11B	6		C*	M1	PL13B	6		C*
P1	PL8D	3		C	P1	PL11D	6		C	P1	PL14D	6		C
N1	PL8C	3	TSALL	T	N1	PL11C	6	TSALL	T	N1	PL14C	6	TSALL	T
L3	PL10A	3		T	L3	PL12A	6		T*	L3	PL15A	6		T*
M3	PL10B	3		C	M3	PL12B	6		C*	M3	PL15B	6		C*
M2	PL9C	3		T	M2	PL12C	6		T	M2	PL15C	6		T
N2	PL9D	3		C	N2	PL12D	6		C	N2	PL15D	6		C
VCCIO3	VCCIO3	3			VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
GND	GNDIO3	3			GND	GNDIO6	6			GND	GNDIO6	6		

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640				LCMxo1200				LCMxo2280					
Ball Number	Ball Function	Bank	Dual Function	Ball Number	Ball Function	Bank	Dual Function	Ball Number	Ball Function	Bank	Dual Function		
J4	PL8A	3	T	J4	PL13A	6	T*	J4	PL16A	6	T*		
J5	PL8B	3	C	J5	PL13B	6	C*	J5	PL16B	6	C*		
R1	PL11A	3	T	R1	PL13C	6	T	R1	PL16C	6	T		
R2	PL11B	3	C	R2	PL13D	6	C	R2	PL16D	6	C		
-	-	-	-	-	-	-	-	GND	GND	-	-		
K5	NC			K5	PL14A	6	LLM0_PLLT_FB_A	T*	K5	PL17A	6	LLM0_PLLT_FB_A	
K4	NC			K4	PL14B	6	LLM0_PLLC_FB_A	C*	K4	PL17B	6	LLM0_PLLC_FB_A	
L5	PL10C	3	T	L5	PL14C	6	T	L5	PL17C	6	T		
L4	PL10D	3	C	L4	PL14D	6	C	L4	PL17D	6	C		
M5	NC			M5	PL15A	6	LLM0_PLLT_IN_A	T*	M5	PL18A	6	LLM0_PLLT_IN_A	
M4	NC			M4	PL15B	6	LLM0_PLLC_IN_A	C*	M4	PL18B	6	LLM0_PLLC_IN_A	
N4	PL11C	3	T	N4	PL16A	6	T	N4	PL19A	6	T		
N3	PL11D	3	C	N3	PL16B	6	C	N3	PL19B	6	C		
VCCIO3	VCCIO3	3		VCCIO6	VCCIO6	6		VCCIO6	VCCIO6	6			
GND	GNDIO3	3		GND	GNDIO6	6		GND	GNDIO6	6			
GND	GNDIO2	2		GND	GNDIO5	5		GND	GNDIO5	5			
VCCIO2	VCCIO2	2		VCCIO5	VCCIO5	5		VCCIO5	VCCIO5	5			
P4	TMS	2	TMS	P4	TMS	5	TMS	P4	TMS	5	TMS		
P2	NC			P2	PB2A	5	T	P2	PB2A	5	T		
P3	NC			P3	PB2B	5	C	P3	PB2B	5	C		
N5	NC			N5	PB2C	5	T	N5	PB2C	5	T		
R3	TCK	2	TCK	R3	TCK	5	TCK	R3	TCK	5	TCK		
N6	NC			N6	PB2D	5	C	N6	PB2D	5	C		
T2	PB2A	2	T	T2	PB3A	5	T	T2	PB3A	5	T		
T3	PB2B	2	C	T3	PB3B	5	C	T3	PB3B	5	C		
R4	PB2C	2	T	R4	PB3C	5	T	R4	PB3C	5	T		
R5	PB2D	2	C	R5	PB3D	5	C	R5	PB3D	5	C		
P5	PB3A	2	T	P5	PB4A	5	T	P5	PB4A	5	T		
P6	PB3B	2	C	P6	PB4B	5	C	P6	PB4B	5	C		
T5	PB3C	2	T	T5	PB4C	5	T	T5	PB4C	5	T		
M6	TDO	2	TDO	M6	TDO	5	TDO	M6	TDO	5	TDO		
T4	PB3D	2	C	T4	PB4D	5	C	T4	PB4D	5	C		
R6	PB4A	2	T	R6	PB5A	5	T	R6	PB5A	5	T		
GND	GNDIO2	2		GND	GNDIO5	5		GND	GNDIO5	5			
VCCIO2	VCCIO2	2		VCCIO5	VCCIO5	5		VCCIO5	VCCIO5	5			
T6	PB4B	2	C	T6	PB5B	5	C	T6	PB5B	5	C		
N7	TDI	2	TDI	N7	TDI	5	TDI	N7	TDI	5	TDI		
T8	PB4C	2	T	T8	PB5C	5	T	T8	PB6A	5	T		
T7	PB4D	2	C	T7	PB5D	5	C	T7	PB6B	5	C		
M7	NC			M7	PB6A	5	T	M7	PB7C	5	T		
M8	NC			M8	PB6B	5	C	M8	PB7D	5	C		
T9	VCCAUX	-		T9	VCCAUX	-		T9	VCCAUX	-			
R7	PB4E	2	T	R7	PB6C	5	T	R7	PB8C	5	T		
R8	PB4F	2	C	R8	PB6D	5	C	R8	PB8D	5	C		
-	-			VCCIO5	VCCIO5	5		VCCIO5	VCCIO5	5			
-	-			GND	GNDIO5	5		GND	GNDIO5	5			
P7	PB5C	2	T	P7	PB6E	5	T	P7	PB9A	4	T		
P8	PB5D	2	C	P8	PB6F	5	C	P8	PB9B	4	C		
N8	PB5A	2	T	N8	PB7A	4	T	N8	PB10E	4	T		
N9	PB5B	2	PCLK2_1***	C	N9	PB7B	4	PCLK4_1***	C	N9	PB10F	4	PCLK4_1***
P10	PB7B	2	C	P10	PB7D	4	C	P10	PB10D	4	C		
P9	PB7A	2	T	P9	PB7C	4	T	P9	PB10C	4	T		
M9	PB6B	2	PCLK2_0***	C	M9	PB7F	4	PCLK4_0***	C	M9	PB10B	4	PCLK4_0***

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200				LCMxo2280					
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E11	NC				E11	PT10D	1		C	E11	PT15B	1		C
E10	NC				E10	PT10C	1		T	E10	PT15A	1		T
D12	PT9D	0		C	D12	PT10B	1		C	D12	PT14D	1		C
D11	PT9C	0		T	D11	PT10A	1		T	D11	PT14C	1		T
A14	PT7F	0		C	A14	PT9F	1		C	A14	PT14B	1		C
A13	PT7E	0		T	A13	PT9E	1		T	A13	PT14A	1		T
C12	PT8B	0		C	C12	PT9D	1		C	C12	PT13D	1		C
C11	PT8A	0		T	C11	PT9C	1		T	C11	PT13C	1		T
-	-			VCCIO1	VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-			GND	GNDIO1	GNDIO1	1			GND	GNDIO1	1		
B12	PT7B	0		C	B12	PT9B	1		C	B12	PT12D	1		C
B11	PT7A	0		T	B11	PT9A	1		T	B11	PT12C	1		T
A12	PT7D	0		C	A12	PT8F	1		C	A12	PT12B	1		C
A11	PT7C	0		T	A11	PT8E	1		T	A11	PT12A	1		T
GND	GND	-		GND	GND	GND	-			GND	GND	-		
B10	PT5D	0		C	B10	PT8D	1		C	B10	PT11B	1		C
B9	PT5C	0		T	B9	PT8C	1		T	B9	PT11A	1		T
D10	PT8D	0		C	D10	PT8B	1		C	D10	PT10F	1		C
D9	PT8C	0		T	D9	PT8A	1		T	D9	PT10E	1		T
-	-			VCCIO1	VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-			GND	GNDIO1	GNDIO1	1			GND	GNDIO1	1		
C10	PT6D	0		C	C10	PT7F	1		C	C10	PT10D	1		C
C9	PT6C	0		T	C9	PT7E	1		T	C9	PT10C	1		T
A9	PT6B	0	PCLK0_1***	C	A9	PT7D	1	PCLK1_1***	C	A9	PT10B	1	PCLK1_1***	C
A10	PT6A	0		T	A10	PT7C	1		T	A10	PT10A	1		T
E9	PT9B	0		C	E9	PT7B	1		C	E9	PT9D	1		C
E8	PT9A	0		T	E8	PT7A	1		T	E8	PT9C	1		T
D7	PT5B	0	PCLK0_0***	C	D7	PT6F	0	PCLK1_0***	C	D7	PT9B	1	PCLK1_0***	C
D8	PT5A	0		T	D8	PT6E	0		T	D8	PT9A	1		T
VCCIO0	VCCIO0	0		VCCIO0	VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0		GND	GNDIO0	GNDIO0	0			GND	GNDIO0	0		
C8	PT4F	0		C	C8	PT6D	0		C	C8	PT8D	0		C
B8	PT4E	0		T	B8	PT6C	0		T	B8	PT8C	0		T
A8	VCCAUX	-		A8	VCCAUX	VCCAUX	-			A8	VCCAUX	-		
A7	PT4D	0		C	A7	PT6B	0		C	A7	PT7D	0		C
A6	PT4C	0		T	A6	PT6A	0		T	A6	PT7C	0		T
VCC	VCC	-		VCC	VCC	VCC	-			VCC	VCC	-		
B7	PT4B	0		C	B7	PT5F	0		C	B7	PT7B	0		C
B6	PT4A	0		T	B6	PT5E	0		T	B6	PT7A	0		T
C6	PT3C	0		T	C6	PT5C	0		T	C6	PT6A	0		T
C7	PT3D	0		C	C7	PT5D	0		C	C7	PT6B	0		C
A5	PT3E	0		T	A5	PT5A	0		T	A5	PT6C	0		T
A4	PT3F	0		C	A4	PT5B	0		C	A4	PT6D	0		C
E7	NC			E7	PT4C	0		T	E7	PT6E	0		T	
E6	NC			E6	PT4D	0		C	E6	PT6F	0		C	
B5	PT3B	0		C	B5	PT3F	0		C	B5	PT5D	0		C
B4	PT3A	0		T	B4	PT3E	0		T	B4	PT5C	0		T
D5	PT2D	0		C	D5	PT3D	0		C	D5	PT5B	0		C
D6	PT2C	0		T	D6	PT3C	0		T	D6	PT5A	0		T
C4	PT2E	0		T	C4	PT4A	0		T	C4	PT4A	0		T
C5	PT2F	0		C	C5	PT4B	0		C	C5	PT4B	0		C
-	-	-		-	-	-	-			GND	GND	-		
D4	NC			D4	PT2D	0		C	D4	PT3D	0		C	

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
T2	PL20B	6		C
P6	TMS	5	TMS	
V1	PB2A	5		T
U2	PB2B	5		C
T3	PB2C	5		T
N7	TCK	5	TCK	
R4	PB2D	5		C
R5	PB3A	5		T
T4	PB3B	5		C
VCC	VCC	-		
R6	PB3C	5		T
P7	PB3D	5		C
U3	PB4A	5		T
T5	PB4B	5		C
V2	PB4C	5		T
N8	TDO	5	TDO	
V3	PB4D	5		C
T6	PB5A	5		T
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		
U4	PB5B	5		C
P8	PB5C	5		T
T7	PB5D	5		C
V4	TDI	5	TDI	
R8	PB6A	5		T
N9	PB6B	5		C
U5	PB6C	5		T
V5	PB6D	5		C
U6	PB7A	5		T
VCC	VCC	-		
V6	PB7B	5		C
P9	PB7C	5		T
T8	PB7D	5		C
U7	PB8A	5		T
V7	PB8B	5		C
M10	VCCAUX	-		
U8	PB8C	5		T
V8	PB8D	5		C
VCCIO5	VCCIO5	5		
GND	GNDIO5	5		
T9	PB8E	5		T
U9	PB8F	5		C
V9	PB9A	4		T

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO3	3		
VCCIO3	VCCIO3	3		
P15	PR20B	3		C
N14	PR20A	3		T
N15	PR19B	3		C
M13	PR19A	3		T
R15	PR18B	3		C*
T16	PR18A	3		T*
N16	PR17D	3		C
M14	PR17C	3		T
U17	PR17B	3		C*
VCC	VCC	-		
U18	PR17A	3		T*
R17	PR16D	3		C
R16	PR16C	3		T
P16	PR16B	3		C*
VCCIO3	VCCIO3	3		
GND	GNDIO3	3		
P17	PR16A	3		T*
L13	PR15D	3		C
M15	PR15C	3		T
T17	PR15B	3		C*
T18	PR15A	3		T*
L14	PR14D	3		C
L15	PR14C	3		T
R18	PR14B	3		C*
P18	PR14A	3		T*
GND	GND	-		
K15	PR13D	3		C
K13	PR13C	3		T
N17	PR13B	3		C*
N18	PR13A	3		T*
K16	PR12D	3		C
K14	PR12C	3		T
M16	PR12B	3		C*
L16	PR12A	3		T*
GND	GNDIO3	3		
VCCIO3	VCCIO3	3		
J16	PR11D	3		C
J14	PR11C	3		T
M17	PR11B	3		C*
L17	PR11A	3		T*
J15	PR10D	2		C

Conventional Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3T100I	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	IND
LCMxo256C-4T100I	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	IND
LCMxo256C-3M100I	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	IND
LCMxo256C-4M100I	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3T100I	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	IND
LCMxo640C-4T100I	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	IND
LCMxo640C-3M100I	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	IND
LCMxo640C-4M100I	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	IND
LCMxo640C-3T144I	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo640C-4T144I	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo640C-3M132I	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo640C-4M132I	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo640C-3B256I	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	IND
LCMxo640C-4B256I	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	IND
LCMxo640C-3FT256I	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	IND
LCMxo640C-4FT256I	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3T100I	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo1200C-4T100I	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo1200C-3T144I	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo1200C-4T144I	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo1200C-3M132I	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo1200C-4M132I	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo1200C-3B256I	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo1200C-4B256I	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo1200C-3FT256I	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo1200C-4FT256I	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280C-3T100I	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo2280C-4T100I	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo2280C-3T144I	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo2280C-4T144I	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo2280C-3M132I	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo2280C-4M132I	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo2280C-3B256I	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo2280C-4B256I	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo2280C-3FT256I	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo2280C-4FT256I	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND
LCMxo2280C-3FT324I	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	IND
LCMxo2280C-4FT324I	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	IND

Lead-Free Packaging
Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3TN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	COM
LCMxo256C-4TN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	COM
LCMxo256C-5TN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free TQFP	100	COM
LCMxo256C-3MN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	COM
LCMxo256C-4MN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	COM
LCMxo256C-5MN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3TN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	COM
LCMxo640C-4TN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	COM
LCMxo640C-5TN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free TQFP	100	COM
LCMxo640C-3MN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	COM
LCMxo640C-4MN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	COM
LCMxo640C-5MN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free csBGA	100	COM
LCMxo640C-3TN144C	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMxo640C-4TN144C	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMxo640C-5TN144C	640	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMxo640C-3MN132C	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMxo640C-4MN132C	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMxo640C-5MN132C	640	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMxo640C-3BN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	COM
LCMxo640C-4BN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	COM
LCMxo640C-5BN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free caBGA	256	COM
LCMxo640C-3FTN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	COM
LCMxo640C-4FTN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	COM
LCMxo640C-5FTN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3TN100C	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMxo1200C-4TN100C	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMxo1200C-5TN100C	1200	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMxo1200C-3TN144C	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMxo1200C-4TN144C	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMxo1200C-5TN144C	1200	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMxo1200C-3MN132C	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMxo1200C-4MN132C	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMxo1200C-5MN132C	1200	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMxo1200C-3BN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMxo1200C-4BN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMxo1200C-5BN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMxo1200C-3FTN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMxo1200C-4FTN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMxo1200C-5FTN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM

Date	Version	Section	Change Summary
April 2006 (cont.)	02.0 (cont.)	Architecture (cont.)	<p>"Top View of the MachXO1200 Device" figure updated.</p> <p>"Top View of the MachXO640 Device" figure updated.</p> <p>"Top View of the MachXO256 Device" figure updated.</p> <p>"Slice Diagram" figure updated.</p> <p>Slice Signal Descriptions table updated.</p> <p>Routing section updated.</p> <p>sysCLOCK Phase Locked Loops (PLLs) section updated.</p> <p>PLL Diagram updated.</p> <p>PLL Signal Descriptions table updated.</p> <p>sysMEM Memory section has been updated.</p> <p>PIO Groups section has been updated.</p> <p>PIO section has been updated.</p> <p>MachXO PIO Block Diagram updated.</p> <p>Supported Input Standards table updated.</p> <p>MachXO Configuration and Programming diagram updated.</p>
		DC and Switching Characteristics	<p>Recommended Operating Conditions table - footnotes updated.</p> <p>MachXO256 and MachXO640 Hot Socketing Specifications - footnotes updated.</p> <p>Added MachXO1200 and MachXO2280 Hot Socketing Specifications table.</p> <p>DC Electrical Characteristics, footnotes have been updated.</p> <p>Supply Current (Sleep Mode) table has been updated, removed "4W" references. Footnotes have been updated.</p> <p>Supply Current (Standby) table and associated footnotes updated.</p> <p>Initialization Supply Current table and footnotes updated.</p> <p>Programming and Erase Flash Supply Current table and associated footnotes have been updated.</p> <p>Register-to-Register Performance table updated (rev. A 0.19).</p> <p>MachXO External Switching Characteristics updated (rev. A 0.19).</p> <p>MachXO Internal Timing Parameters updated (rev. A 0.19).</p> <p>MachXO Family Timing Adders updated (rev. A 0.19).</p> <p>sysCLOCK Timing updated (rev. A 0.19).</p> <p>MachXO "C" Sleep Mode Timing updated (A 0.19).</p> <p>JTAG Port Timing Specification updated (rev. A 0.19).</p> <p>Test Fixture Required Components table updated.</p>
		Pinout Information	<p>Signal Descriptions have been updated.</p> <p>Pin Information Summary has been updated. Footnote has been added.</p> <p>Power Supply and NC Connection table has been updated.</p> <p>Logic Signal Connections have been updated (PCLKTx_x --> PCLKx_x)</p>
		Ordering Information	<p>Removed "4W" references.</p> <p>Added 256-ftBGA Ordering Part Numbers for MachXO640.</p>
May 2006	02.1	Pinout Information	<p>Removed [LOC][0]_PLL_RST from Signal Description table.</p> <p>PCLK footnote has been added to all appropriate pins.</p>
August 2006	02.2	Multiple	Removed 256 fpBGA information for MachXO640.