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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	150
Number of Logic Elements/Cells	1200
Total RAM Bits	9421
Number of I/O	73
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200e-3t100i

Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

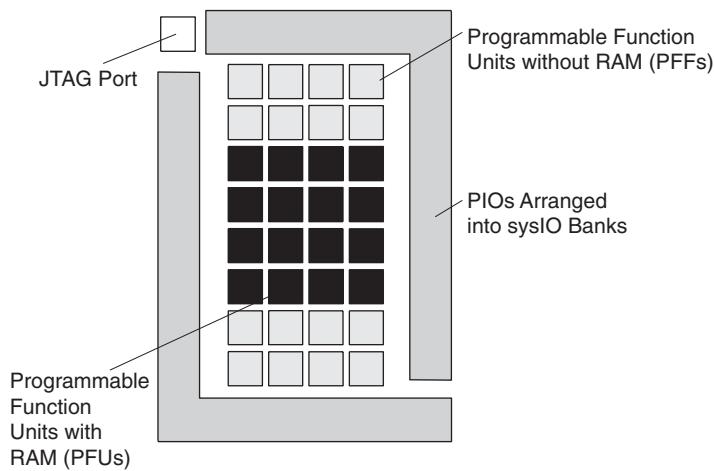
In the MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT use.

The MachXO registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

Figure 2-3. Top View of the MachXO256 Device

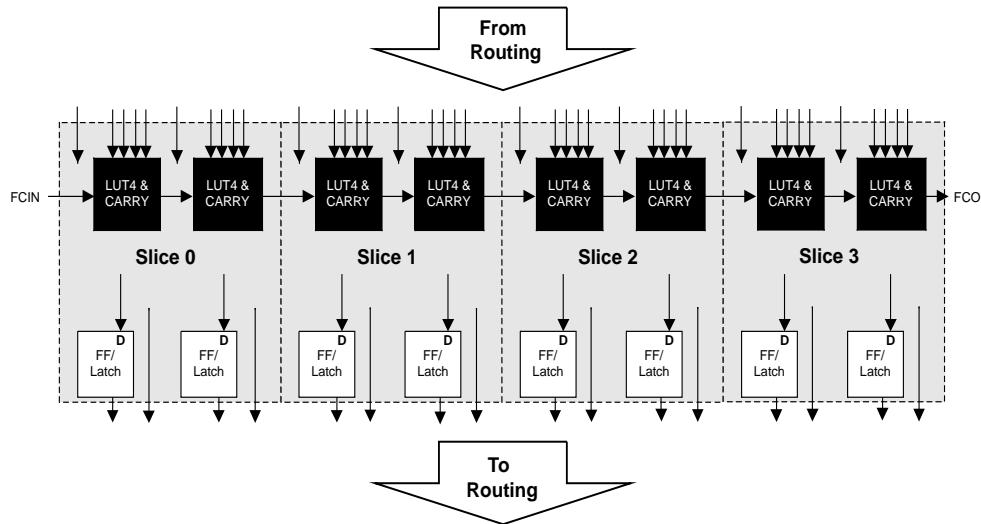


PFU Blocks

The core of the MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected Slices, numbered 0-3 as shown in Figure 2-4. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-4. PFU Diagram



Slice

Each Slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 2-5 shows an overview of the internal logic of the Slice. The registers in the Slice can be configured for positive/negative and edge/level clocks.

sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-10. PLL Diagram

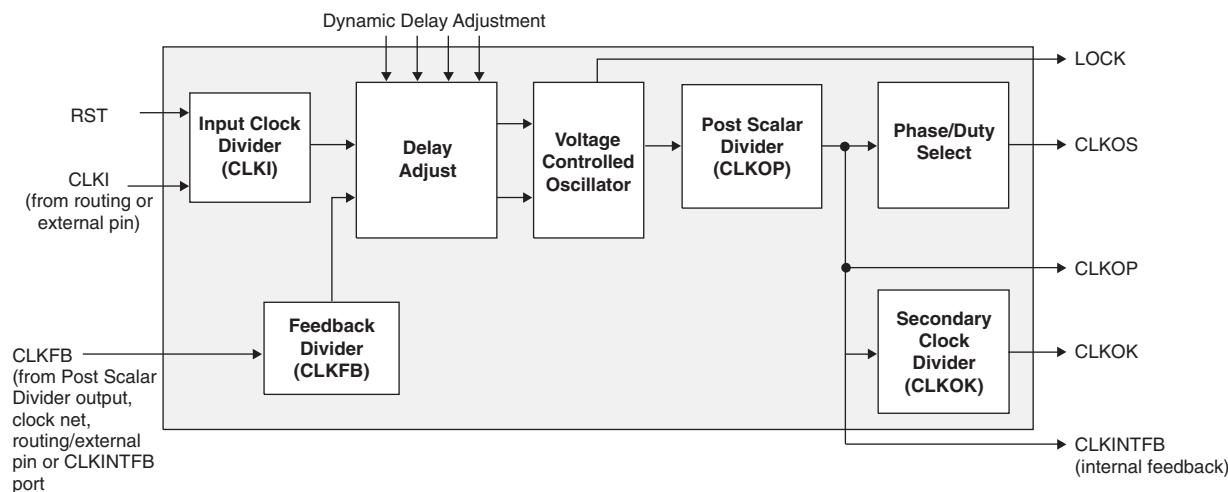


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive

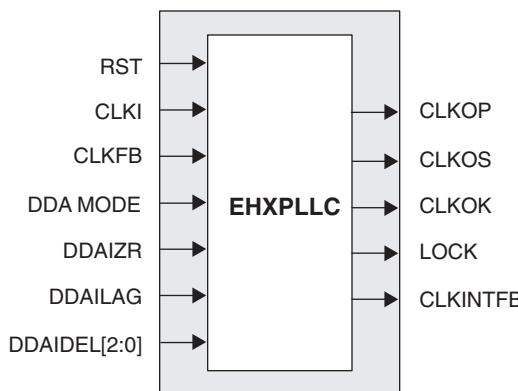
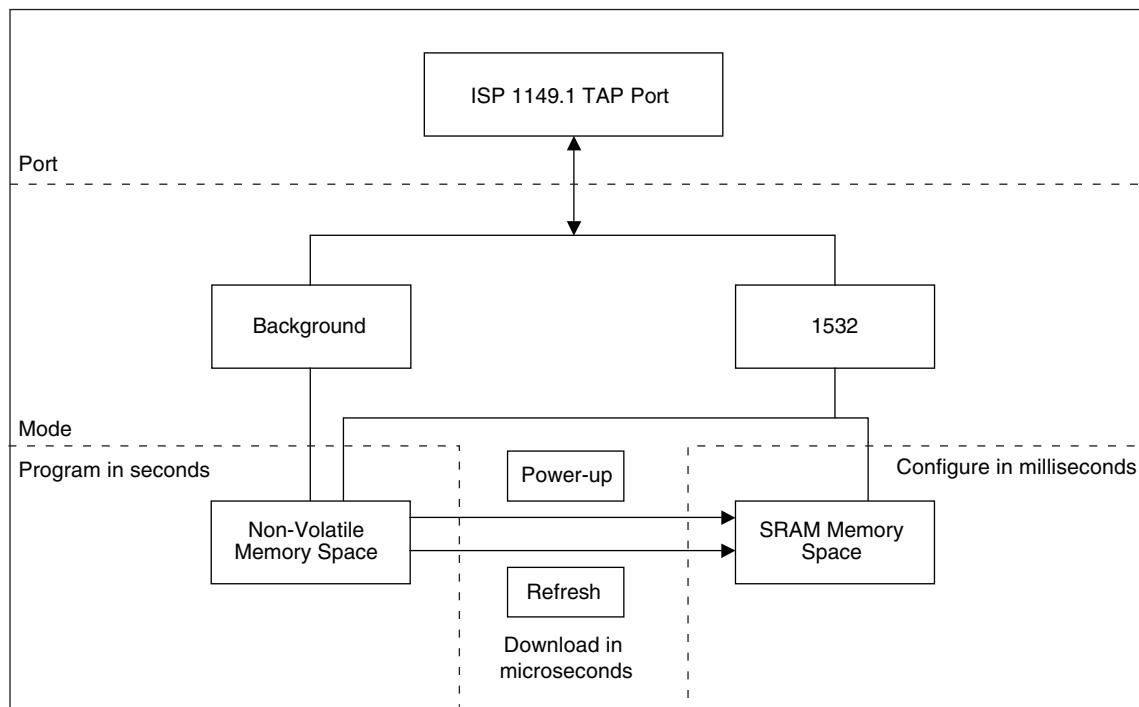


Figure 2-22. MachXO Configuration and Programming



Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Supply Current (Sleep Mode)^{1,2}

Symbol	Parameter	Device	Typ. ³	Max.	Units
I_{CC}	Core Power Supply	LCMxo256C	12	25	μA
		LCMxo640C	12	25	μA
		LCMxo1200C	12	25	μA
		LCMxo2280C	12	25	μA
I_{CCAUX}	Auxiliary Power Supply	LCMxo256C	1	15	μA
		LCMxo640C	1	25	μA
		LCMxo1200C	1	45	μA
		LCMxo2280C	1	85	μA
I_{CCIO}	Bank Power Supply ⁴	All LCMxo 'C' Devices	2	30	μA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.

2. Frequency = 0MHz.

3. $T_A = 25^\circ C$, power supplies at nominal voltage.

4. Per Bank.

Supply Current (Standby)^{1, 2, 3, 4}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMxo256C	7	mA
		LCMxo640C	9	mA
		LCMxo1200C	14	mA
		LCMxo2280C	20	mA
		LCMxo256E	4	mA
		LCMxo640E	6	mA
		LCMxo1200E	10	mA
		LCMxo2280E	12	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LCMxo256E/C	5	mA
		LCMxo640E/C	7	mA
		LCMxo1200E/C	12	mA
		LCMxo2280E/C	13	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND.

3. Frequency = 0MHz.

4. User pattern = blank.

5. $T_J = 25^\circ C$, power supplies at nominal voltage.

6. Per Bank. $V_{CCIO} = 2.5V$. Does not include pull-up/pull-down.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

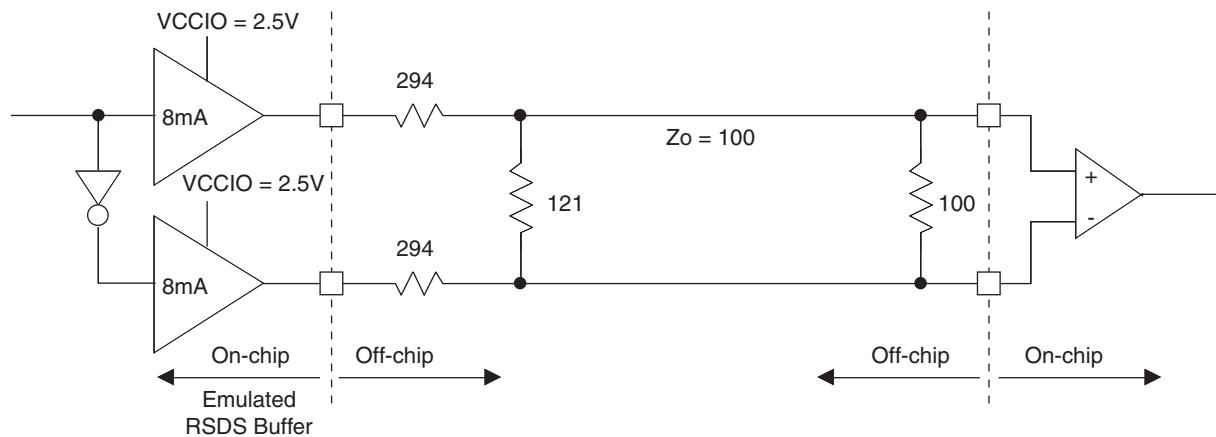


Table 3-4. RSDS DC Conditions

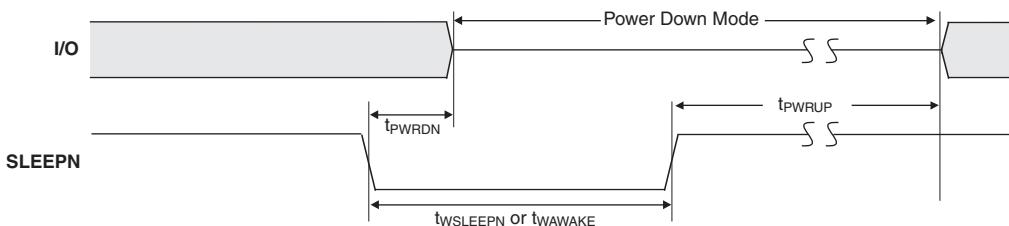
Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	SLEEPN Low to Power Down	All	—	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	LCMXO256	—	—	400	μs
		LCMXO640	—	—	600	μs
		LCMXO1200	—	—	800	μs
		LCMXO2280	—	—	1000	μs
$t_{WSLEEPN}$	SLEEPN Pulse Width	All	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	All	—	—	100	ns

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Flash Download Time



Symbol	Parameter	Min.	Typ.	Max.	Units	
$t_{REFRESH}$	Minimum V_{CC} or V_{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO256	—	—	0.4	ms
		LCMXO640	—	—	0.6	ms
		LCMXO1200	—	—	0.8	ms
		LCMXO2280	—	—	1.0	ms

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUOPEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

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LCMxo256 and LCMxo640 Logic Signal Connections: 100 TQFP

Pin Number	LCMxo256				LCMxo640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	1		T	PL2A	3		T
2	PL2B	1		C	PL2C	3		T
3	PL3A	1		T	PL2B	3		C
4	PL3B	1		C	PL2D	3		C
5	PL3C	1		T	PL3A	3		T
6	PL3D	1		C	PL3B	3		C
7	PL4A	1		T	PL3C	3		T
8	PL4B	1		C	PL3D	3		C
9	PL5A	1		T	PL4A	3		
10	VCCIO1	1			VCCIO3	3		
11	PL5B	1		C	PL4C	3		T
12	GNDIO1	1			GNDIO3	3		
13	PL5C	1		T	PL4D	3		C
14	PL5D	1	GSRN	C	PL5B	3	GSRN	
15	PL6A	1		T	PL7B	3		
16	PL6B	1	TSALL	C	PL8C	3	TSALL	T
17	PL7A	1		T	PL8D	3		C
18	PL7B	1		C	PL9A	3		
19	PL7C	1		T	PL9C	3		
20	PL7D	1		C	PL10A	3		
21	PL8A	1		T	PL10C	3		
22	PL8B	1		C	PL11A	3		
23	PL9A	1		T	PL11C	3		
24	VCCIO1	1			VCCIO3	3		
25	GNDIO1	1			GNDIO3	3		
26	TMS	1	TMS		TMS	2	TMS	
27	PL9B	1		C	PB2C	2		
28	TCK	1	TCK		TCK	2	TCK	
29	PB2A	1		T	VCCIO2	2		
30	PB2B	1		C	GNDIO2	2		
31	TDO	1	TDO		TDO	2	TDO	
32	PB2C	1		T	PB4C	2		
33	TDI	1	TDI		TDI	2	TDI	
34	PB2D	1		C	PB4E	2		
35	VCC	-			VCC	-		
36	PB3A	1	PCLK1_1**	T	PB5B	2	PCLK2_1**	
37	PB3B	1		C	PB5D	2		
38	PB3C	1	PCLK1_0**	T	PB6B	2	PCLK2_0**	
39	PB3D	1		C	PB6C	2		
40	GND	-			GND	-		
41	VCCIO1	1			VCCIO2	2		
42	GNDIO1	1			GNDIO2	2		

LCMxo256 and LCMxo640 Logic Signal Connections: 100 csBGA (Cont.)

LCMxo256					LCMxo640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
P13	PB5A	1			P13	PB9C	2		T
M12*	SLEEPN	-	SLEEPN		M12*	SLEEPN	-	SLEEPN	
P14	PB5C	1		T	P14	PB9D	2		C
N13	PB5D	1		C	N13	PB9F	2		
N14	PR9B	0		C	N14	PR11D	1		C
M14	PR9A	0		T	M14	PR11B	1		C
L13	PR8B	0		C	L13	PR11C	1		T
L14	PR8A	0		T	L14	PR11A	1		T
M13	PR7D	0		C	M13	PR10D	1		C
K14	PR7C	0		T	K14	PR10C	1		T
K13	PR7B	0		C	K13	PR10B	1		C
J14	PR7A	0		T	J14	PR10A	1		T
J13	PR6B	0		C	J13	PR9D	1		
H13	PR6A	0		T	H13	PR9B	1		
G14	GNDIO0	0			G14	GNDIO1	1		
G13	PR5D	0		C	G13	PR7B	1		
F14	PR5C	0		T	F14	PR6C	1		
F13	PR5B	0		C	F13	PR6B	1		
E14	PR5A	0		T	E14	PR5D	1		
E13	PR4B	0		C	E13	PR5B	1		
D14	PR4A	0		T	D14	PR4D	1		
D13	PR3D	0		C	D13	PR4B	1		
C14	PR3C	0		T	C14	PR3D	1		
C13	PR3B	0		C	C13	PR3B	1		
B14	PR3A	0		T	B14	PR2D	1		
C12	PR2B	0		C	C12	PR2B	1		
B13	GNDIO0	0			B13	GNDIO1	1		
A13	PR2A	0		T	A13	PT9F	0		C
A12	PT5C	0			A12	PT9E	0		T
B11	PT5B	0		C	B11	PT9C	0		
A11	PT5A	0		T	A11	PT9A	0		
B12	PT4F	0		C	B12	VCCIO0	0		
A10	PT4E	0		T	A10	GNDIO0	0		
B10	PT4D	0		C	B10	PT7E	0		
A9	PT4C	0		T	A9	PT7A	0		
A8	PT4B	0	PCLK0_1**	C	A8	PT6B	0	PCLK0_1**	
B8	PT4A	0	PCLK0_0**	T	B8	PT5B	0	PCLK0_0**	C
A7	PT3D	0		C	A7	PT5A	0		T
B7	VCCAUX	-			B7	VCCAUX	-		
A6	PT3C	0		T	A6	PT4F	0		
B6	VCC	-			B6	VCC	-		
A5	PT3B	0		C	A5	PT3F	0		

LCMxo256 and LCMxo640 Logic Signal Connections: 100 csBGA (Cont.)

LCMxo256					LCMxo640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A4	GNDIO0	0			A4	GNDIO0	0		
B4	PT3A	0		T	B4	PT3B	0		C
A3	PT2F	0		C	A3	PT3A	0		T
B3	PT2E	0		T	B3	PT2F	0		C
A2	PT2D	0		C	A2	PT2E	0		T
C3	PT2C	0		T	C3	PT2B	0		C
A1	PT2B	0		C	A1	PT2C	0		
B2	PT2A	0		T	B2	PT2A	0		T
N9	GND	-			N9	GND	-		
B9	GND	-			B9	GND	-		
B5	VCCIO0	0			B5	VCCIO0	0		
A14	VCCIO0	0			A14	VCCIO1	1		
H14	VCCIO0	0			H14	VCCIO1	1		
P10	VCCIO1	1			P10	VCCIO2	2		
G1	VCCIO1	1			G1	VCCIO3	3		
P1	VCCIO1	1			P1	VCCIO3	3		

*NC for "E" devices.

**Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
132 csBGA**

LCMxo640					LCMxo1200					LCMxo2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B1	PL2A	3		T	B1	PL2A	7		T	B1	PL2A	7	LUM0_PLLT_FB_A	T
C1	PL2B	3		C	C1	PL3C	7		T	C1	PL3C	7	LUM0_PLLT_IN_A	T
B2	PL2C	3		T	B2	PL2B	7		C	B2	PL2B	7	LUM0_PLLC_FB_A	C
C2	PL2D	3		C	C2	PL4A	7		T*	C2	PL4A	7		T*
C3	PL3A	3		T	C3	PL3D	7		C	C3	PL3D	7	LUM0_PLLC_IN_A	C
D1	PL3B	3		C	D1	PL4B	7		C*	D1	PL4B	7		C*
D3	PL3D	3			D3	PL4C	7			D3	PL4C	7		
E1	GNDIO3	3			E1	GNDIO7	7			E1	GNDIO7	7		
E2	PL5A	3		T	E2	PL6A	7		T*	E2	PL7A	7		T*
E3	PL5B	3	GSRN	C	E3	PL6B	7	GSRN	C*	E3	PL7B	7	GSRN	C*
F2	PL5D	3			F2	PL6D	7			F2	PL7D	7		
F3	PL6B	3			F3	PL7C	7		T	F3	PL9C	7		T
G1	PL6C	3		T	G1	PL7D	7		C	G1	PL9D	7		C
G2	PL6D	3		C	G2	PL8C	7		T	G2	PL10C	7		T
G3	PL7A	3		T	G3	PL8D	7		C	G3	PL10D	7		C
H2	PL7B	3		C	H2	PL10A	6		T*	H2	PL12A	6		T*
H1	PL7C	3			H1	PL10B	6		C*	H1	PL12B	6		C*
H3	VCC	-			H3	VCC	-			H3	VCC	-		
J1	PL8A	3			J1	PL11B	6			J1	PL14D	6		C
J2	PL8C	3	TSALL		J2	PL11C	6	TSALL	T	J2	PL14C	6	TSALL	T
J3	PL9A	3		T	J3	PL11D	6		C	J3	PL14B	6		
K2	PL9B	3		C	K2	PL12A	6		T*	K2	PL15A	6		T*
K1	PL9C	3			K1	PL12B	6		C*	K1	PL15B	6		C*
L2	GNDIO3	3			L2	GNDIO6	6			L2	GNDIO6	6		
L1	PL10A	3		T	L1	PL14A	6	LLM0_PLLT_FB_A	T*	L1	PL17A	6	LLM0_PLLT_FB_A	T*
L3	PL10B	3		C	L3	PL14B	6	LLM0_PLLC_FB_A	C*	L3	PL17B	6	LLM0_PLLC_FB_A	C*
M1	PL11A	3		T	M1	PL15A	6	LLM0_PLLT_IN_A	T*	M1	PL18A	6	LLM0_PLLT_IN_A	T*
N1	PL11B	3		C	N1	PL16A	6		T	N1	PL19A	6		T
M2	PL11C	3		T	M2	PL15B	6	LLM0_PLLC_IN_A	C*	M2	PL18B	6	LLM0_PLLC_IN_A	C*
P1	PL11D	3		C	P1	PL16B	6		C	P1	PL19B	6		C
P2	GNDIO2	2			P2	GNDIO5	5			P2	GNDIO5	5		
P3	TMS	2	TMS		P3	TMS	5	TMS		P3	TMS	5	TMS	
M3	PB2C	2		T	M3	PB2C	5		T	M3	PB2A	5		T
N3	PB2D	2		C	N3	PB2D	5		C	N3	PB2B	5		C
P4	TCK	2	TCK		P4	TCK	5	TCK		P4	TCK	5	TCK	
M4	PB3B	2			M4	PB3B	5			M4	PB3B	5		
N4	PB3C	2		T	N4	PB4A	5		T	N4	PB4A	5		T
P5	PB3D	2		C	P5	PB4B	5		C	P5	PB4B	5		C
N5	TDO	2	TDO		N5	TDO	5	TDO		N5	TDO	5	TDO	
M5	TDI	2	TDI		M5	TDI	5	TDI		M5	TDI	5	TDI	
N6	PB4E	2		T	N6	PB5C	5			N6	PB6C	5		
P6	VCC	-			P6	VCC	-			P6	VCC	-		
M6	PB4F	2		C	M6	PB6A	5			M6	PB8A	5		
P7	VCCAUX	-			P7	VCCAUX	-			P7	VCCAUX	-		
N7	PB5A	2		T	N7	PB6F	5			N7	PB8F	5		
M7	PB5B	2	PCLK2_1***	C	M7	PB7B	4	PCLK4_1***		M7	PB10F	4	PCLK4_1***	
N8	PB5D	2			N8	PB7C	4		T	N8	PB10C	4		T
P8	PB6A	2		T	P8	PB7D	4		C	P8	PB10D	4		C
M8	PB6B	2	PCLK2_0***	C	M8	PB7F	4	PCLK4_0***		M8	PB10B	4	PCLK4_0***	
N9	PB7A	2		T	N9	PB9A	4		T	N9	PB12A	4		T

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 144 TQFP (Cont.)**

Pin Number	LCMxo640				LCMxo1200				LCMxo2280				
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	
101	PR3D	1		C	PR4B	2			C*	PR5B	2		C*
102	PR3C	1		T	PR4A	2			T*	PR5A	2		T*
103	PR3B	1		C	PR3D	2			C	PR4D	2		C
104	PR2D	1		C	PR3C	2			T	PR4C	2		T
105	PR3A	1		T	PR3B	2			C*	PR4B	2		C*
106	PR2B	1		C	PR3A	2			T*	PR4A	2		T*
107	PR2C	1		T	PR2B	2			C	PR3B	2		C*
108	PR2A	1		T	PR2A	2			T	PR3A	2		T*
109	PT9F	0		C	PT11D	1			C	PT16D	1		C
110	PT9D	0		C	PT11C	1			T	PT16C	1		T
111	PT9E	0		T	PT11B	1			C	PT16B	1		C
112	PT9B	0		C	PT11A	1			T	PT16A	1		T
113	PT9C	0		T	PT10F	1			C	PT15D	1		C
114	PT9A	0		T	PT10E	1			T	PT15C	1		T
115	PT8C	0			PT10D	1			C	PT14B	1		C
116	PT8B	0		C	PT10C	1			T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1				VCCIO1	1		
118	GNDIO0	0			GNDIO1	1				GNDIO1	1		
119	PT8A	0		T	PT9F	1			C	PT12F	1		C
120	PT7E	0			PT9E	1			T	PT12E	1		T
121	PT7C	0			PT9B	1			C	PT12D	1		C
122	PT7A	0			PT9A	1			T	PT12C	1		T
123	GND	-			GND	-				GND	-		
124	PT6B	0	PCLK0_1***	C	PT7D	1	PCLK1_1***			PT10B	1	PCLK1_1***	
125	PT6A	0		T	PT7B	1			C	PT9D	1		C
126	PT5C	0			PT7A	1			T	PT9C	1		T
127	PT5B	0	PCLK0_0***		PT6F	0	PCLK1_0***			PT9B	1	PCLK1_0***	
128	VCCAUX	-			VCCAUX	-				VCCAUX	-		
129	VCC	-			VCC	-				VCC	-		
130	PT4D	0			PT5D	0			C	PT7B	0		C
131	PT4B	0		C	PT5C	0			T	PT7A	0		T
132	PT4A	0		T	PT5B	0			C	PT6D	0		
133	PT3F	0			PT5A	0			T	PT6E	0		T
134	PT3D	0			PT4B	0				PT6F	0		C
135	VCCIO0	0			VCCIO0	0				VCCIO0	0		
136	GNDIO0	0			GNDIO0	0				GNDIO0	0		
137	PT3B	0		C	PT3D	0			C	PT4B	0		T
138	PT2F	0		C	PT3C	0			T	PT4A	0		C
139	PT3A	0		T	PT3B	0			C	PT3B	0		C
140	PT2D	0		C	PT3A	0			T	PT3A	0		T
141	PT2E	0		T	PT2D	0			C	PT2D	0		C
142	PT2B	0		C	PT2C	0			T	PT2C	0		T
143	PT2C	0		T	PT2B	0			C	PT2B	0		C
144	PT2A	0		T	PT2A	0			T	PT2A	0		T

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T
A3	PT2B	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2A	0		T	A2	PT3A	0		T	A2	PT3A	0		T
B3	NC				B3	PT2B	0		C	B3	PT2D	0		C
B2	NC				B2	PT2A	0		T	B2	PT2C	0		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A16	GND	-			A16	GND	-			A16	GND	-		
F11	GND	-			F11	GND	-			F11	GND	-		
G8	GND	-			G8	GND	-			G8	GND	-		
G9	GND	-			G9	GND	-			G9	GND	-		
H7	GND	-			H7	GND	-			H7	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
H9	GND	-			H9	GND	-			H9	GND	-		
H10	GND	-			H10	GND	-			H10	GND	-		
J7	GND	-			J7	GND	-			J7	GND	-		
J8	GND	-			J8	GND	-			J8	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
K8	GND	-			K8	GND	-			K8	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L6	GND	-			L6	GND	-			L6	GND	-		
T1	GND	-			T1	GND	-			T1	GND	-		
T16	GND	-			T16	GND	-			T16	GND	-		
G7	VCC	-			G7	VCC	-			G7	VCC	-		
G10	VCC	-			G10	VCC	-			G10	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
K10	VCC	-			K10	VCC	-			K10	VCC	-		
H6	VCCIO3	3			H6	VCCIO7	7			H6	VCCIO7	7		
G6	VCCIO3	3			G6	VCCIO7	7			G6	VCCIO7	7		
K6	VCCIO3	3			K6	VCCIO6	6			K6	VCCIO6	6		
J6	VCCIO3	3			J6	VCCIO6	6			J6	VCCIO6	6		
L8	VCCIO2	2			L8	VCCIO5	5			L8	VCCIO5	5		
L7	VCCIO2	2			L7	VCCIO5	5			L7	VCCIO5	5		
L9	VCCIO2	2			L9	VCCIO4	4			L9	VCCIO4	4		
L10	VCCIO2	2			L10	VCCIO4	4			L10	VCCIO4	4		
K11	VCCIO1	1			K11	VCCIO3	3			K11	VCCIO3	3		
J11	VCCIO1	1			J11	VCCIO3	3			J11	VCCIO3	3		
H11	VCCIO1	1			H11	VCCIO2	2			H11	VCCIO2	2		
G11	VCCIO1	1			G11	VCCIO2	2			G11	VCCIO2	2		
F9	VCCIO0	0			F9	VCCIO1	1			F9	VCCIO1	1		
F10	VCCIO0	0			F10	VCCIO1	1			F10	VCCIO1	1		
F8	VCCIO0	0			F8	VCCIO0	0			F8	VCCIO0	0		
F7	VCCIO0	0			F7	VCCIO0	0			F7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
V10	PB9B	4		C
N10	PB9C	4		T
R10	PB9D	4		C
P10	PB10F	4	PCLK4_1***	C
T10	PB10E	4		T
U10	PB10D	4		C
V11	PB10C	4		T
U11	PB10B	4	PCLK4_0***	C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
T11	PB10A	4		T
U12	PB11A	4		T
R11	PB11B	4		C
GND	GND	-		
T12	PB11C	4		T
P11	PB11D	4		C
V12	PB12A	4		T
V13	PB12B	4		C
R12	PB12C	4		T
N11	PB12D	4		C
U13	PB12E	4		T
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
V14	PB12F	4		C
T13	PB13A	4		T
P12	PB13B	4		C
R13	PB13C	4		T
N12	PB13D	4		C
V15	PB14A	4		T
U14	PB14B	4		C
V16	PB14C	4		T
GND	GND	-		
T14	PB14D	4		C
U15	PB15A	4		T
V17	PB15B	4		C
P13**	SLEEPN	-	SLEEPN	
T15	PB15D	4		
U16	PB16A	4		T
V18	PB16B	4		C
N13	PB16C	4		T
R14	PB16D	4		C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G8	VCCIO0	0		
G7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

Conventional Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM
LCMxo256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM
LCMxo256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM
LCMxo256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM
LCMxo256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM
LCMxo256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMxo640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMxo640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMxo640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMxo640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMxo640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMxo640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMxo640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMxo640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMxo640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMxo640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMxo640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMxo640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMxo640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMxo640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMxo640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMxo640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMxo640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMxo1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMxo1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMxo1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMxo1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMxo1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMxo1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMxo1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMxo1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMxo1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMxo1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMxo1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMxo1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMxo1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMxo1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM

Lead-Free Packaging
Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3TN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	COM
LCMxo256C-4TN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	COM
LCMxo256C-5TN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free TQFP	100	COM
LCMxo256C-3MN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	COM
LCMxo256C-4MN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	COM
LCMxo256C-5MN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3TN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	COM
LCMxo640C-4TN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	COM
LCMxo640C-5TN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free TQFP	100	COM
LCMxo640C-3MN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	COM
LCMxo640C-4MN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	COM
LCMxo640C-5MN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free csBGA	100	COM
LCMxo640C-3TN144C	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMxo640C-4TN144C	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMxo640C-5TN144C	640	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMxo640C-3MN132C	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMxo640C-4MN132C	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMxo640C-5MN132C	640	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMxo640C-3BN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	COM
LCMxo640C-4BN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	COM
LCMxo640C-5BN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free caBGA	256	COM
LCMxo640C-3FTN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	COM
LCMxo640C-4FTN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	COM
LCMxo640C-5FTN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3TN100C	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMxo1200C-4TN100C	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMxo1200C-5TN100C	1200	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMxo1200C-3TN144C	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMxo1200C-4TN144C	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMxo1200C-5TN144C	1200	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMxo1200C-3MN132C	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMxo1200C-4MN132C	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMxo1200C-5MN132C	1200	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMxo1200C-3BN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMxo1200C-4BN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMxo1200C-5BN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMxo1200C-3FTN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMxo1200C-4FTN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMxo1200C-5FTN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200E-3TN100C	1200	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMxo1200E-4TN100C	1200	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMxo1200E-5TN100C	1200	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMxo1200E-3TN144C	1200	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMxo1200E-4TN144C	1200	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMxo1200E-5TN144C	1200	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMxo1200E-3MN132C	1200	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMxo1200E-4MN132C	1200	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMxo1200E-5MN132C	1200	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMxo1200E-3BN256C	1200	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMxo1200E-4BN256C	1200	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMxo1200E-5BN256C	1200	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMxo1200E-3FTN256C	1200	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMxo1200E-4FTN256C	1200	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMxo1200E-5FTN256C	1200	1.2V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280E-3TN100C	2280	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMxo2280E-4TN100C	2280	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMxo2280E-5TN100C	2280	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMxo2280E-3TN144C	2280	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMxo2280E-4TN144C	2280	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMxo2280E-5TN144C	2280	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMxo2280E-3MN132C	2280	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMxo2280E-4MN132C	2280	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMxo2280E-5MN132C	2280	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMxo2280E-3BN256C	2280	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMxo2280E-4BN256C	2280	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMxo2280E-5BN256C	2280	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMxo2280E-3FTN256C	2280	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMxo2280E-4FTN256C	2280	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMxo2280E-5FTN256C	2280	1.2V	211	-5	Lead-Free ftBGA	256	COM
LCMxo2280E-3FTN324C	2280	1.2V	271	-3	Lead-Free ftBGA	324	COM
LCMxo2280E-4FTN324C	2280	1.2V	271	-4	Lead-Free ftBGA	324	COM
LCMxo2280E-5FTN324C	2280	1.2V	271	-5	Lead-Free ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256E-3TN100I	256	1.2V	78	-3	Lead-Free TQFP	100	IND
LCMxo256E-4TN100I	256	1.2V	78	-4	Lead-Free TQFP	100	IND
LCMxo256E-3MN100I	256	1.2V	78	-3	Lead-Free csBGA	100	IND
LCMxo256E-4MN100I	256	1.2V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640E-3TN100I	640	1.2V	74	-3	Lead-Free TQFP	100	IND
LCMxo640E-4TN100I	640	1.2V	74	-4	Lead-Free TQFP	100	IND
LCMxo640E-3MN100I	640	1.2V	74	-3	Lead-Free csBGA	100	IND
LCMxo640E-4MN100I	640	1.2V	74	-4	Lead-Free csBGA	100	IND
LCMxo640E-3TN144I	640	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMxo640E-4TN144I	640	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMxo640E-3MN132I	640	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMxo640E-4MN132I	640	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMxo640E-3BN256I	640	1.2V	159	-3	Lead-Free caBGA	256	IND
LCMxo640E-4BN256I	640	1.2V	159	-4	Lead-Free caBGA	256	IND
LCMxo640E-3FTN256I	640	1.2V	159	-3	Lead-Free ftBGA	256	IND
LCMxo640E-4FTN256I	640	1.2V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200E-3TN100I	1200	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMxo1200E-4TN100I	1200	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMxo1200E-3TN144I	1200	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMxo1200E-4TN144I	1200	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMxo1200E-3MN132I	1200	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMxo1200E-4MN132I	1200	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMxo1200E-3BN256I	1200	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMxo1200E-4BN256I	1200	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMxo1200E-3FTN256I	1200	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMxo1200E-4FTN256I	1200	1.2V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280E-3TN100I	2280	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMxo2280E-4TN100I	2280	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMxo2280E-3TN144I	2280	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMxo2280E-4TN144I	2280	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMxo2280E-3MN132I	2280	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMxo2280E-4MN132I	2280	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMxo2280E-3BN256I	2280	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMxo2280E-4BN256I	2280	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMxo2280E-3FTN256I	2280	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMxo2280E-4FTN256I	2280	1.2V	211	-4	Lead-Free ftBGA	256	IND
LCMxo2280E-3FTN324I	2280	1.2V	271	-3	Lead-Free ftBGA	324	IND
LCMxo2280E-4FTN324I	2280	1.2V	271	-4	Lead-Free ftBGA	324	IND



MachXO Family Data Sheet

Revision History

June 2013

Data Sheet DS1002

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
October 2005	01.1	Introduction	Distributed RAM information in family table updated. Added footnote 1 - fpBGA packaging to the family selection guide.
		Architecture	sysIO Buffer section updated.
			Hot Socketing section updated.
			Sleep Mode section updated.
			SLEEP Pin Characteristics section updated.
			Oscillator section updated.
		DC and Switching Characteristics	Security section updated.
			Recommended Operating Conditions table updated.
			DC Electrical Characteristics table updated.
			Supply Current (Sleep Mode) table added with LCMXO256/640 data.
			Supply Current (Standby) table updated with LCMXO256/640 data.
			Initialization Supply Current table updated with LCMXO256/640 data.
			Programming and Erase Flash Supply Current table updated with LCMXO256/640 data.
			Register-to-Register Performance table updated (rev. A 0.16).
			External Switching Characteristics table updated (rev. A 0.16).
			Internal Timing Parameter table updated (rev. A 0.16).
			Family Timing Adders updated (rev. A 0.16).
			sysCLOCK Timingupdated (rev. A 0.16).
			MachXO "C" Sleep Mode Timing updated (A 0.16).
		Pinout Information	JTAG Port Timing Specification updated (rev. A 0.16).
			SLEEPIN description updated.
			Pin Information Summary updated.
			Power Supply and NC Connection table has been updated.
		Ordering Information	Logic Signal Connection section has been updated to include all devices/packages.
			Part Number Description section has been updated.
			Ordering Part Number section has been updated (added LCMXO256C/ LCMXO640C "4W").
		Supplemental Information	MachXO Density Migration Technical Note (TN1097) added.
November 2005	01.2	Pinout Information	Added "Power Supply and NC Connections" summary information for LCMXO1200 and LCMXO2280 in 100 TQFP package.
December 2005	01.3	DC and Switching Characteristics	Supply Current (Standby) table updated with LCMXO1200/2280 data.
		Ordering Information	Ordering Part Number section updated (added LCMXO2280C "4W").
April 2006	02.0	Introduction	Introduction paragraphs updated.
		Architecture	Architecture Overview paragraphs updated.

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