# Lattice Semiconductor Corporation - LCMXO1200E-4FT256C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 150 |
| Number of Logic Elements/Cells | 1200 |
| Total RAM Bits | 9421 |
| Number of I/O | 211 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200e-4ft256c |

# MachXO Family Data Sheet Introduction

June 2013 Data Sheet DS1002

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- **Sleep Mode**
  - Allows up to 100x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **High I/O to Logic Density**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.7 Kbits distributed RAM
  - Dedicated FIFO control logic
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide, and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - Onboard oscillator
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
  - IEEE 1532 compliant in-system programming

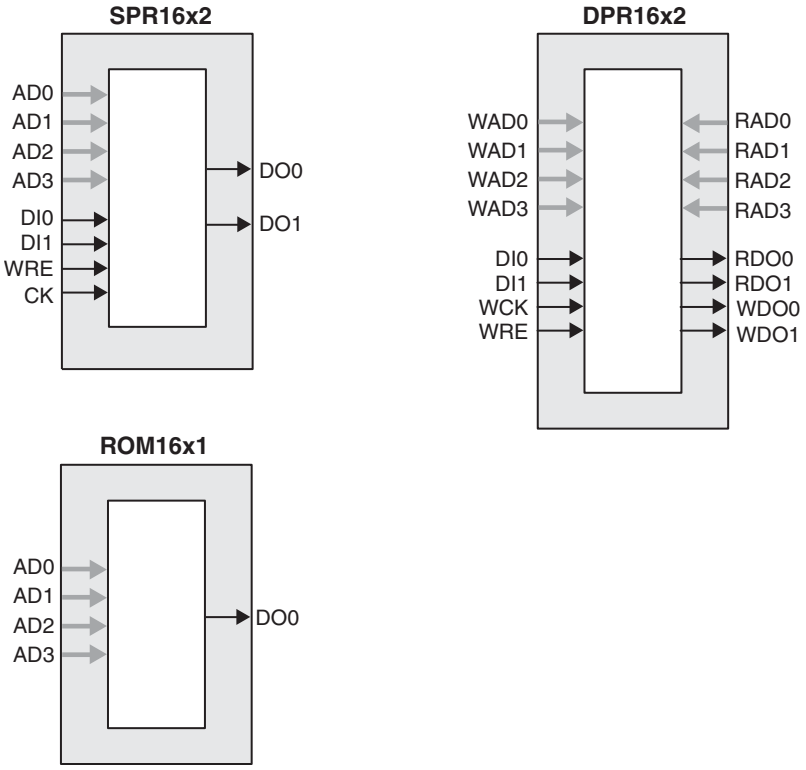
## Introduction

The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, and control logic. These devices bring together the best features of CPLD and FPGA devices on a single chip.

***Table 1-1. MachXO Family Selection Guide***

| Device | LCMXO256 | LCMXO640 | LCMXO1200 | LCMXO2280 |
|---|---|---|---|---|
| LUTs | 256 | 640 | 1200 | 2280 |
| Dist. RAM (Kbits) | 2.0 | 6.1 | 6.4 | 7.7 |
| EBR SRAM (Kbits) | 0 | 0 | 9.2 | 27.6 |
| Number of EBR SRAM Blocks (9 Kbits) | 0 | 0 | 1 | 3 |
| $V_{CC}$ Voltage | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V |
| Number of PLLs | 0 | 0 | 1 | 2 |
| Max. I/O | 78 | 159 | 211 | 271 |
| **Packages** | | | | |
| 100-pin TQFP (14x14 mm) | 78 | 74 | 73 | 73 |
| 144-pin TQFP (20x20 mm) | | 113 | 113 | 113 |
| 100-ball csBGA (8x8 mm) | 78 | 74 | | |
| 132-ball csBGA (8x8 mm) | | 101 | 101 | 101 |
| 256-ball caBGA (14x14 mm) | | 159 | 211 | 211 |
| 256-ball ftBGA (17x17 mm) | | 159 | 211 | 211 |
| 324-ball ftBGA (19x19 mm) | | | | 271 |

*Figure 2-6. Distributed Memory Primitives*




**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

**PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

*Table 2-4. PFU Modes of Operation*

| Logic | Ripple | RAM | ROM |
|---|---|---|---|
| LUT 4x8 or MUX 2x1 x 8 | 2-bit Add x 4 | SPR16x2 x 4 DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4 | 2-bit Sub x 4 | SPR16x4 x 2 DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1 | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM16x8 x 1 |

## Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

**FIFO Configuration**

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2-7.

***Table 2-7. Programmable FIFO Flag Ranges***

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

**Memory Core Reset**

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

of the devices also support differential input buffers. PCI clamps are available on the top Bank I/O buffers. The PCI clamp is enabled after $V_{CC}$, $V_{CCAUX}$, and $V_{CCIO}$ are at valid operating levels and the device has been configured.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Left and Right sysIO Buffer Pairs**
The sysIO buffer pairs in the left and right Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these Banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all $V_{CCIO}$ Banks are active with valid input logic levels to properly control the output logic states of all the I/O Banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to VCCIO. The I/O pins will maintain the blank configuration until VCC, VCCAUX and VCCIO have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore, $V_{CCIO}$ supplies should be powered up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies

**Supported Standards**

The MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The MachXO1200 and MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right Banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all Banks of MachXO1200 and MachXO2280 devices. PCI support is provided in the top Banks of the MachXO1200 and MachXO2280 devices. Table 2-8 summarizes the I/O characteristics of the devices in the MachXO family.

Tables 2-9 and 2-10 show the I/O standards (together with their supply and reference voltages) supported by the MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

*Table 2-8. I/O Support Device by Device*

| | MachXO256 | MachXO640 | MachXO1200 | MachXO2280 |
|---|---|---|---|---|
| Number of I/O Banks | 2 | 4 | 8 | 8 |
| Type of Input Buffers | Single-ended (all I/O Banks) | Single-ended (all I/O Banks) | Single-ended (all I/O Banks)<br><br>Differential Receivers (all I/O Banks) | Single-ended (all I/O Banks)<br><br>Differential Receivers (all I/O Banks) |
| Types of Output Buffers | Single-ended buffers with complementary outputs (all I/O Banks) | Single-ended buffers with complementary outputs (all I/O Banks) | Single-ended buffers with complementary outputs (all I/O Banks)<br><br>Differential buffers with true LVDS outputs (50% on left and right side) | Single-ended buffers with complementary outputs (all I/O Banks)<br><br>Differential buffers with true LVDS outputs (50% on left and right side) |
| Differential Output Emulation Capability | All I/O Banks | All I/O Banks | All I/O Banks | All I/O Banks |
| PCI Support | No | No | Top side only | Top side only |

*Table 2-9. Supported Input Standards*

| | VCCIO (Typ.) | | | | |
|---|---|---|---|---|---|
| **Input Standard** | **3.3V** | **2.5V** | **1.8V** | **1.5V** | **1.2V** |
| **Single Ended Interfaces** | | | | | |
| LVTTL | Yes | Yes | Yes | Yes | Yes |
| LVCMOS33 | Yes | Yes | Yes | Yes | Yes |
| LVCMOS25 | Yes | Yes | Yes | Yes | Yes |
| LVCMOS18 | | | Yes | | |
| LVCMOS15 | | | | Yes | |
| LVCMOS12 | Yes | Yes | Yes | Yes | Yes |
| PCI[1] | Yes | | | | |
| **Differential Interfaces** | | | | | |
| BLVDS[2], LVDS[2], LVPECL[2], RSDS[2] | Yes | Yes | Yes | Yes | Yes |

1. Top Banks of MachXO1200 and MachXO2280 devices only.
2. MachXO1200 and MachXO2280 devices only.

*Figure 2-18. MachXO2280 Banks*

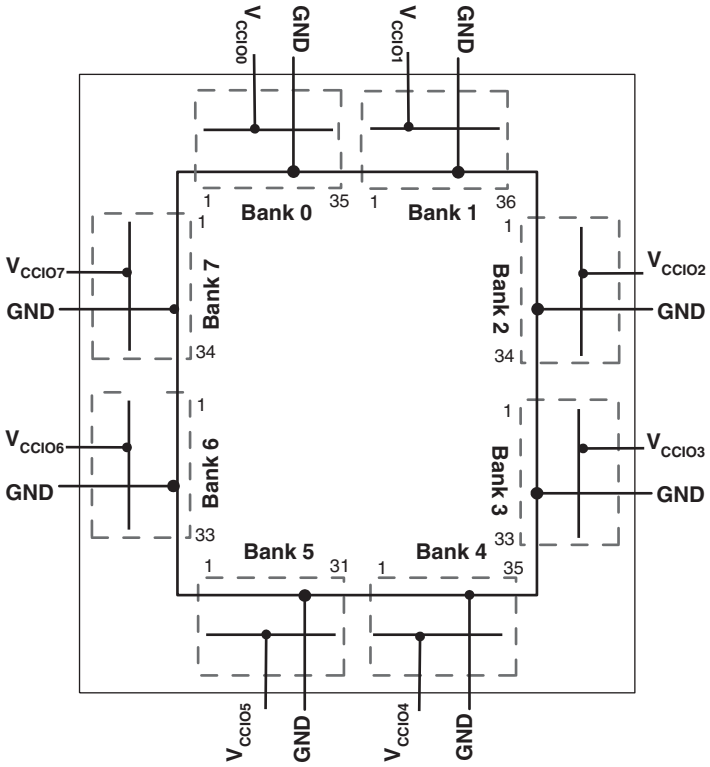
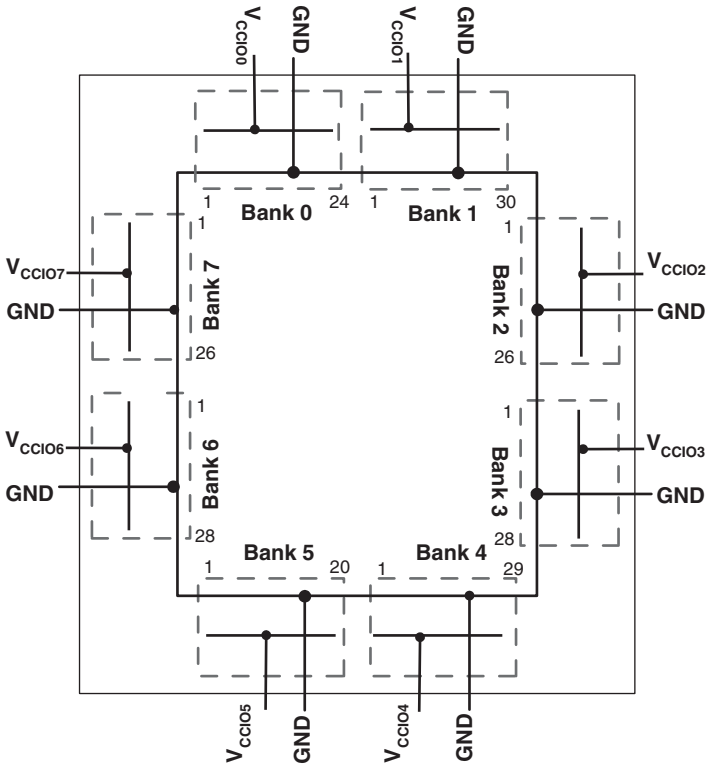



*Figure 2-19. MachXO1200 Banks*



the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

## Sleep Mode

The MachXO "C" devices ($V_{CC}$ = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

***Table 2-11. Characteristics of Normal, Off and Sleep Modes***

| Characteristic | Normal | Off | Sleep |
|---|---|---|---|
| SLEEPN Pin | High | — | Low |
| Static Icc | Typical <10mA | 0 | Typical <100uA |
| I/O Leakage | <10µA | <1mA | <10µA |
| Power Supplies VCC/VCCIO/VCCAUX | Normal Range | 0 | Normal Range |
| Logic Operation | User Defined | Non Operational | Non operational |
| I/O Operation | User Defined | Tri-state | Tri-state |
| JTAG and Programming circuitry | Operational | Non-operational | Non-operational |
| EBR Contents and Registers | Maintained | Non-maintained | Non-maintained |

### SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

## Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

## Configuration and Testing

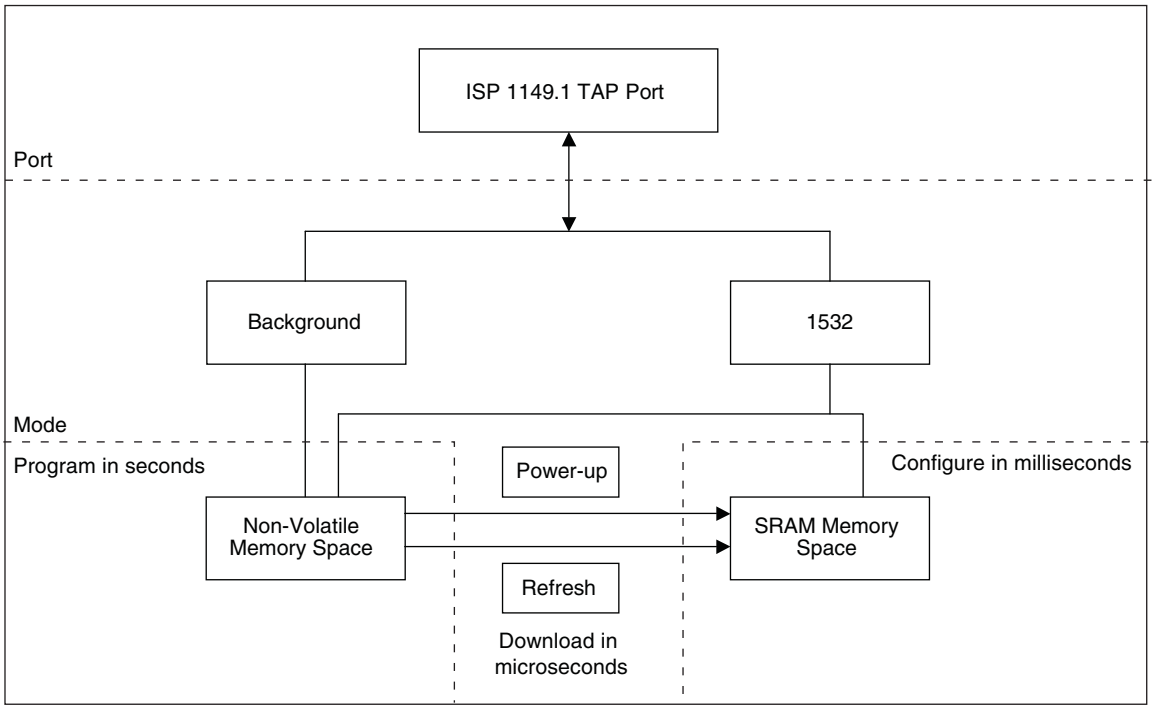
The following section describes the configuration and testing features of the MachXO family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: $V_{CCIO1}$; MachXO640: $V_{CCIO2}$; MachXO1200 and MachXO2280: $V_{CCIO5}$) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

*Figure 2-22. MachXO Configuration and Programming*




## Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

## Absolute Maximum Ratings[1, 2, 3]

| | LCMXO E (1.2V) | LCMXO C (1.8V/2.5V/3.3V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCAUX}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Output Supply Voltage $V_{CCIO}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| I/O Tristate Voltage Applied [4] | -0.5 to 3.75V | -0.5 to 3.75V |
| Dedicated Input Voltage Applied[4] | -0.5 to 3.75V | -0.5 to 4.25V |
| Storage Temperature (ambient) | -65 to 150°C | -65 to 150°C |
| Junction Temp. (Tj) | +125°C | +125°C |

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions[1]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage for 1.2V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCAUX}$[3] | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}$[2] | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| $t_{JCOM}$ | Junction Temperature Commercial Operation | 0 | +85 | °C |
| $t_{JIND}$ | Junction Temperature Industrial Operation | -40 | 100 | °C |
| $t_{JFLASHCOM}$ | Junction Temperature, Flash Programming, Commercial | 0 | +85 | °C |
| $t_{JFLASHIND}$ | Junction Temperature, Flash Programming, Industrial | -40 | 100 | °C |

1. Like power supplies must be tied together. For example, if $V_{CCIO}$ and $V_{CC}$ are both 2.5V, they must also be the same supply. 3.3V $V_{CCIO}$ and 1.2V $V_{CCIO}$ should be tied to $V_{CCAUX}$ or 1.2V $V_{CC}$ respectively.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CC}$ must reach minimum $V_{CC}$ value before $V_{CCAUX}$ reaches 2.5V.

## MachXO Programming/Erase Specifications

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $N_{PROGCYC}$ | Flash Programming Cycles per $t_{RETENTION}$ | | 1,000 | Cycles |
| | Flash Functional Programming Cycles | | 10,000 | Cycles |
| $t_{RETENTION}$ | Data Retention at 125° Junction Temperature | 10 | | Years |

## Supply Current (Sleep Mode)[1, 2]

| Symbol | Parameter | Device | Typ.[3] | Max. | Units |
|---|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | 12 | 25 | µA |
| | | LCMXO640C | 12 | 25 | µA |
| | | LCMXO1200C | 12 | 25 | µA |
| | | LCMXO2280C | 12 | 25 | µA |
| $I_{CCAUX}$ | Auxiliary Power Supply | LCMXO256C | 1 | 15 | µA |
| | | LCMXO640C | 1 | 25 | µA |
| | | LCMXO1200C | 1 | 45 | µA |
| | | LCMXO2280C | 1 | 85 | µA |
| $I_{CCIO}$ | Bank Power Supply[4] | All LCMXO 'C' Devices | 2 | 30 | µA |

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency = 0MHz.
3. $T_A$ = 25°C, power supplies at nominal voltage.
4. Per Bank.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | 7 | mA |
| | | LCMXO640C | 9 | mA |
| | | LCMXO1200C | 14 | mA |
| | | LCMXO2280C | 20 | mA |
| | | LCMXO256E | 4 | mA |
| | | LCMXO640E | 6 | mA |
| | | LCMXO1200E | 10 | mA |
| | | LCMXO2280E | 12 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256E/C | 5 | mA |
| | | LCMXO640E/C | 7 | mA |
| | | LCMXO1200E/C | 12 | mA |
| | | LCMXO2280E/C | 13 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All devices | 2 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND.
3. Frequency = 0MHz.
4. User pattern = blank.
5. $T_J$ = 25°C, power supplies at nominal voltage.
6. Per Bank. $V_{CCIO}$ = 2.5V. Does not include pull-up/pull-down.

*Table 3-2. BLVDS DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | Ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ohms |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

## LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

*Figure 3-3. Differential LVPECL*

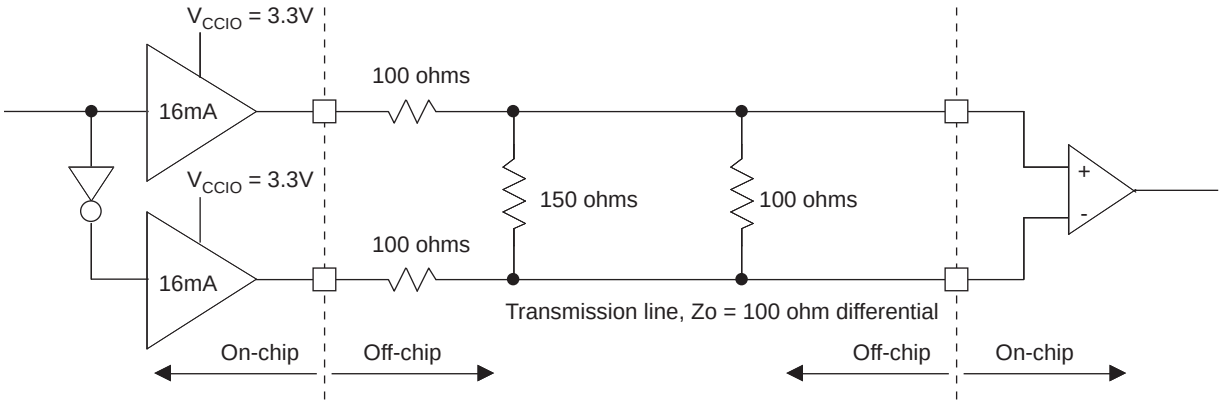


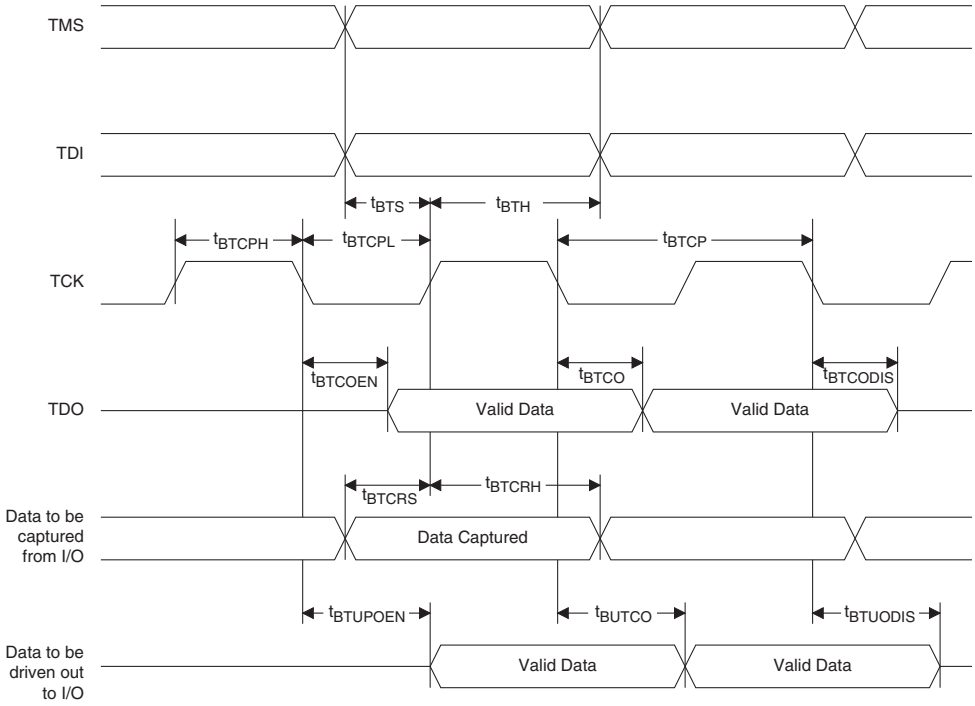

*Table 3-3. LVPECL DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | Ohms |
| $R_P$ | Driver parallel resistor | 150 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | Ohms |
| $I_{DC}$ | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

*Figure 3-5. JTAG Port Timing Waveforms*



# Pin Information Summary

| Pin Type | | LCMXO256C/E | | LCMXO640C/E | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 100 csBGA | 100 TQFP | 144 TQFP | 100 csBGA | 132 csBGA | 256 caBGA / 256 ftBGA |
| Single Ended User I/O | | 78 | 78 | 74 | 113 | 74 | 101 | 159 |
| Differential Pair User I/O[1] | | 38 | 38 | 17 | 43 | 17 | 42 | 79 |
| Muxed | | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| TAP | | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Dedicated (Total Without Supplies) | | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| VCC | | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| VCCAUX | | 1 | 1 | 1 | 2 | 1 | 2 | 2 |
| VCCIO | Bank0 | 3 | 3 | 2 | 2 | 2 | 2 | 4 |
| | Bank1 | 3 | 3 | 2 | 2 | 2 | 2 | 4 |
| | Bank2 | — | — | 2 | 2 | 2 | 2 | 4 |
| | Bank3 | — | — | 2 | 2 | 2 | 2 | 4 |
| GND | | 8 | 8 | 10 | 12 | 10 | 12 | 18 |
| NC | | 0 | 0 | 0 | 0 | 0 | 0 | 52 |
| Single Ended/Differential I/O per Bank | Bank0 | 41/20 | 41/20 | 18/5 | 29/10 | 18/5 | 26/11 | 42/21 |
| | Bank1 | 37/18 | 37/18 | 21/4 | 30/11 | 21/4 | 27/12 | 40/20 |
| | Bank2 | — | — | 14/2 | 24/9 | 14/2 | 21/9 | 36/18 |
| | Bank3 | — | — | 21/6 | 30/13 | 21/6 | 27/10 | 40/20 |

1. These devices support emulated LVDS outputs.þLVDS inputs are not supported.

| Pin Type | | LCMXO1200C/E | | | | LCMXO2280C/E | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 144 TQFP | 132 csBGA | 256 caBGA / 256 ftBGA | 100 TQFP | 144 TQFP | 132 csBGA | 256 caBGA / 256 ftBGA | 324 ftBGA |
| Single Ended User I/O | | 73 | 113 | 101 | 211 | 73 | 113 | 101 | 211 | 271 |
| Differential Pair User I/O[1] | | 27 | 48 | 42 | 105 | 30 | 47 | 41 | 105 | 134 |
| Muxed | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| TAP | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Dedicated (Total Without Supplies) | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| VCC | | 4 | 4 | 4 | 4 | 2 | 4 | 4 | 4 | 6 |
| VCCAUX | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| VCCIO | Bank0 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank2 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank3 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank4 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank5 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank6 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank7 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| GND | | 8 | 12 | 12 | 18 | 8 | 12 | 12 | 18 | 24 |
| NC | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Single Ended/Differential I/O per Bank | Bank0 | 10/3 | 14/6 | 13/5 | 26/13 | 9/3 | 13/6 | 12/5 | 24/12 | 34/17 |
| | Bank1 | 8/2 | 15/7 | 13/5 | 28/14 | 9/3 | 16/7 | 14/5 | 30/15 | 36/18 |
| | Bank2 | 10/4 | 15/7 | 13/6 | 26/13 | 10/4 | 15/7 | 13/6 | 26/13 | 34/17 |
| | Bank3 | 11/5 | 15/7 | 14/7 | 28/14 | 11/5 | 15/7 | 14/7 | 28/14 | 34/17 |
| | Bank4 | 8/3 | 14/5 | 13/5 | 27/13 | 8/3 | 14/4 | 13/4 | 29/14 | 35/17 |
| | Bank5 | 5/2 | 10/4 | 8/2 | 22/11 | 5/2 | 10/4 | 8/2 | 20/10 | 30/15 |
| | Bank6 | 10/3 | 15/6 | 13/6 | 28/14 | 10/4 | 15/6 | 13/6 | 28/14 | 34/17 |
| | Bank7 | 11/5 | 15/6 | 14/6 | 26/13 | 11/5 | 15/6 | 14/6 | 26/13 | 34/17 |

1. These devices support on-chip LVDS buffers for left and right I/O Banks.

## LCMXO1200 and LCMXO2280 Logic Signal Connections: 100 TQFP

| Pin Number | LCMXO1200 | | | | LCMXO2280 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 1 | PL2A | 7 | | T | PL2A | 7 | LUM0_PLLT_FB_A | T |
| 2 | PL2B | 7 | | C | PL2B | 7 | LUM0_PLLC_FB_A | C |
| 3 | PL3C | 7 | | T | PL3C | 7 | LUM0_PLLT_IN_A | T |
| 4 | PL3D | 7 | | C | PL3D | 7 | LUM0_PLLC_IN_A | C |
| 5 | PL4B | 7 | | | PL4B | 7 | | |
| 6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 7 | PL6A | 7 | | T* | PL7A | 7 | | T* |
| 8 | PL6B | 7 | GSRN | C* | PL7B | 7 | GSRN | C* |
| 9 | GND | - | | | GND | - | | |
| 10 | PL7C | 7 | | T | PL9C | 7 | | T |
| 11 | PL7D | 7 | | C | PL9D | 7 | | C |
| 12 | PL8C | 7 | | T | PL10C | 7 | | T |
| 13 | PL8D | 7 | | C | PL10D | 7 | | C |
| 14 | PL9C | 6 | | | PL11C | 6 | | |
| 15 | PL10A | 6 | | T* | PL13A | 6 | | T* |
| 16 | PL10B | 6 | | C* | PL13B | 6 | | C* |
| 17 | VCC | - | | | VCC | - | | |
| 18 | PL11B | 6 | | | PL14D | 6 | | C |
| 19 | PL11C | 6 | TSALL | | PL14C | 6 | TSALL | T |
| 20 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 21 | PL13C | 6 | | | PL16C | 6 | | |
| 22 | PL14A | 6 | LLM0_PLLT_FB_A | T* | PL17A | 6 | LLM0_PLLT_FB_A | T* |
| 23 | PL14B | 6 | LLM0_PLLC_FB_A | C* | PL17B | 6 | LLM0_PLLC_FB_A | C* |
| 24 | PL15A | 6 | LLM0_PLLT_IN_A | T* | PL18A | 6 | LLM0_PLLT_IN_A | T* |
| 25 | PL15B | 6 | LLM0_PLLC_IN_A | C* | PL18B | 6 | LLM0_PLLC_IN_A | C* |
| 26** | GNDIO6 GNDIO5 | - | | | GNDIO6 GNDIO5 | - | | |
| 27 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 28 | TMS | 5 | TMS | | TMS | 5 | TMS | |
| 29 | TCK | 5 | TCK | | TCK | 5 | TCK | |
| 30 | PB3B | 5 | | | PB3B | 5 | | |
| 31 | PB4A | 5 | | T | PB4A | 5 | | T |
| 32 | PB4B | 5 | | C | PB4B | 5 | | C |
| 33 | TDO | 5 | TDO | | TDO | 5 | TDO | |
| 34 | TDI | 5 | TDI | | TDI | 5 | TDI | |
| 35 | VCC | - | | | VCC | - | | |
| 36 | VCCAUX | - | | | VCCAUX | - | | |
| 37 | PB6E | 5 | | T | PB8E | 5 | | T |
| 38 | PB6F | 5 | | C | PB8F | 5 | | C |
| 39 | PB7B | 4 | PCLK4_1**** | | PB10F | 4 | PCLK4_1**** | |
| 40 | PB7F | 4 | PCLK4_0**** | | PB10B | 4 | PCLK4_0**** | |
| 41 | GND | - | | | GND | - | | |

## LCMXO1200 and LCMXO2280 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | LCMXO1200 | | | | LCMXO2280 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 82 | PT9A | 1 | | | PT12C | 1 | | T |
| 83 | GND | - | | | GND | - | | |
| 84 | PT8B | 1 | | C | PT11B | 1 | | C |
| 85 | PT8A | 1 | | T | PT11A | 1 | | T |
| 86 | PT7D | 1 | PCLK1_1**** | | PT10B | 1 | PCLK1_1**** | |
| 87 | PT6F | 0 | PCLK0_0**** | | PT9B | 1 | PCLK1_0**** | |
| 88 | PT6D | 0 | | C | PT8F | 0 | | C |
| 89 | PT6C | 0 | | T | PT8E | 0 | | T |
| 90 | VCCAUX | - | | | VCCAUX | - | | |
| 91 | VCC | - | | | VCC | - | | |
| 92 | PT5B | 0 | | | PT6D | 0 | | |
| 93 | PT4B | 0 | | | PT6F | 0 | | |
| 94 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 95 | PT3D | 0 | | C | PT4B | 0 | | C |
| 96 | PT3C | 0 | | T | PT4A | 0 | | T |
| 97 | PT3B | 0 | | | PT3B | 0 | | |
| 98 | PT2B | 0 | | C | PT2B | 0 | | C |
| 99 | PT2A | 0 | | T | PT2A | 0 | | T |
| 100** | GNDIO0 GNDIO7 | - | | | GNDIO0 GNDIO7 | - | | |

*Supports true LVDS outputs.
**Double bonded to the pin.
***NC for "E" devices.
****Primary clock inputs are single-ended.

## LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA

| LCMXO256 | | | | | LCMXO640 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Dual Function | Differen-tial | Ball Number | Ball Function | Bank | Dual Function | Differen-tial |
| B1 | PL2A | 1 | | T | B1 | PL2A | 3 | | T |
| C1 | PL2B | 1 | | C | C1 | PL2C | 3 | | T |
| D2 | PL3A | 1 | | T | D2 | PL2B | 3 | | C |
| D1 | PL3B | 1 | | C | D1 | PL2D | 3 | | C |
| C2 | PL3C | 1 | | T | C2 | PL3A | 3 | | T |
| E1 | PL3D | 1 | | C | E1 | PL3B | 3 | | C |
| E2 | PL4A | 1 | | T | E2 | PL3C | 3 | | T |
| F1 | PL4B | 1 | | C | F1 | PL3D | 3 | | C |
| F2 | PL5A | 1 | | T | F2 | PL4A | 3 | | |
| G2 | PL5B | 1 | | C | G2 | PL4C | 3 | | T |
| H1 | GNDIO1 | 1 | | | H1 | GNDIO3 | 3 | | |
| H2 | PL5C | 1 | | T | H2 | PL4D | 3 | | C |
| J1 | PL5D | 1 | GSRN | C | J1 | PL5B | 3 | GSRN | |
| J2 | PL6A | 1 | | T | J2 | PL7B | 3 | | |
| K1 | PL6B | 1 | TSALL | C | K1 | PL8C | 3 | TSALL | T |
| K2 | PL7A | 1 | | T | K2 | PL8D | 3 | | C |
| L1 | PL7B | 1 | | C | L1 | PL9A | 3 | | |
| L2 | PL7C | 1 | | T | L2 | PL9C | 3 | | |
| M1 | PL7D | 1 | | C | M1 | PL10A | 3 | | |
| M2 | PL8A | 1 | | T | M2 | PL10C | 3 | | |
| N1 | PL8B | 1 | | C | N1 | PL11A | 3 | | |
| M3 | PL9A | 1 | | T | M3 | PL11C | 3 | | |
| N2 | GNDIO1 | 1 | | | N2 | GNDIO3 | 3 | | |
| P2 | TMS | 1 | TMS | | P2 | TMS | 2 | TMS | |
| P3 | PL9B | 1 | | C | P3 | PB2C | 2 | | |
| N4 | TCK | 1 | TCK | | N4 | TCK | 2 | TCK | |
| P4 | PB2A | 1 | | T | P4 | VCCIO2 | 2 | | |
| N3 | PB2B | 1 | | C | N3 | GNDIO2 | 2 | | |
| P5 | TDO | 1 | TDO | | P5 | TDO | 2 | TDO | |
| N5 | PB2C | 1 | | T | N5 | PB4C | 2 | | |
| P6 | TDI | 1 | TDI | | P6 | TDI | 2 | TDI | |
| N6 | PB2D | 1 | | C | N6 | PB4E | 2 | | |
| P7 | VCC | - | | | P7 | VCC | - | | |
| N7 | PB3A | 1 | PCLK1_1** | T | N7 | PB5B | 2 | PCLK2_1** | |
| P8 | PB3B | 1 | | C | P8 | PB5D | 2 | | |
| N8 | PB3C | 1 | PCLK1_0** | T | N8 | PB6B | 2 | PCLK2_0** | |
| P9 | PB3D | 1 | | C | P9 | PB6C | 2 | | |
| N10 | GNDIO1 | 1 | | | N10 | GNDIO2 | 2 | | |
| P11 | PB4A | 1 | | T | P11 | PB8B | 2 | | |
| N11 | PB4B | 1 | | C | N11 | PB8C | 2 | | T |
| P12 | PB4C | 1 | | T | P12 | PB8D | 2 | | C |
| N12 | PB4D | 1 | | C | N12 | PB9A | 2 | | |

## LCMXO2280 Logic Signal Connections: 324 ftBGA

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| GND | GNDIO7 | 7 | | |
| VCCIO7 | VCCIO7 | 7 | | |
| D4 | PL2A | 7 | LUM0_PLLT_FB_A | T |
| F5 | PL2B | 7 | LUM0_PLLC_FB_A | C |
| B3 | PL3A | 7 | | T* |
| C3 | PL3B | 7 | | C* |
| E4 | PL3C | 7 | LUM0_PLLT_IN_A | T |
| G6 | PL3D | 7 | LUM0_PLLC_IN_A | C |
| A1 | PL4A | 7 | | T* |
| B1 | PL4B | 7 | | C* |
| F4 | PL4C | 7 | | T |
| VCC | VCC | - | | |
| E3 | PL4D | 7 | | C |
| D2 | PL5A | 7 | | T* |
| D3 | PL5B | 7 | | C* |
| G5 | PL5C | 7 | | T |
| F3 | PL5D | 7 | | C |
| C2 | PL6A | 7 | | T* |
| VCCIO7 | VCCIO7 | 7 | | |
| GND | GNDIO7 | 7 | | |
| C1 | PL6B | 7 | | C* |
| H5 | PL6C | 7 | | T |
| G4 | PL6D | 7 | | C |
| E2 | PL7A | 7 | | T* |
| D1 | PL7B | 7 | GSRN | C* |
| J6 | PL7C | 7 | | T |
| H4 | PL7D | 7 | | C |
| F2 | PL8A | 7 | | T* |
| E1 | PL8B | 7 | | C* |
| GND | GND | - | | |
| J3 | PL8C | 7 | | T |
| J5 | PL8D | 7 | | C |
| G3 | PL9A | 7 | | T* |
| H3 | PL9B | 7 | | C* |
| K3 | PL9C | 7 | | T |
| K5 | PL9D | 7 | | C |
| F1 | PL10A | 7 | | T* |
| VCCIO7 | VCCIO7 | 7 | | |
| GND | GNDIO7 | 7 | | |
| G1 | PL10B | 7 | | C* |
| K4 | PL10C | 7 | | T |
| K6 | PL10D | 7 | | C |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| GND | GNDIO3 | 3 | | |
| VCCIO3 | VCCIO3 | 3 | | |
| P15 | PR20B | 3 | | C |
| N14 | PR20A | 3 | | T |
| N15 | PR19B | 3 | | C |
| M13 | PR19A | 3 | | T |
| R15 | PR18B | 3 | | C* |
| T16 | PR18A | 3 | | T* |
| N16 | PR17D | 3 | | C |
| M14 | PR17C | 3 | | T |
| U17 | PR17B | 3 | | C* |
| VCC | VCC | - | | |
| U18 | PR17A | 3 | | T* |
| R17 | PR16D | 3 | | C |
| R16 | PR16C | 3 | | T |
| P16 | PR16B | 3 | | C* |
| VCCIO3 | VCCIO3 | 3 | | |
| GND | GNDIO3 | 3 | | |
| P17 | PR16A | 3 | | T* |
| L13 | PR15D | 3 | | C |
| M15 | PR15C | 3 | | T |
| T17 | PR15B | 3 | | C* |
| T18 | PR15A | 3 | | T* |
| L14 | PR14D | 3 | | C |
| L15 | PR14C | 3 | | T |
| R18 | PR14B | 3 | | C* |
| P18 | PR14A | 3 | | T* |
| GND | GND | - | | |
| K15 | PR13D | 3 | | C |
| K13 | PR13C | 3 | | T |
| N17 | PR13B | 3 | | C* |
| N18 | PR13A | 3 | | T* |
| K16 | PR12D | 3 | | C |
| K14 | PR12C | 3 | | T |
| M16 | PR12B | 3 | | C* |
| L16 | PR12A | 3 | | T* |
| GND | GNDIO3 | 3 | | |
| VCCIO3 | VCCIO3 | 3 | | |
| J16 | PR11D | 3 | | C |
| J14 | PR11C | 3 | | T |
| M17 | PR11B | 3 | | C* |
| L17 | PR11A | 3 | | T* |
| J15 | PR10D | 2 | | C |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| A10 | PT8E | 0 | | T |
| VCCIO0 | VCCIO0 | 0 | | |
| GND | GNDIO0 | 0 | | |
| A9 | PT8D | 0 | | C |
| C9 | PT8C | 0 | | T |
| B9 | PT8B | 0 | | C |
| F9 | VCCAUX | - | | |
| A8 | PT8A | 0 | | T |
| B8 | PT7D | 0 | | C |
| C8 | PT7C | 0 | | T |
| VCC | VCC | - | | |
| A7 | PT7B | 0 | | C |
| B7 | PT7A | 0 | | T |
| A6 | PT6A | 0 | | T |
| B6 | PT6B | 0 | | C |
| D8 | PT6C | 0 | | T |
| F8 | PT6D | 0 | | C |
| C7 | PT6E | 0 | | T |
| E8 | PT6F | 0 | | C |
| D7 | PT5D | 0 | | C |
| VCCIO0 | VCCIO0 | 0 | | |
| GND | GNDIO0 | 0 | | |
| E7 | PT5C | 0 | | T |
| A5 | PT5B | 0 | | C |
| C6 | PT5A | 0 | | T |
| B5 | PT4A | 0 | | T |
| A4 | PT4B | 0 | | C |
| D6 | PT4C | 0 | | T |
| F7 | PT4D | 0 | | C |
| B4 | PT4E | 0 | | T |
| GND | GND | - | | |
| C5 | PT4F | 0 | | C |
| F6 | PT3D | 0 | | C |
| E5 | PT3C | 0 | | T |
| E6 | PT3B | 0 | | C |
| D5 | PT3A | 0 | | T |
| A3 | PT2D | 0 | | C |
| C4 | PT2C | 0 | | T |
| A2 | PT2B | 0 | | C |
| B2 | PT2A | 0 | | T |
| VCCIO0 | VCCIO0 | 0 | | |
| GND | GNDIO0 | 0 | | |
| E14 | GND | - | | |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280C-3TN100C | 2280 | 1.8V/2.5V/3.3V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO2280C-4TN100C | 2280 | 1.8V/2.5V/3.3V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO2280C-5TN100C | 2280 | 1.8V/2.5V/3.3V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO2280C-3TN144C | 2280 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO2280C-4TN144C | 2280 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO2280C-5TN144C | 2280 | 1.8V/2.5V/3.3V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO2280C-3MN132C | 2280 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO2280C-4MN132C | 2280 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO2280C-5MN132C | 2280 | 1.8V/2.5V/3.3V | 101 | -5 | Lead-Free csBGA | 132 | COM |
| LCMXO2280C-3BN256C | 2280 | 1.8V/2.5V/3.3V | 211 | -3 | Lead-Free caBGA | 256 | COM |
| LCMXO2280C-4BN256C | 2280 | 1.8V/2.5V/3.3V | 211 | -4 | Lead-Free caBGA | 256 | COM |
| LCMXO2280C-5BN256C | 2280 | 1.8V/2.5V/3.3V | 211 | -5 | Lead-Free caBGA | 256 | COM |
| LCMXO2280C-3FTN256C | 2280 | 1.8V/2.5V/3.3V | 211 | -3 | Lead-Free ftBGA | 256 | COM |
| LCMXO2280C-4FTN256C | 2280 | 1.8V/2.5V/3.3V | 211 | -4 | Lead-Free ftBGA | 256 | COM |
| LCMXO2280C-5FTN256C | 2280 | 1.8V/2.5V/3.3V | 211 | -5 | Lead-Free ftBGA | 256 | COM |
| LCMXO2280C-3FTN324C | 2280 | 1.8V/2.5V/3.3V | 271 | -3 | Lead-Free ftBGA | 324 | COM |
| LCMXO2280C-4FTN324C | 2280 | 1.8V/2.5V/3.3V | 271 | -4 | Lead-Free ftBGA | 324 | COM |
| LCMXO2280C-5FTN324C | 2280 | 1.8V/2.5V/3.3V | 271 | -5 | Lead-Free ftBGA | 324 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256E-3TN100C | 256 | 1.2V | 78 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO256E-4TN100C | 256 | 1.2V | 78 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO256E-5TN100C | 256 | 1.2V | 78 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO256E-3MN100C | 256 | 1.2V | 78 | -3 | Lead-Free csBGA | 100 | COM |
| LCMXO256E-4MN100C | 256 | 1.2V | 78 | -4 | Lead-Free csBGA | 100 | COM |
| LCMXO256E-5MN100C | 256 | 1.2V | 78 | -5 | Lead-Free csBGA | 100 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640E-3TN100C | 640 | 1.2V | 74 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO640E-4TN100C | 640 | 1.2V | 74 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO640E-5TN100C | 640 | 1.2V | 74 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO640E-3MN100C | 640 | 1.2V | 74 | -3 | Lead-Free csBGA | 100 | COM |
| LCMXO640E-4MN100C | 640 | 1.2V | 74 | -4 | Lead-Free csBGA | 100 | COM |
| LCMXO640E-5MN100C | 640 | 1.2V | 74 | -5 | Lead-Free csBGA | 100 | COM |
| LCMXO640E-3TN144C | 640 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO640E-4TN144C | 640 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO640E-5TN144C | 640 | 1.2V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO640E-3MN132C | 640 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO640E-4MN132C | 640 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO640E-5MN132C | 640 | 1.2V | 101 | -5 | Lead-Free csBGA | 132 | COM |
| LCMXO640E-3BN256C | 640 | 1.2V | 159 | -3 | Lead-Free caBGA | 256 | COM |
| LCMXO640E-4BN256C | 640 | 1.2V | 159 | -4 | Lead-Free caBGA | 256 | COM |
| LCMXO640E-5BN256C | 640 | 1.2V | 159 | -5 | Lead-Free caBGA | 256 | COM |
| LCMXO640E-3FTN256C | 640 | 1.2V | 159 | -3 | Lead-Free ftBGA | 256 | COM |
| LCMXO640E-4FTN256C | 640 | 1.2V | 159 | -4 | Lead-Free ftBGA | 256 | COM |
| LCMXO640E-5FTN256C | 640 | 1.2V | 159 | -5 | Lead-Free ftBGA | 256 | COM |