Lattice Semiconductor Corporation - LCMXO1200E-4T100I Datasheet

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Details	
Product Status	Obsolete
Number of LABs/CLBs	150
Number of Logic Elements/Cells	1200
Total RAM Bits	9421
Number of I/O	73
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo1200e-4t100i

MachXO Family Data Sheet Architecture

June 2013 Data Sheet DS1002

Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT use.

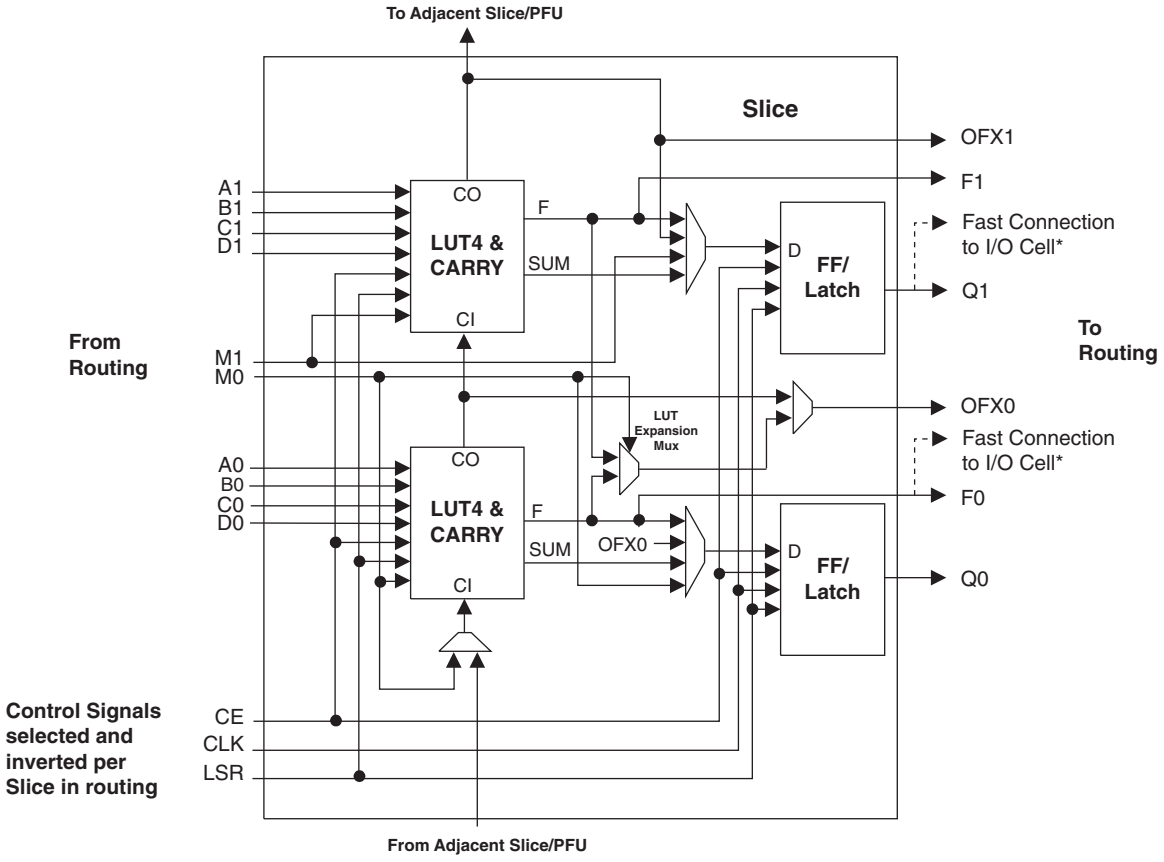
The MachXO registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2-1 lists the signals associated with each Slice.

Figure 2-5. Slice Diagram



Notes:
Some inter-Slice signals are not shown.
*** Only PFUs at the edges have fast connections to the I/O cell.**

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the Slice
Output	Inter-PFU signal	FCO	Fast Carry Out[1]

1. See Figure 2-4 for connection details.
2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

FIFO Configuration

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2-7.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

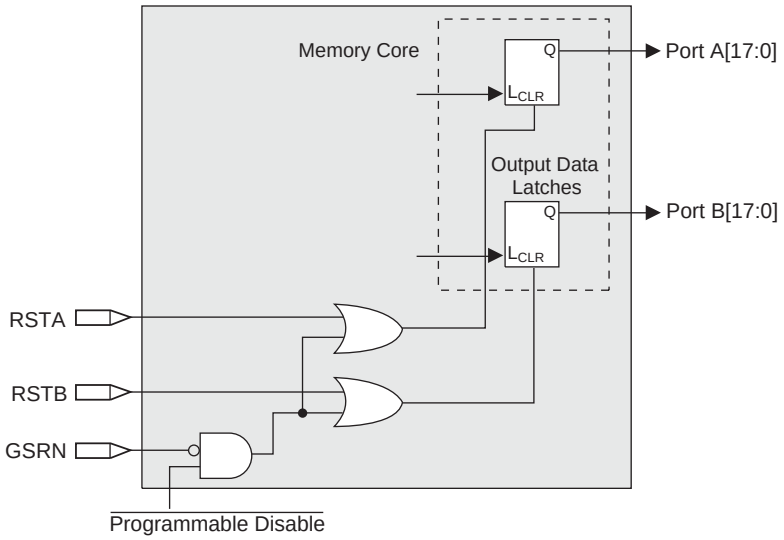
N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

Figure 2-13. Memory Core Reset

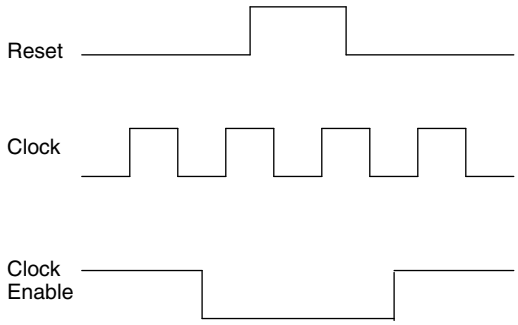


For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPReset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled

Device Configuration

All MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-22 provides a pictorial representation of the different programming modes available in the MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

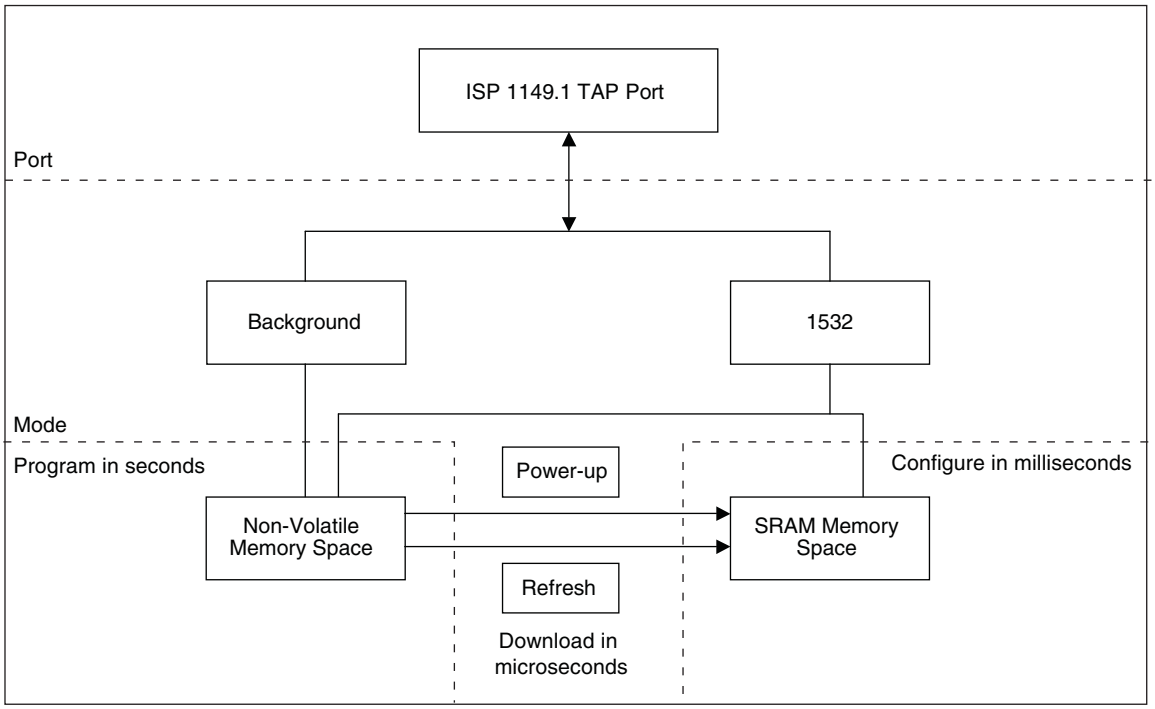
Leave Alone I/O
When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

Security
The MachXO devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-22. MachXO Configuration and Programming



Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

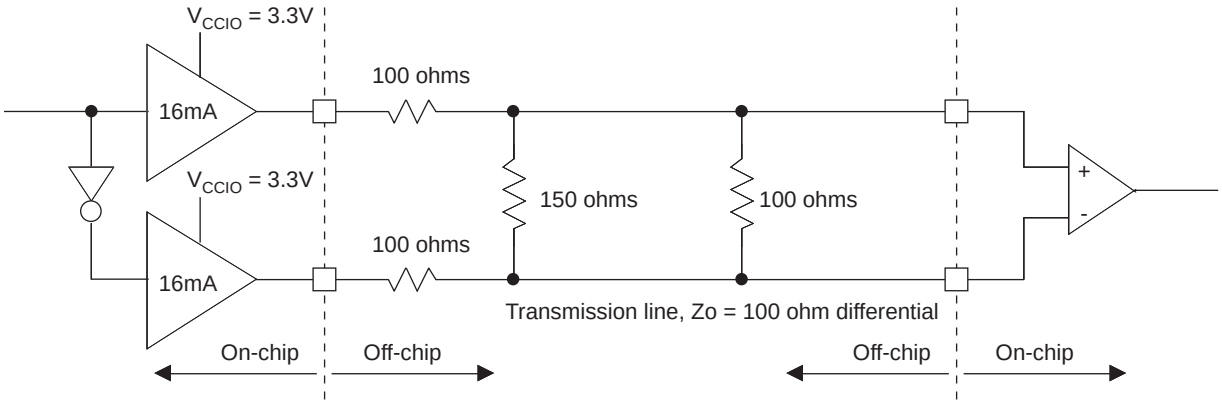


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	100	Ohms
R_P	Driver parallel resistor	150	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	Ohms
I_{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

MachXO External Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Global Clock without PLL)[1]									
t_{PD}	Best Case t_{PD} Through 1 LUT	LCMXO256	—	3.5	—	4.2	—	4.9	ns
		LCMXO640	—	3.5	—	4.2	—	4.9	ns
		LCMXO1200	—	3.6	—	4.4	—	5.1	ns
		LCMXO2280	—	3.6	—	4.4	—	5.1	ns
t_{CO}	Best Case Clock to Output - From PFU	LCMXO256	—	4.0	—	4.8	—	5.6	ns
		LCMXO640	—	4.0	—	4.8	—	5.7	ns
		LCMXO1200	—	4.3	—	5.2	—	6.1	ns
		LCMXO2280	—	4.3	—	5.2	—	6.1	ns
t_{SU}	Clock to Data Setup - To PFU	LCMXO256	1.3	—	1.6	—	1.8	—	ns
		LCMXO640	1.1	—	1.3	—	1.5	—	ns
		LCMXO1200	1.1	—	1.3	—	1.6	—	ns
		LCMXO2280	1.1	—	1.3	—	1.5	—	ns
t_{H}	Clock to Data Hold - To PFU	LCMXO256	-0.3	—	-0.3	—	-0.3	—	ns
		LCMXO640	-0.1	—	-0.1	—	-0.1	—	ns
		LCMXO1200	0.0	—	0.0	—	0.0	—	ns
		LCMXO2280	-0.4	—	-0.4	—	-0.4	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LCMXO256	—	600	—	550	—	500	MHz
		LCMXO640	—	600	—	550	—	500	MHz
		LCMXO1200	—	600	—	550	—	500	MHz
		LCMXO2280	—	600	—	550	—	500	MHz
t_{SKEW_PRI}	Global Clock Skew Across Device	LCMXO256	—	200	—	220	—	240	ps
		LCMXO640	—	200	—	220	—	240	ps
		LCMXO1200	—	220	—	240	—	260	ps
		LCMXO2280	—	220	—	240	—	260	ps

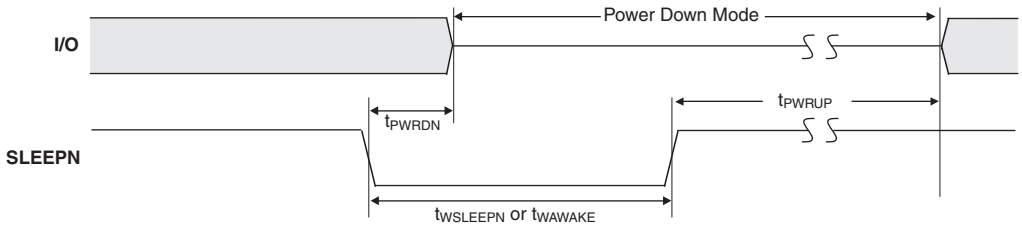
1. General timing numbers based on LVCMOS2.5V, 12 mA.

MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	SLEEPN Low to Power Down	All	—	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	LCMXO256	—	—	400	µs
		LCMXO640	—	—	600	µs
		LCMXO1200	—	—	800	µs
		LCMXO2280	—	—	1000	µs
$t_{WSLEEPN}$	SLEEPN Pulse Width	All	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	All	—	—	100	ns

Rev. A 0.19

Flash Download Time



Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	Minimum V_{CC} or V_{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO256	—	—	0.4	ms
		LCMXO640	—	—	0.6	ms
		LCMXO1200	—	—	0.8	ms
		LCMXO2280	—	—	1.0	ms

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

Rev. A 0.19

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
51	TDI	2	TDI		TDI	5	TDI		TDI	5	TDI	
52	VCC	-			VCC	-			VCC	-		
53	VCCAUX	-			VCCAUX	-			VCCAUX	-		
54	PB5A	2		T	PB6F	5			PB8F	5		
55	PB5B	2	PCLKT2_1***	C	PB7B	4	PCLK4_1***		PB10F	4	PCLK4_1***	
56	PB5D	2			PB7C	4		T	PB10C	4		T
57	PB6A	2		T	PB7D	4		C	PB10D	4		C
58	PB6B	2	PCLKT2_0***	C	PB7F	4	PCLK4_0***		PB10B	4	PCLK4_0***	
59	GND	-			GND	-			GND	-		
60	PB7C	2			PB9A	4		T	PB12A	4		T
61	PB7E	2			PB9B	4		C	PB12B	4		C
62	PB8A	2			PB9E	4			PB12E	4		
63	VCCIO2	2			VCCIO4	4			VCCIO4	4		
64	GNDIO2	2			GNDIO4	4			GNDIO4	4		
65	PB8C	2		T	PB10A	4		T	PB13A	4		T
66	PB8D	2		C	PB10B	4		C	PB13B	4		C
67	PB9A	2		T	PB10C	4		T	PB13C	4		T
68	PB9C	2		T	PB10D	4		C	PB13D	4		C
69	PB9B	2		C	PB10F	4			PB14D	4		
70**	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
71	PB9D	2		C	PB11C	4		T	PB16C	4		T
72	PB9F	2			PB11D	4		C	PB16D	4		C
73	PR11D	1		C	PR16B	3		C	PR20B	3		C
74	PR11B	1		C	PR16A	3		T	PR20A	3		T
75	PR11C	1		T	PR15B	3		C*	PR19B	3		C
76	PR10D	1		C	PR15A	3		T*	PR19A	3		T
77	PR11A	1		T	PR14D	3		C	PR17D	3		C
78	PR10B	1		C	PR14C	3		T	PR17C	3		T
79	PR10C	1		T	PR14B	3		C*	PR17B	3		C*
80	PR10A	1		T	PR14A	3		T*	PR17A	3		T*
81	PR9D	1			PR13D	3			PR16D	3		
82	VCCIO1	1			VCCIO3	3			VCCIO3	3		
83	GNDIO1	1			GNDIO3	3			GNDIO3	3		
84	PR9A	1			PR12B	3		C*	PR15B	3		C*
85	PR8C	1			PR12A	3		T*	PR15A	3		T*
86	PR8A	1			PR11B	3		C*	PR14B	3		C*
87	PR7D	1			PR11A	3		T*	PR14A	3		T*
88	GND	-			GND	-			GND	-		
89	PR7B	1		C	PR10B	3		C*	PR13B	3		C*
90	PR7A	1		T	PR10A	3		T*	PR13A	3		T*
91	PR6D	1		C	PR8B	2		C*	PR10B	2		C*
92	PR6C	1		T	PR8A	2		T*	PR10A	2		T*
93	VCC	-			VCC	-			VCC	-		
94	PR5D	1			PR6B	2		C*	PR8B	2		C*
95	PR5B	1			PR6A	2		T*	PR8A	2		T*
96	PR4D	1			PR5B	2		C*	PR7B	2		C*
97	PR4B	1		C	PR5A	2		T*	PR7A	2		T*
98	VCCIO1	1			VCCIO2	2			VCCIO2	2		
99	GNDIO1	1			GNDIO2	2			GNDIO2	2		
100	PR4A	1		T	PR4C	2			PR5C	2		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR8C	1		T	J13	PR11A	3		T*	J13	PR14A	3		T*
GND	GND	-			GND	GND	-			GND	GND	-		
K14	PR8B	1		C	K14	PR10D	3		C	K14	PR13D	3		C
J14	PR8A	1		T	J14	PR10C	3		T	J14	PR13C	3		T
K15	PR7D	1		C	K15	PR10B	3		C*	K15	PR13B	3		C*
J15	PR7C	1		T	J15	PR10A	3		T*	J15	PR13A	3		T*
-	-				GND	GNDIO3	3			GND	GNDIO3	3		
-	-				VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
K12	NC				K12	PR9D	3		C	K12	PR11D	3		C
J12	NC				J12	PR9C	3		T	J12	PR11C	3		T
J16	PR7B	1		C	J16	PR9B	3		C*	J16	PR11B	3		C*
H16	PR7A	1		T	H16	PR9A	3		T*	H16	PR11A	3		T*
H15	PR6B	1		C	H15	PR8D	2		C	H15	PR10D	2		C
G15	PR6A	1		T	G15	PR8C	2		T	G15	PR10C	2		T
H14	PR5D	1		C	H14	PR8B	2		C*	H14	PR10B	2		C*
G14	PR5C	1		T	G14	PR8A	2		T*	G14	PR10A	2		T*
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
H13	PR6D	1		C	H13	PR7D	2		C	H13	PR9D	2		C
H12	PR6C	1		T	H12	PR7C	2		T	H12	PR9C	2		T
G13	PR4D	1		C	G13	PR7B	2		C*	G13	PR9B	2		C*
G12	PR4C	1		T	G12	PR7A	2		T*	G12	PR9A	2		T*
G16	PR5B	1		C	G16	PR6D	2		C	G16	PR7D	2		C
F16	PR5A	1		T	F16	PR6C	2		T	F16	PR7C	2		T
F15	PR4B	1		C	F15	PR6B	2		C*	F15	PR7B	2		C*
E15	PR4A	1		T	E15	PR6A	2		T*	E15	PR7A	2		T*
E16	PR3B	1		C	E16	PR5D	2		C	E16	PR6D	2		C
D16	PR3A	1		T	D16	PR5C	2		T	D16	PR6C	2		T
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
D15	PR2D	1		C	D15	PR5B	2		C*	D15	PR6B	2		C*
C15	PR2C	1		T	C15	PR5A	2		T*	C15	PR6A	2		T*
C16	PR2B	1		C	C16	PR4D	2		C	C16	PR5D	2		C
B16	PR2A	1		T	B16	PR4C	2		T	B16	PR5C	2		T
F14	PR3D	1		C	F14	PR4B	2		C*	F14	PR5B	2		C*
E14	PR3C	1		T	E14	PR4A	2		T*	E14	PR5A	2		T*
-	-	-			-	-	-			GND	GND	-		
F12	NC				F12	PR3D	2		C	F12	PR4D	2		C
F13	NC				F13	PR3C	2		T	F13	PR4C	2		T
E12	NC				E12	PR3B	2		C*	E12	PR4B	2		C*
E13	NC				E13	PR3A	2		T*	E13	PR4A	2		T*
D13	NC				D13	PR2B	2		C	D13	PR3B	2		C*
D14	NC				D14	PR2A	2		T	D14	PR3A	2		T*
VCCIO0	VCCIO0	0			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO0	0			GND	GNDIO2	2			GND	GNDIO2	2		
GND	GNDIO0	0			GND	GNDIO1	1			GND	GNDIO1	1		
VCCIO0	VCCIO0	0			VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
B15	NC				B15	PT11D	1		C	B15	PT16D	1		C
A15	NC				A15	PT11C	1		T	A15	PT16C	1		T
C14	NC				C14	PT11B	1		C	C14	PT16B	1		C
B14	NC				B14	PT11A	1		T	B14	PT16A	1		T
C13	PT9F	0		C	C13	PT10F	1		C	C13	PT15D	1		C
B13	PT9E	0		T	B13	PT10E	1		T	B13	PT15C	1		T

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
T2	PL20B	6		C
P6	TMS	5	TMS	
V1	PB2A	5		T
U2	PB2B	5		C
T3	PB2C	5		T
N7	TCK	5	TCK	
R4	PB2D	5		C
R5	PB3A	5		T
T4	PB3B	5		C
VCC	VCC	-		
R6	PB3C	5		T
P7	PB3D	5		C
U3	PB4A	5		T
T5	PB4B	5		C
V2	PB4C	5		T
N8	TDO	5	TDO	
V3	PB4D	5		C
T6	PB5A	5		T
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		
U4	PB5B	5		C
P8	PB5C	5		T
T7	PB5D	5		C
V4	TDI	5	TDI	
R8	PB6A	5		T
N9	PB6B	5		C
U5	PB6C	5		T
V5	PB6D	5		C
U6	PB7A	5		T
VCC	VCC	-		
V6	PB7B	5		C
P9	PB7C	5		T
T8	PB7D	5		C
U7	PB8A	5		T
V7	PB8B	5		C
M10	VCCAUX	-		
U8	PB8C	5		T
V8	PB8D	5		C
VCCIO5	VCCIO5	5		
GND	GNDIO5	5		
T9	PB8E	5		T
U9	PB8F	5		C
V9	PB9A	4		T

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
V10	PB9B	4		C
N10	PB9C	4		T
R10	PB9D	4		C
P10	PB10F	4	PCLK4_1***	C
T10	PB10E	4		T
U10	PB10D	4		C
V11	PB10C	4		T
U11	PB10B	4	PCLK4_0***	C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
T11	PB10A	4		T
U12	PB11A	4		T
R11	PB11B	4		C
GND	GND	-		
T12	PB11C	4		T
P11	PB11D	4		C
V12	PB12A	4		T
V13	PB12B	4		C
R12	PB12C	4		T
N11	PB12D	4		C
U13	PB12E	4		T
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
V14	PB12F	4		C
T13	PB13A	4		T
P12	PB13B	4		C
R13	PB13C	4		T
N12	PB13D	4		C
V15	PB14A	4		T
U14	PB14B	4		C
V16	PB14C	4		T
GND	GND	-		
T14	PB14D	4		C
U15	PB15A	4		T
V17	PB15B	4		C
P13**	SLEEPN	-	SLEEPN	
T15	PB15D	4		
U16	PB16A	4		T
V18	PB16B	4		C
N13	PB16C	4		T
R14	PB16D	4		C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		

MachXO Family Data Sheet Ordering Information

June 2013 Data Sheet DS1002

Part Number Description

LCMXO XXXX X – X XXXXXX X XX

Device Family
MachXO PLD

Logic Capacity
256 LUTs = 256
640 LUTs = 640
1200 LUTs = 1200
2280 LUTs = 2280

Supply Voltage
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked as described.

Speed
3 = Slowest
4
5 = Fastest

Package
T100 = 100-pin TQFP
T144 = 144-pin TQFP
M100 = 100-ball csBGA
M132 = 132-ball csBGA
B256 = 256-ball caBGA
FT256 = 256-ball ftBGA
FT324 = 324-ball ftBGA

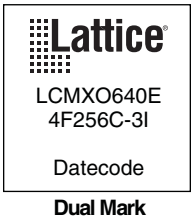
TN100 = 100-pin Lead-Free TQFP
TN144 = 144-pin Lead-Free TQFP
MN100 = 100-ball Lead-Free csBGA
MN132 = 132-ball Lead-Free csBGA
BN256 = 256-ball Lead-Free caBGA
FTN256 = 256-ball Lead-Free ftBGA
FTN324 = 324-ball Lead-Free ftBGA

Grade
C = Commercial
I = Industrial

ES = Engineering Sample
Blank = Production Device

Ordering Information

Note: MachXO devices are dual marked except the slowest commercial speed grade device.þFor example the commercial speed grade LCMXO640E-4F256C is also marked with industrial grade -3I grade.þThe slowest commercial speed grade does not have industrial markings.þ The markings appears as follows:



Dual Mark

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3T100I	256	1.2V	78	-3	TQFP	100	IND
LCMXO256E-4T100I	256	1.2V	78	-4	TQFP	100	IND
LCMXO256E-3M100I	256	1.2V	78	-3	csBGA	100	IND
LCMXO256E-4M100I	256	1.2V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3T100I	640	1.2V	74	-3	TQFP	100	IND
LCMXO640E-4T100I	640	1.2V	74	-4	TQFP	100	IND
LCMXO640E-3M100I	640	1.2V	74	-3	csBGA	100	IND
LCMXO640E-4M100I	640	1.2V	74	-4	csBGA	100	IND
LCMXO640E-3T144I	640	1.2V	113	-3	TQFP	144	IND
LCMXO640E-4T144I	640	1.2V	113	-4	TQFP	144	IND
LCMXO640E-3M132I	640	1.2V	101	-3	csBGA	132	IND
LCMXO640E-4M132I	640	1.2V	101	-4	csBGA	132	IND
LCMXO640E-3B256I	640	1.2V	159	-3	caBGA	256	IND
LCMXO640E-4B256I	640	1.2V	159	-4	caBGA	256	IND
LCMXO640E-3FT256I	640	1.2V	159	-3	ftBGA	256	IND
LCMXO640E-4FT256I	640	1.2V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100I	1200	1.2V	73	-3	TQFP	100	IND
LCMXO1200E-4T100I	1200	1.2V	73	-4	TQFP	100	IND
LCMXO1200E-3T144I	1200	1.2V	113	-3	TQFP	144	IND
LCMXO1200E-4T144I	1200	1.2V	113	-4	TQFP	144	IND
LCMXO1200E-3M132I	1200	1.2V	101	-3	csBGA	132	IND
LCMXO1200E-4M132I	1200	1.2V	101	-4	csBGA	132	IND
LCMXO1200E-3B256I	1200	1.2V	211	-3	caBGA	256	IND
LCMXO1200E-4B256I	1200	1.2V	211	-4	caBGA	256	IND
LCMXO1200E-3FT256I	1200	1.2V	211	-3	ftBGA	256	IND
LCMXO1200E-4FT256I	1200	1.2V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100I	2280	1.2V	73	-3	TQFP	100	IND
LCMXO2280E-4T100I	2280	1.2V	73	-4	TQFP	100	IND
LCMXO2280E-3T144I	2280	1.2V	113	-3	TQFP	144	IND
LCMXO2280E-4T144I	2280	1.2V	113	-4	TQFP	144	IND
LCMXO2280E-3M132I	2280	1.2V	101	-3	csBGA	132	IND
LCMXO2280E-4M132I	2280	1.2V	101	-4	csBGA	132	IND
LCMXO2280E-3B256I	2280	1.2V	211	-3	caBGA	256	IND
LCMXO2280E-4B256I	2280	1.2V	211	-4	caBGA	256	IND
LCMXO2280E-3FT256I	2280	1.2V	211	-3	ftBGA	256	IND
LCMXO2280E-4FT256I	2280	1.2V	211	-4	ftBGA	256	IND
LCMXO2280E-3FT324I	2280	1.2V	271	-3	ftBGA	324	IND
LCMXO2280E-4FT324I	2280	1.2V	271	-4	ftBGA	324	IND

Lead-Free Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	COM
LCMXO256C-4TN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	COM
LCMXO256C-5TN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free TQFP	100	COM
LCMXO256C-3MN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	COM
LCMXO256C-4MN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	COM
LCMXO256C-5MN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3TN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	COM
LCMXO640C-4TN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	COM
LCMXO640C-5TN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free TQFP	100	COM
LCMXO640C-3MN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	COM
LCMXO640C-4MN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	COM
LCMXO640C-5MN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free csBGA	100	COM
LCMXO640C-3TN144C	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO640C-4TN144C	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO640C-5TN144C	640	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO640C-3MN132C	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO640C-4MN132C	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO640C-5MN132C	640	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO640C-3BN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	COM
LCMXO640C-4BN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	COM
LCMXO640C-5BN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free caBGA	256	COM
LCMXO640C-3FTN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640C-4FTN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640C-5FTN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3TN100C	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200C-4TN100C	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200C-5TN100C	1200	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200C-3TN144C	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200C-4TN144C	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200C-5TN144C	1200	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200C-3MN132C	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200C-4MN132C	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200C-5MN132C	1200	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200C-3BN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200C-4BN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200C-5BN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200C-3FTN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200C-4FTN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200C-5FTN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-3TN100C	2280	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280C-4TN100C	2280	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280C-5TN100C	2280	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280C-3TN144C	2280	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO2280C-4TN144C	2280	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO2280C-5TN144C	2280	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO2280C-3MN132C	2280	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280C-4MN132C	2280	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280C-5MN132C	2280	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280C-3BN256C	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280C-4BN256C	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280C-5BN256C	2280	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280C-3FTN256C	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280C-4FTN256C	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280C-5FTN256C	2280	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280C-3FTN324C	2280	1.8V/2.5V/3.3V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280C-4FTN324C	2280	1.8V/2.5V/3.3V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280C-5FTN324C	2280	1.8V/2.5V/3.3V	271	-5	Lead-Free ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3TN100C	256	1.2V	78	-3	Lead-Free TQFP	100	COM
LCMXO256E-4TN100C	256	1.2V	78	-4	Lead-Free TQFP	100	COM
LCMXO256E-5TN100C	256	1.2V	78	-5	Lead-Free TQFP	100	COM
LCMXO256E-3MN100C	256	1.2V	78	-3	Lead-Free csBGA	100	COM
LCMXO256E-4MN100C	256	1.2V	78	-4	Lead-Free csBGA	100	COM
LCMXO256E-5MN100C	256	1.2V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN100C	640	1.2V	74	-3	Lead-Free TQFP	100	COM
LCMXO640E-4TN100C	640	1.2V	74	-4	Lead-Free TQFP	100	COM
LCMXO640E-5TN100C	640	1.2V	74	-5	Lead-Free TQFP	100	COM
LCMXO640E-3MN100C	640	1.2V	74	-3	Lead-Free csBGA	100	COM
LCMXO640E-4MN100C	640	1.2V	74	-4	Lead-Free csBGA	100	COM
LCMXO640E-5MN100C	640	1.2V	74	-5	Lead-Free csBGA	100	COM
LCMXO640E-3TN144C	640	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO640E-4TN144C	640	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO640E-5TN144C	640	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO640E-3MN132C	640	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO640E-4MN132C	640	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO640E-5MN132C	640	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO640E-3BN256C	640	1.2V	159	-3	Lead-Free caBGA	256	COM
LCMXO640E-4BN256C	640	1.2V	159	-4	Lead-Free caBGA	256	COM
LCMXO640E-5BN256C	640	1.2V	159	-5	Lead-Free caBGA	256	COM
LCMXO640E-3FTN256C	640	1.2V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640E-4FTN256C	640	1.2V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640E-5FTN256C	640	1.2V	159	-5	Lead-Free ftBGA	256	COM

Date	Version	Section	Change Summary
April 2006 (cont.)	02.0 (cont.)	Architecture (cont.)	"Top View of the MachXO1200 Device" figure updated.
			"Top View of the MachXO640 Device" figure updated.
			"Top View of the MachXO256 Device" figure updated.
			"Slice Diagram" figure updated.
			Slice Signal Descriptions table updated.
			Routing section updated.
			sysCLOCK Phase Lockecd Loops (PLLs) section updated.
			PLL Diagram updated.
			PLL Signal Descriptions table updated.
			sysMEM Memory section has been updated.
			PIO Groups section has been updated.
			PIO section has been updated.
			MachXO PIO Block Diagram updated.
			Supported Input Standards table updated.
			MachXO Configuration and Programming diagram updated.
		DC and Switching Characteristics	Recommended Operating Conditions table - footnotes updated.
			MachXO256 and MachXO640 Hot Socketing Specifications - footnotes updated.
			Added MachXO1200 and MachXO2280 Hot Socketing Specifications table.
			DC Electrical Characteristics, footnotes have been updated.
			Supply Current (Sleep Mode) table has been updated, removed "4W" references. Footnotes have been updated.
			Supply Current (Standby) table and associated footnotes updated.
			Intialization Supply Current table and footnotes updated.
			Programming and Erase Flash Supply Current table and associated footnotes have been updatd.
			Register-to-Register Performance table updated (rev. A 0.19).
			MachXO External Switching Characteristics updated (rev. A 0.19).
			MachXO Internal Timing Parameters updated (rev. A 0.19).
			MachXO Family Timing Adders updated (rev. A 0.19).
			sysCLOCK Timing updated (rev. A 0.19).
			MachXO "C" Sleep Mode Timing updated (A 0.19).
			JTAG Port Timing Specification updated (rev. A 0.19).
			Test Fixture Required Components table updated.
		Pinout Information	Signal Descriptions have been updated.
			Pin Information Summary has been updated. Footnote has been added.
			Power Supply and NC Connection table has been updated.
			Logic Signal Connections have been updated (PCLKTx_x --> PCLKx_x)
		Ordering Information	Removed "4W" references.
			Added 256-ftBGA Ordering Part Numbers for MachXO640.
May 2006	02.1	Pinout Information	Removed [LOC][0]_PLL_RST from Signal Description table.
			PCLK footnote has been added to all appropriate pins.
August 2006	02.2	Multiple	Removed 256 fpBGA information for MachXO640.

Date	Version	Section	Change Summary
November 2006	02.3	DC and Switching Characteristics	Corrections to MachXO "C" Sleep Mode Timing table - value for $t_{WSLEEPN}$ (400ns) changed from max. to min. Value for t_{WAWAKE} (100ns) changed from min. to max.
			Added Flash Download Time table.
December 2006	02.4	Architecture	EBR Asynchronous Reset section added.
		Pinout Information	Power Supply and NC table: Pin/Ball orientation footnotes added.
February 2007	02.5	Architecture	Updated EBR Asynchronous Reset section.
August 2007	02.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table.
November 2007	02.7	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
June 2009	02.8	Introduction	Added 0.8-mm 256-pin caBGA package to MachXO Family Selection Guide table.
		Pinout Information	Added Logic Signal Connections table for 0.8-mm 256-pin caBGA package.
		Ordering Information	Updated Part Number Description diagram and Ordering Part Number tables with 0.8-mm 256-pin caBGA package information.
July 2010	02.9	DC and Switching Characteristics	Updated sysCLOCK PLL Timing table.
June 2013	03.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	MachXO1200 and MachXO2280 Hot Socketing Specifications table – Removed footnote 4.
			Added MachXO Programming/Erase Specifications table.