Lattice Semiconductor Corporation - LCMXO2280C-3FT256C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	285
Number of Logic Elements/Cells	2280
Total RAM Bits	28262
Number of I/O	211
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280c-3ft256c

MachXO Family Data Sheet Introduction

June 2013 Data Sheet DS1002

Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- **Sleep Mode**
  - Allows up to 100x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **High I/O to Logic Density**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.7 Kbits distributed RAM
  - Dedicated FIFO control logic
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide, and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - Onboard oscillator
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
  - IEEE 1532 compliant in-system programming

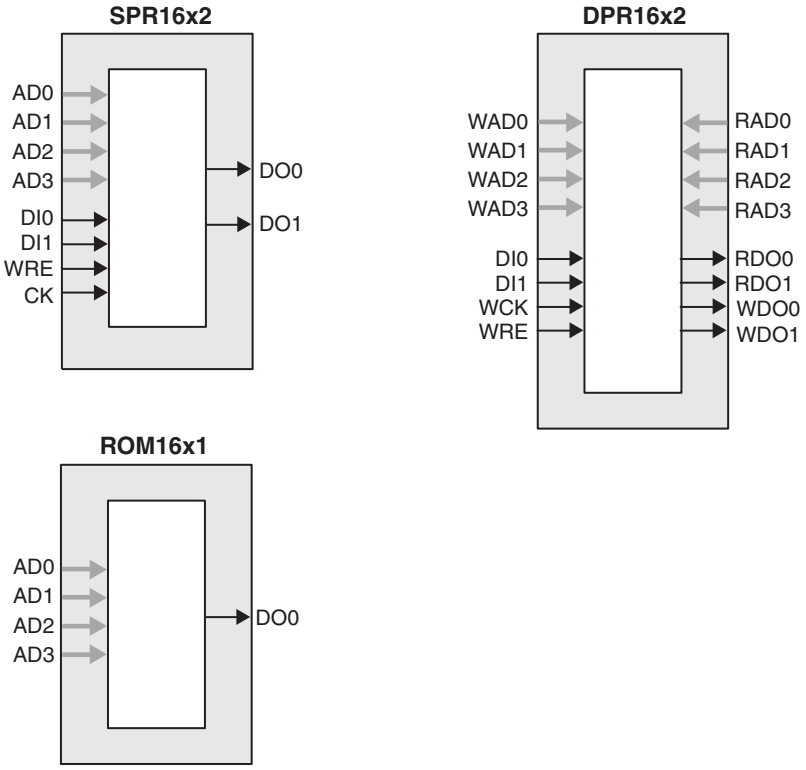
Introduction

The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, and control logic. These devices bring together the best features of CPLD and FPGA devices on a single chip.

Table 1-1. MachXO Family Selection Guide

Device	LCMXO256	LCMXO640	LCMXO1200	LCMXO2280
LUTs	256	640	1200	2280
Dist. RAM (Kbits)	2.0	6.1	6.4	7.7
EBR SRAM (Kbits)	0	0	9.2	27.6
Number of EBR SRAM Blocks (9 Kbits)	0	0	1	3
V_{CC} Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
Number of PLLs	0	0	1	2
Max. I/O	78	159	211	271
Packages				
100-pin TQFP (14x14 mm)	78	74	73	73
144-pin TQFP (20x20 mm)		113	113	113
100-ball csBGA (8x8 mm)	78	74		
132-ball csBGA (8x8 mm)		101	101	101
256-ball caBGA (14x14 mm)		159	211	211
256-ball ftBGA (17x17 mm)		159	211	211
324-ball ftBGA (19x19 mm)				271

Figure 2-6. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

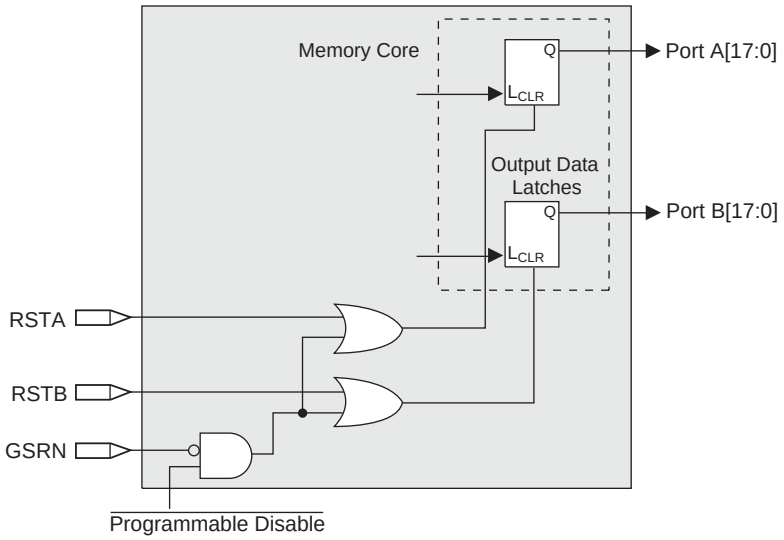
Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

Figure 2-13. Memory Core Reset

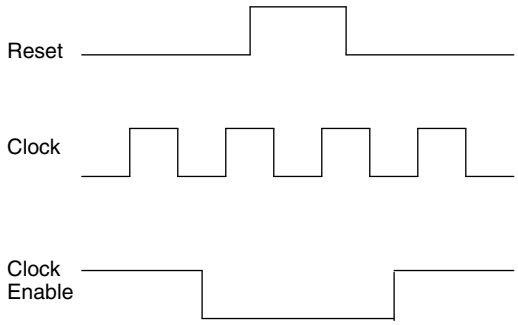


For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPReset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled

PIO Groups

On the MachXO devices, PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four IOs are placed on the left and right sides of the device while PIO groups with six IOs are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and PADs.

On all MachXO devices, two adjacent PIOs can be joined to provide a complementary Output driver pair. The I/O pin pairs are labeled as "T" and "C" to distinguish between the true and complement pins.

The MachXO1200 and MachXO2280 devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. In addition, half of the PIO pairs on the left and right sides of these devices can be configured as LVDS transmit/receive pairs. PIOs on the top of these larger devices also provide PCI support.

Figure 2-15. Group of Four Programmable I/O Cells

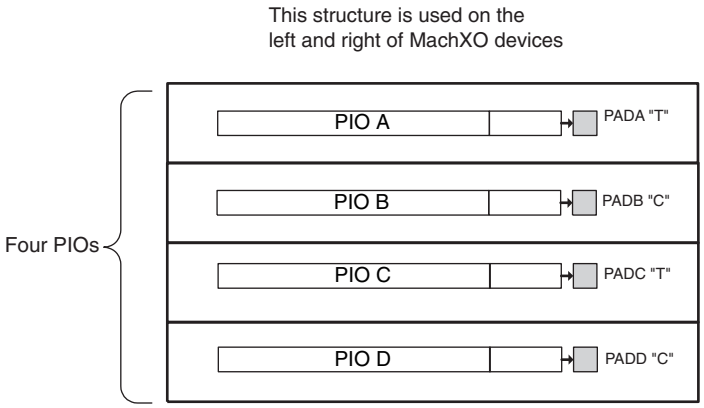
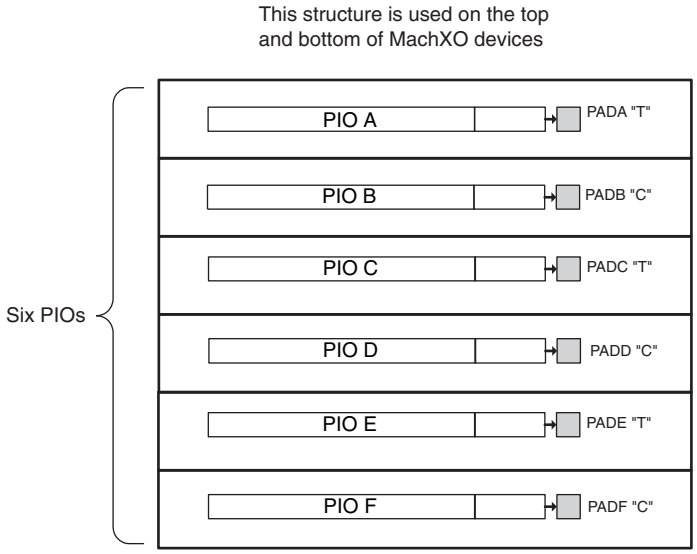


Figure 2-16. Group ofpSix Programmable I/O Cells



PIO

The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast

Table 2-10. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Typ.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA	3.3
LVCMOS33	4mA, 8mA, 12mA, 14mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 14mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 14mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33[3]	N/A	3.3
Differential Interfaces		
LVDS[1, 2]	N/A	2.5
BLVDS, RSDS[2]	N/A	2.5
LVPECL[2]	N/A	3.3

1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top Banks of MachXO1200 and MachXO2280 devices only.

sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the MachXO1200 and MachXO2280 (two Banks per side). The MachXO640 has four Banks (one Bank per side). The smallest member of this family, the MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V_{CCIO}) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

MachXO256 and MachXO640 Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX}, and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) and $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

MachXO1200 and MachXO2280 Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Non-LVDS General Purpose sysIOs						
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	—	—	+/-1000	µA
LVDS General Purpose sysIOs						
I_{DK_LVDS}	Input or I/O Leakage Current	$V_{IN} \le V_{CCIO}$	—	—	+/-1000	µA
		$V_{IN} > V_{CCIO}$	—	35	—	mA

1. Insensitive to sequence of V_{CC}, V_{CCAUX}, and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX), and $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4, 5]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}[3]	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Not applicable to SLEEPN pin.
5. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For MachXO1200 and MachXO2280 true LVDS output pins, V_{IH} must be less than or equal to V_{CCIO}.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465
LVCMOS 2.5	2.375	2.5	2.625
LVCMOS 1.8	1.71	1.8	1.89
LVCMOS 1.5	1.425	1.5	1.575
LVCMOS 1.2	1.14	1.2	1.26
LVTTL	3.135	3.3	3.465
PCI[3]	3.135	3.3	3.465
LVDS[1, 2]	2.375	2.5	2.625
LVPECL[1]	3.135	3.3	3.465
BLVDS[1]	2.375	2.5	2.625
RSDS[1]	2.375	2.5	2.625

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers
3. Input on the top bank of the MachXO1200 and MachXO2280 only.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	2.4	16	-16
					0.4	V_{CCIO} - 0.4	12, 8, 4	-12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“C” Version)	-0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“E” Version)	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

MachXO External Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Global Clock without PLL)[1]									
t_{PD}	Best Case t_{PD} Through 1 LUT	LCMXO256	—	3.5	—	4.2	—	4.9	ns
		LCMXO640	—	3.5	—	4.2	—	4.9	ns
		LCMXO1200	—	3.6	—	4.4	—	5.1	ns
		LCMXO2280	—	3.6	—	4.4	—	5.1	ns
t_{CO}	Best Case Clock to Output - From PFU	LCMXO256	—	4.0	—	4.8	—	5.6	ns
		LCMXO640	—	4.0	—	4.8	—	5.7	ns
		LCMXO1200	—	4.3	—	5.2	—	6.1	ns
		LCMXO2280	—	4.3	—	5.2	—	6.1	ns
t_{SU}	Clock to Data Setup - To PFU	LCMXO256	1.3	—	1.6	—	1.8	—	ns
		LCMXO640	1.1	—	1.3	—	1.5	—	ns
		LCMXO1200	1.1	—	1.3	—	1.6	—	ns
		LCMXO2280	1.1	—	1.3	—	1.5	—	ns
t_{H}	Clock to Data Hold - To PFU	LCMXO256	-0.3	—	-0.3	—	-0.3	—	ns
		LCMXO640	-0.1	—	-0.1	—	-0.1	—	ns
		LCMXO1200	0.0	—	0.0	—	0.0	—	ns
		LCMXO2280	-0.4	—	-0.4	—	-0.4	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LCMXO256	—	600	—	550	—	500	MHz
		LCMXO640	—	600	—	550	—	500	MHz
		LCMXO1200	—	600	—	550	—	500	MHz
		LCMXO2280	—	600	—	550	—	500	MHz
t_{SKEW_PRI}	Global Clock Skew Across Device	LCMXO256	—	200	—	220	—	240	ps
		LCMXO640	—	200	—	220	—	240	ps
		LCMXO1200	—	220	—	240	—	260	ps
		LCMXO2280	—	220	—	240	—	260	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA.

MachXO Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25[4]	LVDS	0.44	0.53	0.61	ns
BLVDS25[4]	BLVDS	0.44	0.53	0.61	ns
LVPECL33[4]	LVPECL	0.42	0.50	0.59	ns
LVTTL33	LVTTL	0.01	0.01	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	0.01	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	0.07	0.08	0.10	ns
LVCMOS15	LVCMOS 1.5	0.14	0.17	0.19	ns
LVCMOS12	LVCMOS 1.2	0.40	0.48	0.56	ns
PCI33[4]	PCI	0.01	0.01	0.01	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E	-0.13	-0.15	-0.18	ns
LVDS25[4]	LVDS 2.5	-0.21	-0.26	-0.30	ns
BLVDS25	BLVDS 2.5	-0.03	-0.03	-0.04	ns
LVPECL33	LVPECL 3.3	0.04	0.04	0.05	ns
LVTTL33_4mA	LVTTL 4mA drive	0.04	0.04	0.05	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.07	0.08	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.01	-0.01	-0.01	ns
LVTTL33_16mA	LVTTL 16mA drive	0.50	0.60	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.04	0.04	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.06	0.07	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	-0.01	-0.01	-0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14mA drive	0.50	0.60	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.05	0.06	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.10	0.12	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14mA drive	0.34	0.40	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.11	0.13	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.05	0.06	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	-0.06	-0.07	-0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14mA drive	0.06	0.07	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.15	0.19	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.05	0.06	0.07	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.26	0.31	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.05	0.06	0.07	ns
PCI33[4]	PCI33	1.85	2.22	2.59	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

Rev. A 0.19

sysCLOCK PLL Timing

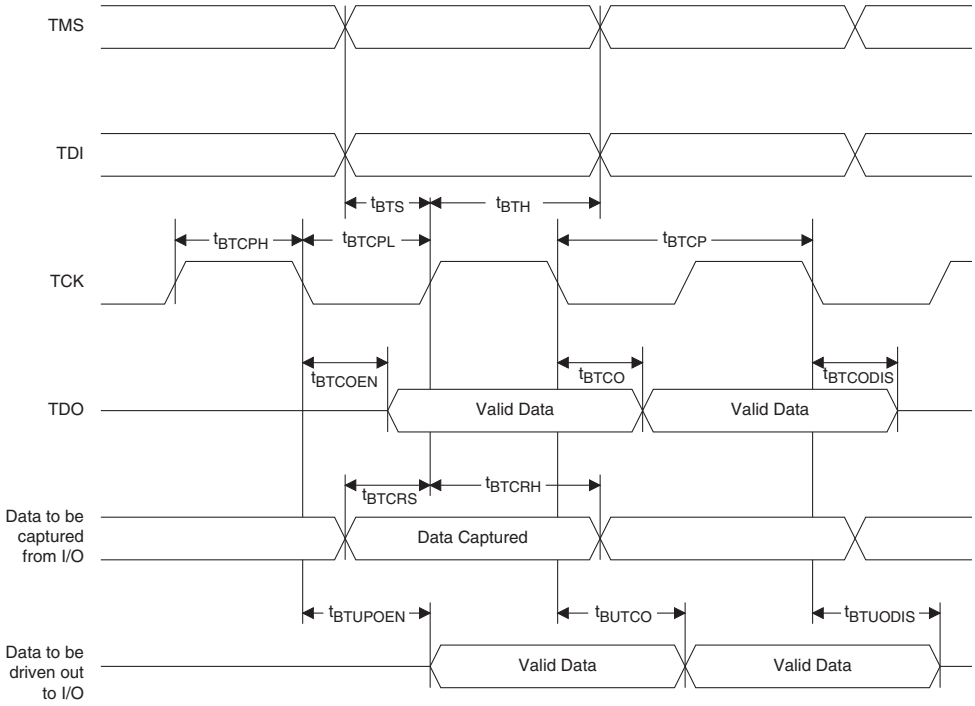
Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6]	18	25	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f_{VCO}	PLL VCO Frequency		420	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6]	18	25	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	55	%
t_{PH}[4]	Output Phase Accuracy		—	0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	+/-120	ps
		f_{OUT} < 100 MHz	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	1	—	ns
t_{LOCK}[2]	PLL Lock-in Time		—	150	µs
t_{PA}	Programmable Delay Unit		100	450	ps
t_{IPJIT}	Input Clock Period Jitter	$f_{OUT} \geq$ 100 MHz	—	+/-200	ps
		f_{OUT} < 100 MHz	—	0.02	UI
t_{FBKDLY}	External Feedback Delay		—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST Pulse Width		10	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output.
5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.
6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.

Rev. A 0.19

Figure 3-5. JTAG Port Timing Waveforms



LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	1		T	PL2A	3		T
2	PL2B	1		C	PL2C	3		T
3	PL3A	1		T	PL2B	3		C
4	PL3B	1		C	PL2D	3		C
5	PL3C	1		T	PL3A	3		T
6	PL3D	1		C	PL3B	3		C
7	PL4A	1		T	PL3C	3		T
8	PL4B	1		C	PL3D	3		C
9	PL5A	1		T	PL4A	3		
10	VCCIO1	1			VCCIO3	3		
11	PL5B	1		C	PL4C	3		T
12	GNDIO1	1			GNDIO3	3		
13	PL5C	1		T	PL4D	3		C
14	PL5D	1	GSRN	C	PL5B	3	GSRN	
15	PL6A	1		T	PL7B	3		
16	PL6B	1	TSALL	C	PL8C	3	TSALL	T
17	PL7A	1		T	PL8D	3		C
18	PL7B	1		C	PL9A	3		
19	PL7C	1		T	PL9C	3		
20	PL7D	1		C	PL10A	3		
21	PL8A	1		T	PL10C	3		
22	PL8B	1		C	PL11A	3		
23	PL9A	1		T	PL11C	3		
24	VCCIO1	1			VCCIO3	3		
25	GNDIO1	1			GNDIO3	3		
26	TMS	1	TMS		TMS	2	TMS	
27	PL9B	1		C	PB2C	2		
28	TCK	1	TCK		TCK	2	TCK	
29	PB2A	1		T	VCCIO2	2		
30	PB2B	1		C	GNDIO2	2		
31	TDO	1	TDO		TDO	2	TDO	
32	PB2C	1		T	PB4C	2		
33	TDI	1	TDI		TDI	2	TDI	
34	PB2D	1		C	PB4E	2		
35	VCC	-			VCC	-		
36	PB3A	1	PCLK1_1**	T	PB5B	2	PCLK2_1**	
37	PB3B	1		C	PB5D	2		
38	PB3C	1	PCLK1_0**	T	PB6B	2	PCLK2_0**	
39	PB3D	1		C	PB6C	2		
40	GND	-			GND	-		
41	VCCIO1	1			VCCIO2	2		
42	GNDIO1	1			GNDIO2	2		

LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA

LCMXO256					LCMXO640				
Ball Number	Ball Function	Bank	Dual Function	Differen-tial	Ball Number	Ball Function	Bank	Dual Function	Differen-tial
B1	PL2A	1		T	B1	PL2A	3		T
C1	PL2B	1		C	C1	PL2C	3		T
D2	PL3A	1		T	D2	PL2B	3		C
D1	PL3B	1		C	D1	PL2D	3		C
C2	PL3C	1		T	C2	PL3A	3		T
E1	PL3D	1		C	E1	PL3B	3		C
E2	PL4A	1		T	E2	PL3C	3		T
F1	PL4B	1		C	F1	PL3D	3		C
F2	PL5A	1		T	F2	PL4A	3		
G2	PL5B	1		C	G2	PL4C	3		T
H1	GNDIO1	1			H1	GNDIO3	3		
H2	PL5C	1		T	H2	PL4D	3		C
J1	PL5D	1	GSRN	C	J1	PL5B	3	GSRN	
J2	PL6A	1		T	J2	PL7B	3		
K1	PL6B	1	TSALL	C	K1	PL8C	3	TSALL	T
K2	PL7A	1		T	K2	PL8D	3		C
L1	PL7B	1		C	L1	PL9A	3		
L2	PL7C	1		T	L2	PL9C	3		
M1	PL7D	1		C	M1	PL10A	3		
M2	PL8A	1		T	M2	PL10C	3		
N1	PL8B	1		C	N1	PL11A	3		
M3	PL9A	1		T	M3	PL11C	3		
N2	GNDIO1	1			N2	GNDIO3	3		
P2	TMS	1	TMS		P2	TMS	2	TMS	
P3	PL9B	1		C	P3	PB2C	2		
N4	TCK	1	TCK		N4	TCK	2	TCK	
P4	PB2A	1		T	P4	VCCIO2	2		
N3	PB2B	1		C	N3	GNDIO2	2		
P5	TDO	1	TDO		P5	TDO	2	TDO	
N5	PB2C	1		T	N5	PB4C	2		
P6	TDI	1	TDI		P6	TDI	2	TDI	
N6	PB2D	1		C	N6	PB4E	2		
P7	VCC	-			P7	VCC	-		
N7	PB3A	1	PCLK1_1**	T	N7	PB5B	2	PCLK2_1**	
P8	PB3B	1		C	P8	PB5D	2		
N8	PB3C	1	PCLK1_0**	T	N8	PB6B	2	PCLK2_0**	
P9	PB3D	1		C	P9	PB6C	2		
N10	GNDIO1	1			N10	GNDIO2	2		
P11	PB4A	1		T	P11	PB8B	2		
N11	PB4B	1		C	N11	PB8C	2		T
P12	PB4C	1		T	P12	PB8D	2		C
N12	PB4D	1		C	N12	PB9A	2		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
M9	PB7B	2		C	M9	PB9B	4		C	M9	PB12B	4		C
N10	PB7E	2		T	N10	PB9C	4		T	N10	PB12C	4		T
P10	PB7F	2		C	P10	PB9D	4		C	P10	PB12D	4		C
N11	GNDIO2	2			N11	GNDIO4	4			N11	GNDIO4	4		
P11	PB8C	2		T	P11	PB10A	4		T	P11	PB13C	4		T
M11	PB8D	2		C	M11	PB10B	4		C	M11	PB13D	4		C
P12	PB9C	2		T	P12	PB10C	4			P12	PB15B	4		
P13	PB9D	2		C	P13	PB11C	4		T	P13	PB16C	4		T
N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB11D	4		C	P14	PB16D	4		C
N14	PR11D	1		C	N14	PR16B	3		C	N14	PR19B	3		C
M14	PR11C	1		T	M14	PR15B	3		C*	M14	PR18B	3		C*
N13	PR11B	1		C	N13	PR16A	3		T	N13	PR19A	3		T
M12	PR11A	1		T	M12	PR15A	3		T*	M12	PR18A	3		T*
M13	PR10B	1		C	M13	PR14B	3		C*	M13	PR17B	3		C*
L14	PR10A	1		T	L14	PR14A	3		T*	L14	PR17A	3		T*
L13	GNDIO1	1			L13	GNDIO3	3			L13	GNDIO3	3		
K14	PR8D	1		C	K14	PR12B	3		C*	K14	PR15B	3		C*
K13	PR8C	1		T	K13	PR12A	3		T*	K13	PR15A	3		T*
K12	PR8B	1		C	K12	PR11B	3		C*	K12	PR14B	3		C*
J13	PR8A	1		T	J13	PR11A	3		T*	J13	PR14A	3		T*
J12	PR7C	1			J12	PR10B	3		C*	J12	PR13B	3		C*
H14	PR7B	1		C	H14	PR10A	3		T*	H14	PR13A	3		T*
H13	PR7A	1		T	H13	PR9B	3		C*	H13	PR11B	3		C*
H12	PR6D	1		C	H12	PR9A	3		T*	H12	PR11A	3		T*
G13	PR6C	1		T	G13	PR8B	2		C*	G13	PR10B	2		C*
G14	PR6B	1			G14	PR8A	2		T*	G14	PR10A	2		T*
G12	VCC	-			G12	VCC	-			G12	VCC	-		
F14	PR5D	1		C	F14	PR6C	2			F14	PR8C	2		
F13	PR5C	1		T	F13	PR6B	2		C*	F13	PR8B	2		C*
F12	PR4D	1		C	F12	PR6A	2		T*	F12	PR8A	2		T*
E13	PR4C	1		T	E13	PR5B	2		C*	E13	PR7B	2		C*
E14	PR4B	1			E14	PR5A	2		T*	E14	PR7A	2		T*
D13	GNDIO1	1			D13	GNDIO2	2			D13	GNDIO2	2		
D14	PR3D	1		C	D14	PR4B	2		C*	D14	PR5B	2		C*
D12	PR3C	1		T	D12	PR4A	2		T*	D12	PR5A	2		T*
C14	PR2D	1		C	C14	PR3D	2		C	C14	PR4D	2		C
B14	PR2C	1		T	B14	PR2B	2		C	B14	PR3B	2		C*
C13	PR2B	1		C	C13	PR3C	2		T	C13	PR4C	2		T
A14	PR2A	1		T	A14	PR2A	2		T	A14	PR3A	2		T*
A13	PT9F	0		C	A13	PT11D	1		C	A13	PT16D	1		C
A12	PT9E	0		T	A12	PT11B	1		C	A12	PT16B	1		C
B13	PT9D	0		C	B13	PT11C	1		T	B13	PT16C	1		T
B12	PT9C	0		T	B12	PT10F	1			B12	PT15D	1		
C12	PT9B	0		C	C12	PT11A	1		T	C12	PT16A	1		T
A11	PT9A	0		T	A11	PT10D	1		C	A11	PT14B	1		C
C11	PT8C	0			C11	PT10C	1		T	C11	PT14A	1		T
A10	GNDIO0	0			A10	GNDIO1	1			A10	GNDIO1	1		
B10	PT7F	0		C	B10	PT9F	1		C	B10	PT12F	1		C
C10	PT7E	0		T	C10	PT9E	1		T	C10	PT12E	1		T

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1***	C	A8	PT7D	1	PCLK1_1***		A8	PT10B	1	PCLK1_1***	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0***	C	C8	PT6F	0	PCLK1_0***		C8	PT9B	1	PCLK1_0***	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	-			A7	VCCAUX	-			A7	VCCAUX	-		
C7	VCC	-			C7	VCC	-			C7	VCC	-		
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	-			F1	GND	-			F1	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
C9	GND	-			C9	GND	-			C9	GND	-		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

*Supports true LVDS outputs.
**NC for “E” devices.
***Primary clock inputs arer single-ended.

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	3		T	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2C	3		T	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL2B	3		C	PL3A	7		T*	PL3A	7		T*
4	PL3A	3		T	PL3B	7		C*	PL3B	7		C*
5	PL2D	3		C	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
6	PL3B	3		C	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
7	PL3C	3		T	PL4A	7		T*	PL4A	7		T*
8	PL3D	3		C	PL4B	7		C*	PL4B	7		C*
9	PL4A	3			PL4C	7			PL4C	7		
10	VCCIO3	3			VCCIO7	7			VCCIO7	7		
11	GNDIO3	3			GNDIO7	7			GNDIO7	7		
12	PL4D	3			PL5C	7			PL6C	7		
13	PL5A	3		T	PL6A	7		T*	PL7A	7		T*
14	PL5B	3	GSRN	C	PL6B	7	GSRN	C*	PL7B	7	GSRN	C*
15	PL5D	3			PL6D	7			PL7D	7		
16	GND	-			GND	-			GND	-		
17	PL6C	3		T	PL7C	7		T	PL9C	7		T
18	PL6D	3		C	PL7D	7		C	PL9D	7		C
19	PL7A	3		T	PL10A	6		T*	PL13A	6		T*
20	PL7B	3		C	PL10B	6		C*	PL13B	6		C*
21	VCC	-			VCC	-			VCC	-		
22	PL8A	3		T	PL11A	6		T*	PL13D	6		
23	PL8B	3		C	PL11B	6		C*	PL14D	6		C
24	PL8C	3	TSALL		PL11C	6	TSALL		PL14C	6	TSALL	T
25	PL9C	3		T	PL12B	6			PL15B	6		
26	VCCIO3	3			VCCIO6	6			VCCIO6	6		
27	GNDIO3	3			GNDIO6	6			GNDIO6	6		
28	PL9D	3		C	PL13D	6			PL16D	6		
29	PL10A	3		T	PL14A	6	LLM0_PLLT_FB_A	T*	PL17A	6	LLM0_PLLT_FB_A	T*
30	PL10B	3		C	PL14B	6	LLM0_PLLC_FB_A	C*	PL17B	6	LLM0_PLLC_FB_A	C*
31	PL10C	3		T	PL14C	6		T	PL17C	6		T
32	PL11A	3		T	PL14D	6		C	PL17D	6		C
33	PL10D	3		C	PL15A	6	LLM0_PLLT_IN_A	T*	PL18A	6	LLM0_PLLT_IN_A	T*
34	PL11C	3		T	PL15B	6	LLM0_PLLC_IN_A	C*	PL18B	6	LLM0_PLLC_IN_A	C*
35	PL11B	3		C	PL16A	6		T	PL19A	6		T
36	PL11D	3		C	PL16B	6		C	PL19B	6		C
37	GNDIO2	2			GNDIO5	5			GNDIO5	5		
38	VCCIO2	2			VCCIO5	5			VCCIO5	5		
39	TMS	2	TMS		TMS	5	TMS		TMS	5	TMS	
40	PB2C	2			PB2C	5		T	PB2A	5		T
41	PB3A	2		T	PB2D	5		C	PB2B	5		C
42	TCK	2	TCK		TCK	5	TCK		TCK	5	TCK	
43	PB3B	2		C	PB3A	5		T	PB3A	5		T
44	PB3C	2		T	PB3B	5		C	PB3B	5		C
45	PB3D	2		C	PB4A	5		T	PB4A	5		T
46	PB4A	2		T	PB4B	5		C	PB4B	5		C
47	TDO	2	TDO		TDO	5	TDO		TDO	5	TDO	
48	PB4B	2		C	PB4D	5			PB4D	5		
49	PB4C	2		T	PB5A	5		T	PB5A	5		T
50	PB4D	2		C	PB5B	5		C	PB5B	5		C

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
A10	PT8E	0		T
VCCIO0	VCCIO0	0		
GND	GNDIO0	0		
A9	PT8D	0		C
C9	PT8C	0		T
B9	PT8B	0		C
F9	VCCAUX	-		
A8	PT8A	0		T
B8	PT7D	0		C
C8	PT7C	0		T
VCC	VCC	-		
A7	PT7B	0		C
B7	PT7A	0		T
A6	PT6A	0		T
B6	PT6B	0		C
D8	PT6C	0		T
F8	PT6D	0		C
C7	PT6E	0		T
E8	PT6F	0		C
D7	PT5D	0		C
VCCIO0	VCCIO0	0		
GND	GNDIO0	0		
E7	PT5C	0		T
A5	PT5B	0		C
C6	PT5A	0		T
B5	PT4A	0		T
A4	PT4B	0		C
D6	PT4C	0		T
F7	PT4D	0		C
B4	PT4E	0		T
GND	GND	-		
C5	PT4F	0		C
F6	PT3D	0		C
E5	PT3C	0		T
E6	PT3B	0		C
D5	PT3A	0		T
A3	PT2D	0		C
C4	PT2C	0		T
A2	PT2B	0		C
B2	PT2A	0		T
VCCIO0	VCCIO0	0		
GND	GNDIO0	0		
E14	GND	-		

Conventional Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM
LCMXO256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM
LCMXO256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM
LCMXO256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM
LCMXO256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM
LCMXO256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMXO640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMXO640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMXO640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMXO640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMXO640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMXO640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMXO640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMXO640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMXO640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMXO640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMXO640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMXO1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMXO1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMXO1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMXO1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMXO1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMXO1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMXO1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMXO1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3T100I	256	1.2V	78	-3	TQFP	100	IND
LCMXO256E-4T100I	256	1.2V	78	-4	TQFP	100	IND
LCMXO256E-3M100I	256	1.2V	78	-3	csBGA	100	IND
LCMXO256E-4M100I	256	1.2V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3T100I	640	1.2V	74	-3	TQFP	100	IND
LCMXO640E-4T100I	640	1.2V	74	-4	TQFP	100	IND
LCMXO640E-3M100I	640	1.2V	74	-3	csBGA	100	IND
LCMXO640E-4M100I	640	1.2V	74	-4	csBGA	100	IND
LCMXO640E-3T144I	640	1.2V	113	-3	TQFP	144	IND
LCMXO640E-4T144I	640	1.2V	113	-4	TQFP	144	IND
LCMXO640E-3M132I	640	1.2V	101	-3	csBGA	132	IND
LCMXO640E-4M132I	640	1.2V	101	-4	csBGA	132	IND
LCMXO640E-3B256I	640	1.2V	159	-3	caBGA	256	IND
LCMXO640E-4B256I	640	1.2V	159	-4	caBGA	256	IND
LCMXO640E-3FT256I	640	1.2V	159	-3	ftBGA	256	IND
LCMXO640E-4FT256I	640	1.2V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100I	1200	1.2V	73	-3	TQFP	100	IND
LCMXO1200E-4T100I	1200	1.2V	73	-4	TQFP	100	IND
LCMXO1200E-3T144I	1200	1.2V	113	-3	TQFP	144	IND
LCMXO1200E-4T144I	1200	1.2V	113	-4	TQFP	144	IND
LCMXO1200E-3M132I	1200	1.2V	101	-3	csBGA	132	IND
LCMXO1200E-4M132I	1200	1.2V	101	-4	csBGA	132	IND
LCMXO1200E-3B256I	1200	1.2V	211	-3	caBGA	256	IND
LCMXO1200E-4B256I	1200	1.2V	211	-4	caBGA	256	IND
LCMXO1200E-3FT256I	1200	1.2V	211	-3	ftBGA	256	IND
LCMXO1200E-4FT256I	1200	1.2V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100I	2280	1.2V	73	-3	TQFP	100	IND
LCMXO2280E-4T100I	2280	1.2V	73	-4	TQFP	100	IND
LCMXO2280E-3T144I	2280	1.2V	113	-3	TQFP	144	IND
LCMXO2280E-4T144I	2280	1.2V	113	-4	TQFP	144	IND
LCMXO2280E-3M132I	2280	1.2V	101	-3	csBGA	132	IND
LCMXO2280E-4M132I	2280	1.2V	101	-4	csBGA	132	IND
LCMXO2280E-3B256I	2280	1.2V	211	-3	caBGA	256	IND
LCMXO2280E-4B256I	2280	1.2V	211	-4	caBGA	256	IND
LCMXO2280E-3FT256I	2280	1.2V	211	-3	ftBGA	256	IND
LCMXO2280E-4FT256I	2280	1.2V	211	-4	ftBGA	256	IND
LCMXO2280E-3FT324I	2280	1.2V	271	-3	ftBGA	324	IND
LCMXO2280E-4FT324I	2280	1.2V	271	-4	ftBGA	324	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3TN100I	256	1.2V	78	-3	Lead-Free TQFP	100	IND
LCMXO256E-4TN100I	256	1.2V	78	-4	Lead-Free TQFP	100	IND
LCMXO256E-3MN100I	256	1.2V	78	-3	Lead-Free csBGA	100	IND
LCMXO256E-4MN100I	256	1.2V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN100I	640	1.2V	74	-3	Lead-Free TQFP	100	IND
LCMXO640E-4TN100I	640	1.2V	74	-4	Lead-Free TQFP	100	IND
LCMXO640E-3MN100I	640	1.2V	74	-3	Lead-Free csBGA	100	IND
LCMXO640E-4MN100I	640	1.2V	74	-4	Lead-Free csBGA	100	IND
LCMXO640E-3TN144I	640	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO640E-4TN144I	640	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO640E-3MN132I	640	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO640E-4MN132I	640	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO640E-3BN256I	640	1.2V	159	-3	Lead-Free caBGA	256	IND
LCMXO640E-4BN256I	640	1.2V	159	-4	Lead-Free caBGA	256	IND
LCMXO640E-3FTN256I	640	1.2V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640E-4FTN256I	640	1.2V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100I	1200	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200E-4TN100I	1200	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200E-3TN144I	1200	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200E-4TN144I	1200	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200E-3MN132I	1200	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200E-4MN132I	1200	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200E-3BN256I	1200	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200E-4BN256I	1200	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200E-3FTN256I	1200	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200E-4FTN256I	1200	1.2V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100I	2280	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280E-4TN100I	2280	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280E-3TN144I	2280	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280E-4TN144I	2280	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280E-3MN132I	2280	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280E-4MN132I	2280	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280E-3BN256I	2280	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280E-4BN256I	2280	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280E-3FTN256I	2280	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280E-4FTN256I	2280	1.2V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280E-3FTN324I	2280	1.2V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280E-4FTN324I	2280	1.2V	271	-4	Lead-Free ftBGA	324	IND