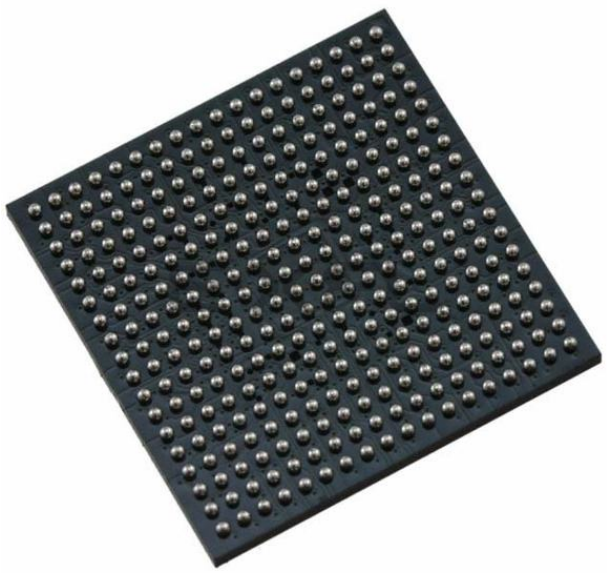
Lattice Semiconductor Corporation - LCMXO2280C-3FTN324C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	285
Number of Logic Elements/Cells	2280
Total RAM Bits	28262
Number of I/O	271
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-LBGA
Supplier Device Package	324-FTBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280c-3ftn324c

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices

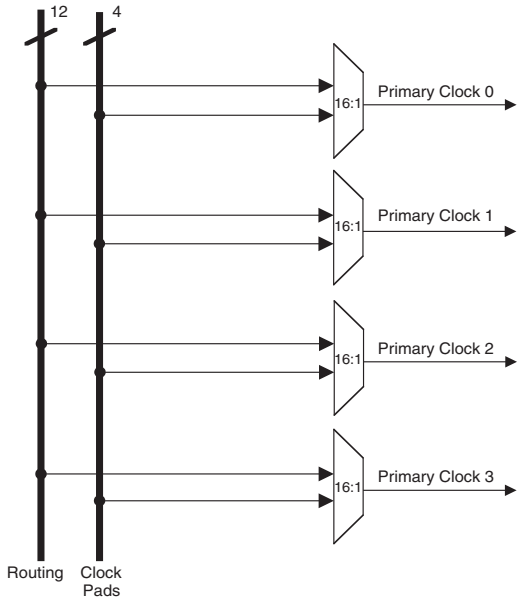
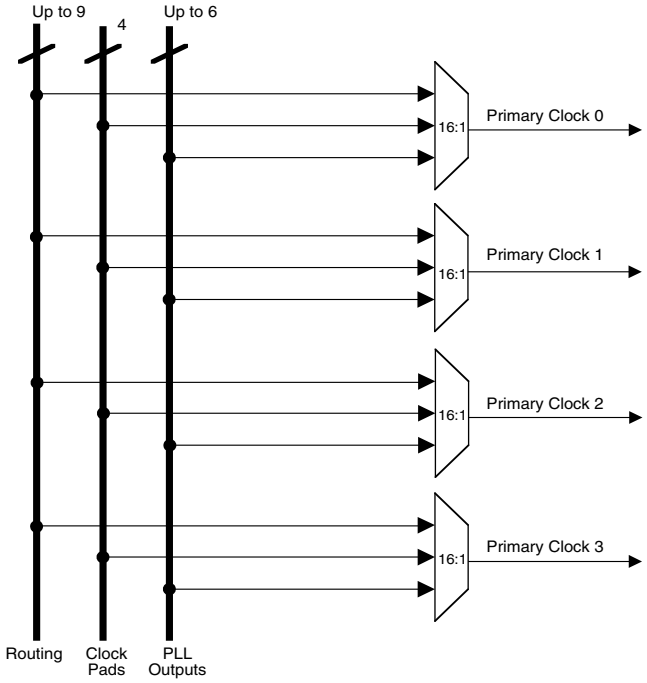


Figure 2-8. Primary Clocks for MachXO1200 and MachXO2280 Devices



Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 2-9. Secondary Clocks for MachXO Devices

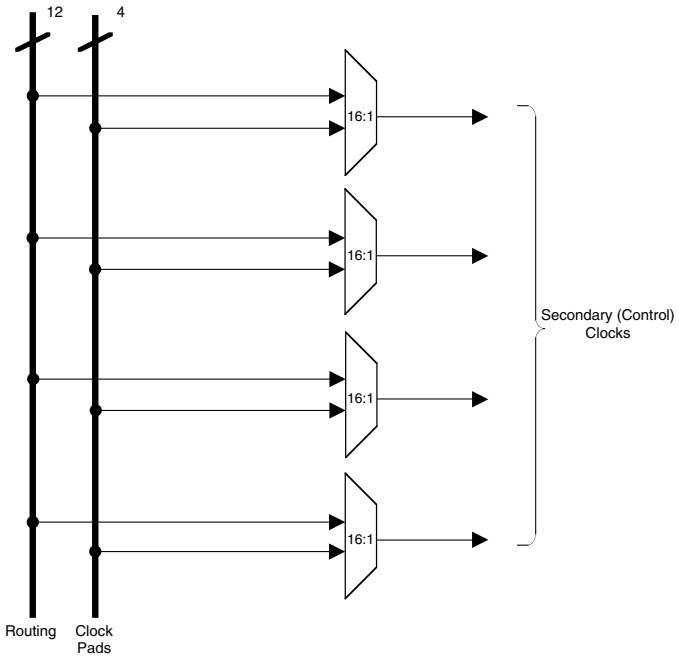


Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from PLL output, clock net, routing/external pin or internal feedback from CLKINTFB port
RST	I	"1" to reset the input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
CLKINTFB	O	Internal feedback source, CLKOP divider output before CLOCKTREE
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lag, "0": Lead
DDAIDEL[2:0]	I	Dynamic Delay Input

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

sysMEM Memory

The MachXO1200 and MachXO2280 devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

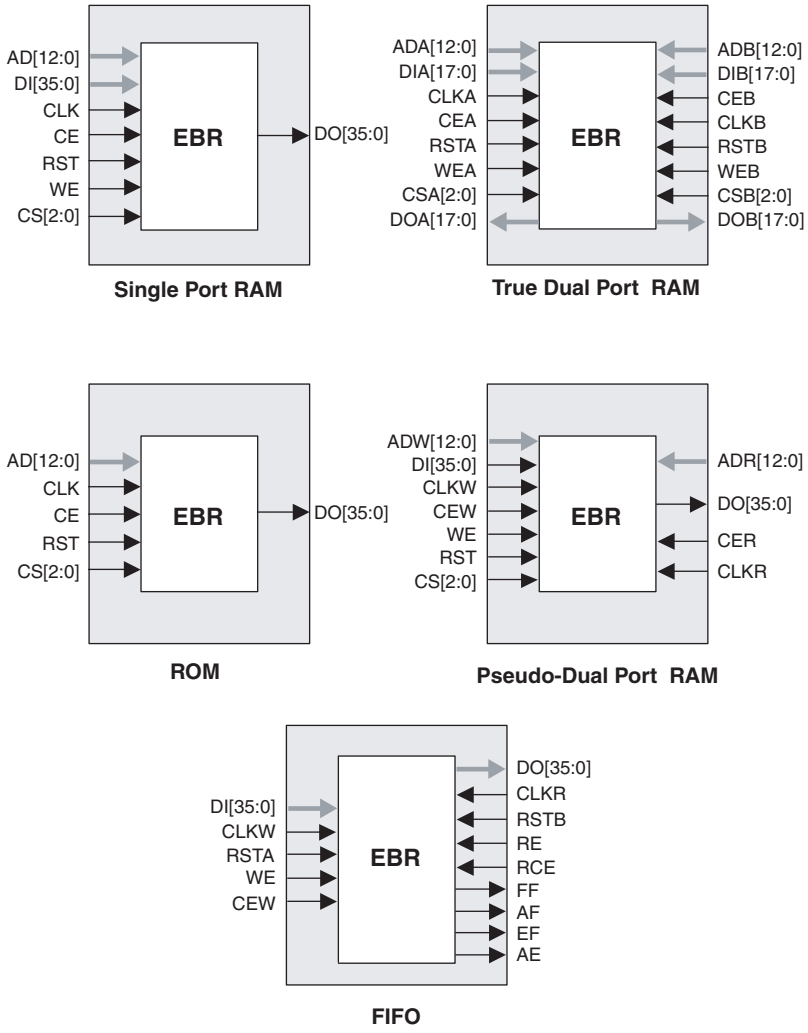
Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-12 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

Figure 2-12. sysMEM Memory Primitives



PIO Groups

On the MachXO devices, PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four IOs are placed on the left and right sides of the device while PIO groups with six IOs are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and PADs.

On all MachXO devices, two adjacent PIOs can be joined to provide a complementary Output driver pair. The I/O pin pairs are labeled as "T" and "C" to distinguish between the true and complement pins.

The MachXO1200 and MachXO2280 devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. In addition, half of the PIO pairs on the left and right sides of these devices can be configured as LVDS transmit/receive pairs. PIOs on the top of these larger devices also provide PCI support.

Figure 2-15. Group of Four Programmable I/O Cells

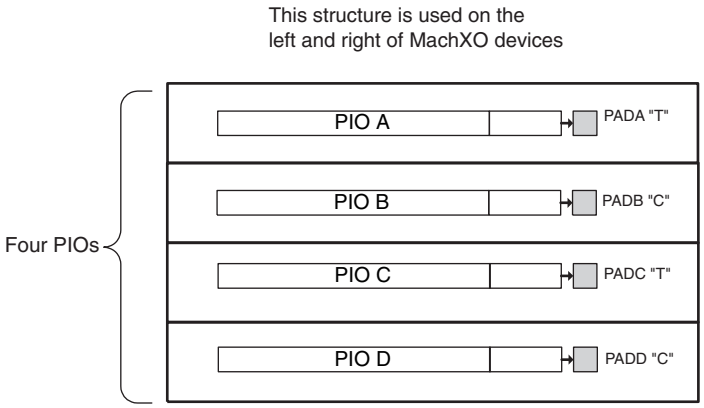
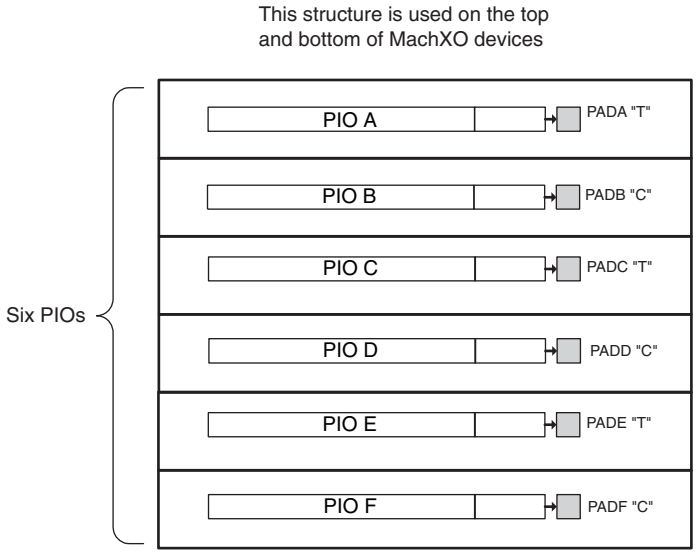


Figure 2-16. Group ofpSix Programmable I/O Cells



PIO

The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast

Table 2-8. I/O Support Device by Device

	MachXO256	MachXO640	MachXO1200	MachXO2280
Number of I/O Banks	2	4	8	8
Type of Input Buffers	Single-ended (all I/O Banks)	Single-ended (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)
Differential Output Emulation Capability	All I/O Banks	All I/O Banks	All I/O Banks	All I/O Banks
PCI Support	No	No	Top side only	Top side only

Table 2-9. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3V**	**2.5V**	**1.8V**	**1.5V**	**1.2V**
Single Ended Interfaces					
LVTTL	Yes	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes	Yes
LVCMOS18			Yes		
LVCMOS15				Yes	
LVCMOS12	Yes	Yes	Yes	Yes	Yes
PCI[1]	Yes				
Differential Interfaces					
BLVDS[2], LVDS[2], LVPECL[2], RSDS[2]	Yes	Yes	Yes	Yes	Yes

1. Top Banks of MachXO1200 and MachXO2280 devices only.
2. MachXO1200 and MachXO2280 devices only.

Table 2-10. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Typ.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA	3.3
LVCMOS33	4mA, 8mA, 12mA, 14mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 14mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 14mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33[3]	N/A	3.3
Differential Interfaces		
LVDS[1, 2]	N/A	2.5
BLVDS, RSDS[2]	N/A	2.5
LVPECL[2]	N/A	3.3

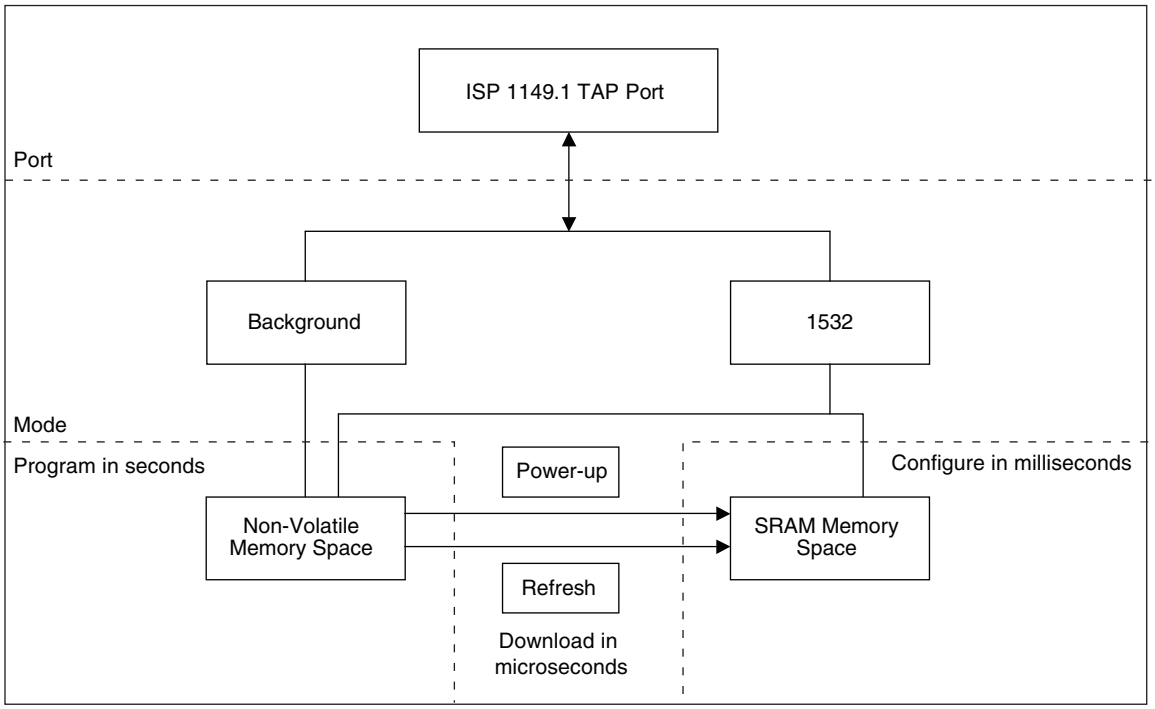
1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top Banks of MachXO1200 and MachXO2280 devices only.

sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the MachXO1200 and MachXO2280 (two Banks per side). The MachXO640 has four Banks (one Bank per side). The smallest member of this family, the MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V_{CCIO}) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

Figure 2-22. MachXO Configuration and Programming



Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

sysIO Differential Electrical Characteristics

LVDS

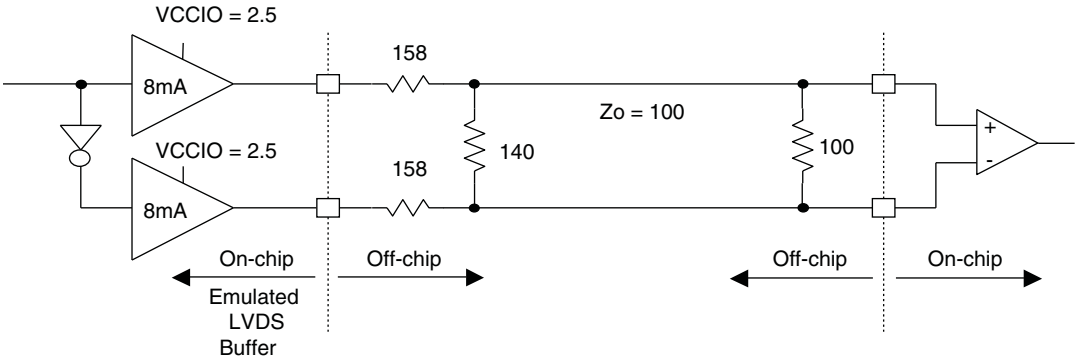
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{THD}	Differential Input Threshold		+/-100	—	—	mV
V_{CM}	Input Common Mode Voltage	100mV ≤ V_{THD}	V_{THD}/2	1.2	1.8	V
		200mV ≤ V_{THD}	V_{THD}/2	1.2	1.9	V
		350mV ≤ V_{THD}	V_{THD}/2	1.2	2.0	V
I_{IN}	Input current	Power on	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

LVDS Emulation

MachXO devices can support LVDS outputs via emulation (LVDS25E), in addition to the LVDS support that is available on-chip on certain devices. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

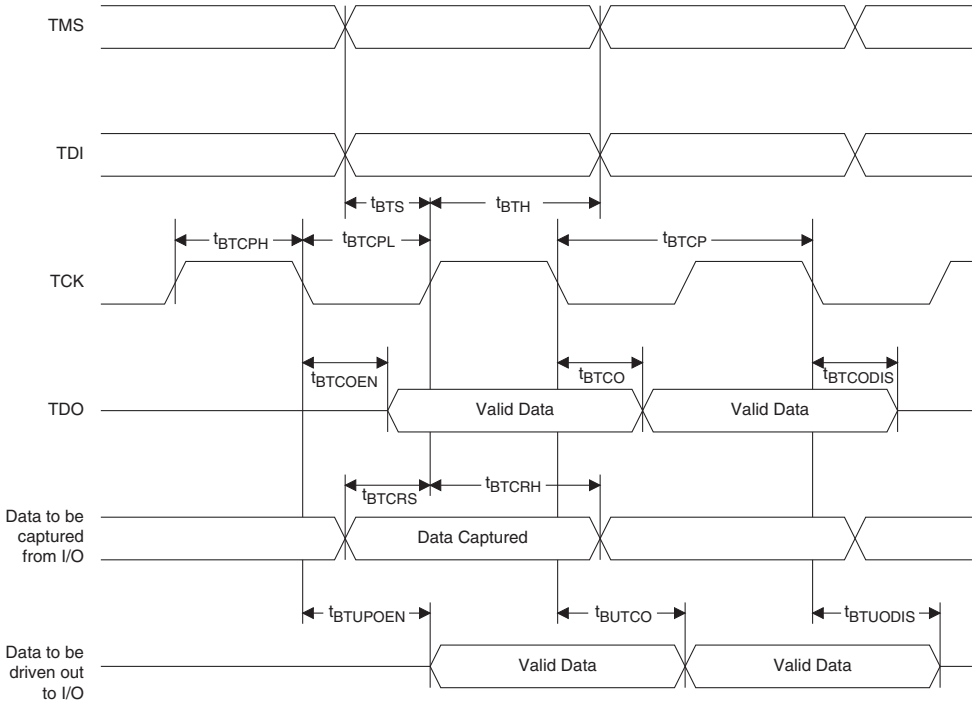
Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

The LVDS differential input buffers are available on certain devices in the MachXO family.

Figure 3-5. JTAG Port Timing Waveforms



LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
43	PB4A	1		T	PB8B	2		
44	PB4B	1		C	PB8C	2		T
45	PB4C	1		T	PB8D	2		C
46	PB4D	1		C	PB9A	2		
47	PB5A	1			PB9C	2		T
48*	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
49	PB5C	1		T	PB9D	2		C
50	PB5D	1		C	PB9F	2		
51	PR9B	0		C	PR11D	1		C
52	PR9A	0		T	PR11B	1		C
53	PR8B	0		C	PR11C	1		T
54	PR8A	0		T	PR11A	1		T
55	PR7D	0		C	PR10D	1		C
56	PR7C	0		T	PR10C	1		T
57	PR7B	0		C	PR10B	1		C
58	PR7A	0		T	PR10A	1		T
59	PR6B	0		C	PR9D	1		
60	VCCIO0	0			VCCIO1	1		
61	PR6A	0		T	PR9B	1		
62	GNDIO0	0			GNDIO1	1		
63	PR5D	0		C	PR7B	1		
64	PR5C	0		T	PR6C	1		
65	PR5B	0		C	PR6B	1		
66	PR5A	0		T	PR5D	1		
67	PR4B	0		C	PR5B	1		
68	PR4A	0		T	PR4D	1		
69	PR3D	0		C	PR4B	1		
70	PR3C	0		T	PR3D	1		
71	PR3B	0		C	PR3B	1		
72	PR3A	0		T	PR2D	1		
73	PR2B	0		C	PR2B	1		
74	VCCIO0	0			VCCIO1	1		
75	GNDIO0	0			GNDIO1	1		
76	PR2A	0		T	PT9F	0		C
77	PT5C	0			PT9E	0		T
78	PT5B	0		C	PT9C	0		
79	PT5A	0		T	PT9A	0		
80	PT4F	0		C	VCCIO0	0		
81	PT4E	0		T	GNDIO0	0		
82	PT4D	0		C	PT7E	0		
83	PT4C	0		T	PT7A	0		
84	GND	-			GND	-		

LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA (Cont.)

LCMXO256					LCMXO640				
Ball Number	Ball Function	Bank	Dual Function	Differen-tial	Ball Number	Ball Function	Bank	Dual Function	Differen-tial
P13	PB5A	1			P13	PB9C	2		T
M12*	SLEEPN	-	SLEEPN		M12*	SLEEPN	-	SLEEPN	
P14	PB5C	1		T	P14	PB9D	2		C
N13	PB5D	1		C	N13	PB9F	2		
N14	PR9B	0		C	N14	PR11D	1		C
M14	PR9A	0		T	M14	PR11B	1		C
L13	PR8B	0		C	L13	PR11C	1		T
L14	PR8A	0		T	L14	PR11A	1		T
M13	PR7D	0		C	M13	PR10D	1		C
K14	PR7C	0		T	K14	PR10C	1		T
K13	PR7B	0		C	K13	PR10B	1		C
J14	PR7A	0		T	J14	PR10A	1		T
J13	PR6B	0		C	J13	PR9D	1		
H13	PR6A	0		T	H13	PR9B	1		
G14	GNDIO0	0			G14	GNDIO1	1		
G13	PR5D	0		C	G13	PR7B	1		
F14	PR5C	0		T	F14	PR6C	1		
F13	PR5B	0		C	F13	PR6B	1		
E14	PR5A	0		T	E14	PR5D	1		
E13	PR4B	0		C	E13	PR5B	1		
D14	PR4A	0		T	D14	PR4D	1		
D13	PR3D	0		C	D13	PR4B	1		
C14	PR3C	0		T	C14	PR3D	1		
C13	PR3B	0		C	C13	PR3B	1		
B14	PR3A	0		T	B14	PR2D	1		
C12	PR2B	0		C	C12	PR2B	1		
B13	GNDIO0	0			B13	GNDIO1	1		
A13	PR2A	0		T	A13	PT9F	0		C
A12	PT5C	0			A12	PT9E	0		T
B11	PT5B	0		C	B11	PT9C	0		
A11	PT5A	0		T	A11	PT9A	0		
B12	PT4F	0		C	B12	VCCIO0	0		
A10	PT4E	0		T	A10	GNDIO0	0		
B10	PT4D	0		C	B10	PT7E	0		
A9	PT4C	0		T	A9	PT7A	0		
A8	PT4B	0	PCLK0_1**	C	A8	PT6B	0	PCLK0_1**	
B8	PT4A	0	PCLK0_0**	T	B8	PT5B	0	PCLK0_0**	C
A7	PT3D	0		C	A7	PT5A	0		T
B7	VCCAUX	-			B7	VCCAUX	-		
A6	PT3C	0		T	A6	PT4F	0		
B6	VCC	-			B6	VCC	-		
A5	PT3B	0		C	A5	PT3F	0		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
51	TDI	2	TDI		TDI	5	TDI		TDI	5	TDI	
52	VCC	-			VCC	-			VCC	-		
53	VCCAUX	-			VCCAUX	-			VCCAUX	-		
54	PB5A	2		T	PB6F	5			PB8F	5		
55	PB5B	2	PCLKT2_1***	C	PB7B	4	PCLK4_1***		PB10F	4	PCLK4_1***	
56	PB5D	2			PB7C	4		T	PB10C	4		T
57	PB6A	2		T	PB7D	4		C	PB10D	4		C
58	PB6B	2	PCLKT2_0***	C	PB7F	4	PCLK4_0***		PB10B	4	PCLK4_0***	
59	GND	-			GND	-			GND	-		
60	PB7C	2			PB9A	4		T	PB12A	4		T
61	PB7E	2			PB9B	4		C	PB12B	4		C
62	PB8A	2			PB9E	4			PB12E	4		
63	VCCIO2	2			VCCIO4	4			VCCIO4	4		
64	GNDIO2	2			GNDIO4	4			GNDIO4	4		
65	PB8C	2		T	PB10A	4		T	PB13A	4		T
66	PB8D	2		C	PB10B	4		C	PB13B	4		C
67	PB9A	2		T	PB10C	4		T	PB13C	4		T
68	PB9C	2		T	PB10D	4		C	PB13D	4		C
69	PB9B	2		C	PB10F	4			PB14D	4		
70**	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
71	PB9D	2		C	PB11C	4		T	PB16C	4		T
72	PB9F	2			PB11D	4		C	PB16D	4		C
73	PR11D	1		C	PR16B	3		C	PR20B	3		C
74	PR11B	1		C	PR16A	3		T	PR20A	3		T
75	PR11C	1		T	PR15B	3		C*	PR19B	3		C
76	PR10D	1		C	PR15A	3		T*	PR19A	3		T
77	PR11A	1		T	PR14D	3		C	PR17D	3		C
78	PR10B	1		C	PR14C	3		T	PR17C	3		T
79	PR10C	1		T	PR14B	3		C*	PR17B	3		C*
80	PR10A	1		T	PR14A	3		T*	PR17A	3		T*
81	PR9D	1			PR13D	3			PR16D	3		
82	VCCIO1	1			VCCIO3	3			VCCIO3	3		
83	GNDIO1	1			GNDIO3	3			GNDIO3	3		
84	PR9A	1			PR12B	3		C*	PR15B	3		C*
85	PR8C	1			PR12A	3		T*	PR15A	3		T*
86	PR8A	1			PR11B	3		C*	PR14B	3		C*
87	PR7D	1			PR11A	3		T*	PR14A	3		T*
88	GND	-			GND	-			GND	-		
89	PR7B	1		C	PR10B	3		C*	PR13B	3		C*
90	PR7A	1		T	PR10A	3		T*	PR13A	3		T*
91	PR6D	1		C	PR8B	2		C*	PR10B	2		C*
92	PR6C	1		T	PR8A	2		T*	PR10A	2		T*
93	VCC	-			VCC	-			VCC	-		
94	PR5D	1			PR6B	2		C*	PR8B	2		C*
95	PR5B	1			PR6A	2		T*	PR8A	2		T*
96	PR4D	1			PR5B	2		C*	PR7B	2		C*
97	PR4B	1		C	PR5A	2		T*	PR7A	2		T*
98	VCCIO1	1			VCCIO2	2			VCCIO2	2		
99	GNDIO1	1			GNDIO2	2			GNDIO2	2		
100	PR4A	1		T	PR4C	2			PR5C	2		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T
A3	PT2B	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2A	0		T	A2	PT3A	0		T	A2	PT3A	0		T
B3	NC				B3	PT2B	0		C	B3	PT2D	0		C
B2	NC				B2	PT2A	0		T	B2	PT2C	0		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A16	GND	-			A16	GND	-			A16	GND	-		
F11	GND	-			F11	GND	-			F11	GND	-		
G8	GND	-			G8	GND	-			G8	GND	-		
G9	GND	-			G9	GND	-			G9	GND	-		
H7	GND	-			H7	GND	-			H7	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
H9	GND	-			H9	GND	-			H9	GND	-		
H10	GND	-			H10	GND	-			H10	GND	-		
J7	GND	-			J7	GND	-			J7	GND	-		
J8	GND	-			J8	GND	-			J8	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
K8	GND	-			K8	GND	-			K8	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L6	GND	-			L6	GND	-			L6	GND	-		
T1	GND	-			T1	GND	-			T1	GND	-		
T16	GND	-			T16	GND	-			T16	GND	-		
G7	VCC	-			G7	VCC	-			G7	VCC	-		
G10	VCC	-			G10	VCC	-			G10	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
K10	VCC	-			K10	VCC	-			K10	VCC	-		
H6	VCCIO3	3			H6	VCCIO7	7			H6	VCCIO7	7		
G6	VCCIO3	3			G6	VCCIO7	7			G6	VCCIO7	7		
K6	VCCIO3	3			K6	VCCIO6	6			K6	VCCIO6	6		
J6	VCCIO3	3			J6	VCCIO6	6			J6	VCCIO6	6		
L8	VCCIO2	2			L8	VCCIO5	5			L8	VCCIO5	5		
L7	VCCIO2	2			L7	VCCIO5	5			L7	VCCIO5	5		
L9	VCCIO2	2			L9	VCCIO4	4			L9	VCCIO4	4		
L10	VCCIO2	2			L10	VCCIO4	4			L10	VCCIO4	4		
K11	VCCIO1	1			K11	VCCIO3	3			K11	VCCIO3	3		
J11	VCCIO1	1			J11	VCCIO3	3			J11	VCCIO3	3		
H11	VCCIO1	1			H11	VCCIO2	2			H11	VCCIO2	2		
G11	VCCIO1	1			G11	VCCIO2	2			G11	VCCIO2	2		
F9	VCCIO0	0			F9	VCCIO1	1			F9	VCCIO1	1		
F10	VCCIO0	0			F10	VCCIO1	1			F10	VCCIO1	1		
F8	VCCIO0	0			F8	VCCIO0	0			F8	VCCIO0	0		
F7	VCCIO0	0			F7	VCCIO0	0			F7	VCCIO0	0		

* Supports true LVDS outputs.
** NC for “E” devices.
*** Primary clock inputs are single-ended.

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
E13	PT16D	1		C
C15	PT16C	1		T
F13	PT16B	1		C
D14	PT16A	1		T
A18	PT15D	1		C
B17	PT15C	1		T
A16	PT15B	1		C
A17	PT15A	1		T
VCC	VCC	-		
D13	PT14D	1		C
F12	PT14C	1		T
C14	PT14B	1		C
E12	PT14A	1		T
C13	PT13D	1		C
B16	PT13C	1		T
B15	PT13B	1		C
A15	PT13A	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
B14	PT12F	1		C
A14	PT12E	1		T
D12	PT12D	1		C
F11	PT12C	1		T
B13	PT12B	1		C
A13	PT12A	1		T
C12	PT11D	1		C
GND	GND	-		
B12	PT11C	1		T
E11	PT11B	1		C
D11	PT11A	1		T
C11	PT10F	1		C
A12	PT10E	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
F10	PT10D	1		C
D10	PT10C	1		T
B11	PT10B	1	PCLK1_1***	C
A11	PT10A	1		T
E10	PT9D	1		C
C10	PT9C	1		T
D9	PT9B	1	PCLK1_0***	C
E9	PT9A	1		T
B10	PT8F	0		C

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1090 - Power Estimation and Management for MachXO Devices
- Power Calculator tool included with the Lattice ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

Conventional Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100I	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	IND
LCMXO256C-4T100I	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	IND
LCMXO256C-3M100I	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	IND
LCMXO256C-4M100I	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3T100I	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	IND
LCMXO640C-4T100I	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	IND
LCMXO640C-3M100I	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	IND
LCMXO640C-4M100I	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	IND
LCMXO640C-3T144I	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMXO640C-4T144I	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMXO640C-3M132I	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMXO640C-4M132I	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMXO640C-3B256I	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	IND
LCMXO640C-4B256I	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	IND
LCMXO640C-3FT256I	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	IND
LCMXO640C-4FT256I	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3T100I	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMXO1200C-4T100I	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMXO1200C-3T144I	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMXO1200C-4T144I	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMXO1200C-3M132I	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMXO1200C-4M132I	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMXO1200C-3B256I	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMXO1200C-4B256I	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMXO1200C-3FT256I	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMXO1200C-4FT256I	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-3T100I	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMXO2280C-4T100I	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMXO2280C-3T144I	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMXO2280C-4T144I	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMXO2280C-3M132I	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMXO2280C-4M132I	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMXO2280C-3B256I	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMXO2280C-4B256I	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMXO2280C-3FT256I	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMXO2280C-4FT256I	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND
LCMXO2280C-3FT324I	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	IND
LCMXO2280C-4FT324I	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	IND

Lead-Free Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100I	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	IND
LCMXO256C-4TN100I	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	IND
LCMXO256C-3MN100I	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	IND
LCMXO256C-4MN100I	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3TN100I	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	IND
LCMXO640C-4TN100I	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	IND
LCMXO640C-3MN100I	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	IND
LCMXO640C-4MN100I	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	IND
LCMXO640C-3TN144I	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	IND
LCMXO640C-4TN144I	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	IND
LCMXO640C-3MN132I	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	IND
LCMXO640C-4MN132I	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	IND
LCMXO640C-3BN256I	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	IND
LCMXO640C-4BN256I	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	IND
LCMXO640C-3FTN256I	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640C-4FTN256I	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3TN100I	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200C-4TN100I	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200C-3TN144I	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200C-4TN144I	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200C-3MN132I	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200C-4MN132I	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200C-3BN256I	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200C-4BN256I	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200C-3FTN256I	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200C-4FTN256I	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-3TN100I	2280	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280C-4TN100I	2280	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280C-3TN144I	2280	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280C-4TN144I	2280	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280C-3MN132I	2280	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280C-4MN132I	2280	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280C-3BN256I	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280C-4BN256I	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280C-3FTN256I	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280C-4FTN256I	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280C-3FTN324I	2280	1.8V/2.5V/3.3V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280C-4FTN324I	2280	1.8V/2.5V/3.3V	271	-4	Lead-Free ftBGA	324	IND

Date	Version	Section	Change Summary
April 2006 (cont.)	02.0 (cont.)	Architecture (cont.)	"Top View of the MachXO1200 Device" figure updated.
			"Top View of the MachXO640 Device" figure updated.
			"Top View of the MachXO256 Device" figure updated.
			"Slice Diagram" figure updated.
			Slice Signal Descriptions table updated.
			Routing section updated.
			sysCLOCK Phase Lockecd Loops (PLLs) section updated.
			PLL Diagram updated.
			PLL Signal Descriptions table updated.
			sysMEM Memory section has been updated.
			PIO Groups section has been updated.
			PIO section has been updated.
			MachXO PIO Block Diagram updated.
			Supported Input Standards table updated.
			MachXO Configuration and Programming diagram updated.
		DC and Switching Characteristics	Recommended Operating Conditions table - footnotes updated.
			MachXO256 and MachXO640 Hot Socketing Specifications - footnotes updated.
			Added MachXO1200 and MachXO2280 Hot Socketing Specifications table.
			DC Electrical Characteristics, footnotes have been updated.
			Supply Current (Sleep Mode) table has been updated, removed "4W" references. Footnotes have been updated.
			Supply Current (Standby) table and associated footnotes updated.
			Intialization Supply Current table and footnotes updated.
			Programming and Erase Flash Supply Current table and associated footnotes have been updatd.
			Register-to-Register Performance table updated (rev. A 0.19).
			MachXO External Switching Characteristics updated (rev. A 0.19).
			MachXO Internal Timing Parameters updated (rev. A 0.19).
			MachXO Family Timing Adders updated (rev. A 0.19).
			sysCLOCK Timing updated (rev. A 0.19).
			MachXO "C" Sleep Mode Timing updated (A 0.19).
			JTAG Port Timing Specification updated (rev. A 0.19).
			Test Fixture Required Components table updated.
		Pinout Information	Signal Descriptions have been updated.
			Pin Information Summary has been updated. Footnote has been added.
			Power Supply and NC Connection table has been updated.
			Logic Signal Connections have been updated (PCLKTx_x --> PCLKx_x)
		Ordering Information	Removed "4W" references.
			Added 256-ftBGA Ordering Part Numbers for MachXO640.
May 2006	02.1	Pinout Information	Removed [LOC][0]_PLL_RST from Signal Description table.
			PCLK footnote has been added to all appropriate pins.
August 2006	02.2	Multiple	Removed 256 fpBGA information for MachXO640.