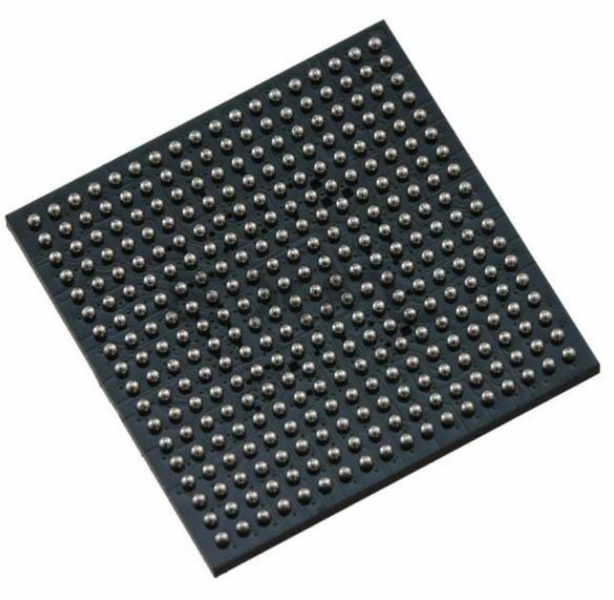

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Details	
Product Status	Active
Number of LABs/CLBs	285
Number of Logic Elements/Cells	2280
Total RAM Bits	28262
Number of I/O	271
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LBGA
Supplier Device Package	324-FTBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280c-3ftn324i

MachXO Family Data Sheet
Architecture

June 2013 Data Sheet DS1002

Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT use.

The MachXO registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

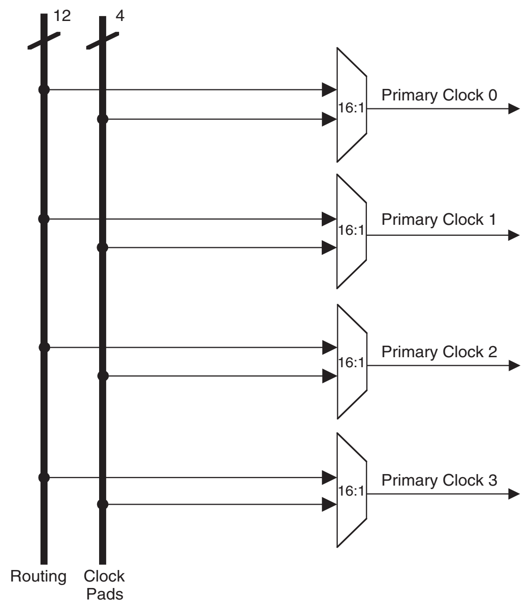
Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices



of the devices also support differential input buffers. PCI clamps are available on the top Bank I/O buffers. The PCI clamp is enabled after V_{CC}, V_{CCAUX}, and V_{CCIO} are at valid operating levels and the device has been configured.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Left and Right sysIO Buffer Pairs**
The sysIO buffer pairs in the left and right Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these Banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all V_{CCIO} Banks are active with valid input logic levels to properly control the output logic states of all the I/O Banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to VCCIO. The I/O pins will maintain the blank configuration until VCC, VCCAUX and VCCIO have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore, V_{CCIO} supplies should be powered up before or together with the V_{CC} and V_{CCAUX} supplies

Supported Standards

The MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The MachXO1200 and MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right Banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all Banks of MachXO1200 and MachXO2280 devices. PCI support is provided in the top Banks of the MachXO1200 and MachXO2280 devices. Table 2-8 summarizes the I/O characteristics of the devices in the MachXO family.

Tables 2-9 and 2-10 show the I/O standards (together with their supply and reference voltages) supported by the MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The MachXO "C" devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

Table 2-11. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <10mA	0	Typical <100uA
I/O Leakage	<10µA	<1mA	<10µA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1}; MachXO640: V_{CCIO2}; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Supply Current (Sleep Mode)[1, 2]

Symbol	Parameter	Device	Typ.[3]	Max.	Units
I_{CC}	Core Power Supply	LCMXO256C	12	25	µA
		LCMXO640C	12	25	µA
		LCMXO1200C	12	25	µA
		LCMXO2280C	12	25	µA
I_{CCAUX}	Auxiliary Power Supply	LCMXO256C	1	15	µA
		LCMXO640C	1	25	µA
		LCMXO1200C	1	45	µA
		LCMXO2280C	1	85	µA
I_{CCIO}	Bank Power Supply[4]	All LCMXO ‘C’ Devices	2	30	µA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency = 0MHz.
3. T_A = 25°C, power supplies at nominal voltage.
4. Per Bank.

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	7	mA
		LCMXO640C	9	mA
		LCMXO1200C	14	mA
		LCMXO2280C	20	mA
		LCMXO256E	4	mA
		LCMXO640E	6	mA
		LCMXO1200E	10	mA
		LCMXO2280E	12	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LCMXO256E/C	5	mA
		LCMXO640E/C	7	mA
		LCMXO1200E/C	12	mA
		LCMXO2280E/C	13	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND.
3. Frequency = 0MHz.
4. User pattern = blank.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	13	mA
		LCMXO640C	17	mA
		LCMXO1200C	21	mA
		LCMXO2280C	23	mA
		LCMXO256E	10	mA
		LCMXO640E	14	mA
		LCMXO1200E	18	mA
		LCMXO2280E	20	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LCMXO256E/C	10	mA
		LCMXO640E/C	13	mA
		LCMXO1200E/C	24	mA
		LCMXO2280E/C	25	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Frequency = 0MHz.
4. Typical user pattern.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank, V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	9	mA
		LCMXO640C	11	mA
		LCMXO1200C	16	mA
		LCMXO2280C	22	mA
		LCMXO256E	6	mA
		LCMXO640E	8	mA
		LCMXO1200E	12	mA
		LCMXO2280E	14	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LCMXO256C/E	8	mA
		LCMXO640C/E	10	mA
		LCMXO1200/E	15	mA
		LCMXO2280C/E	16	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Typical user pattern.
4. JTAG programming is at 25MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

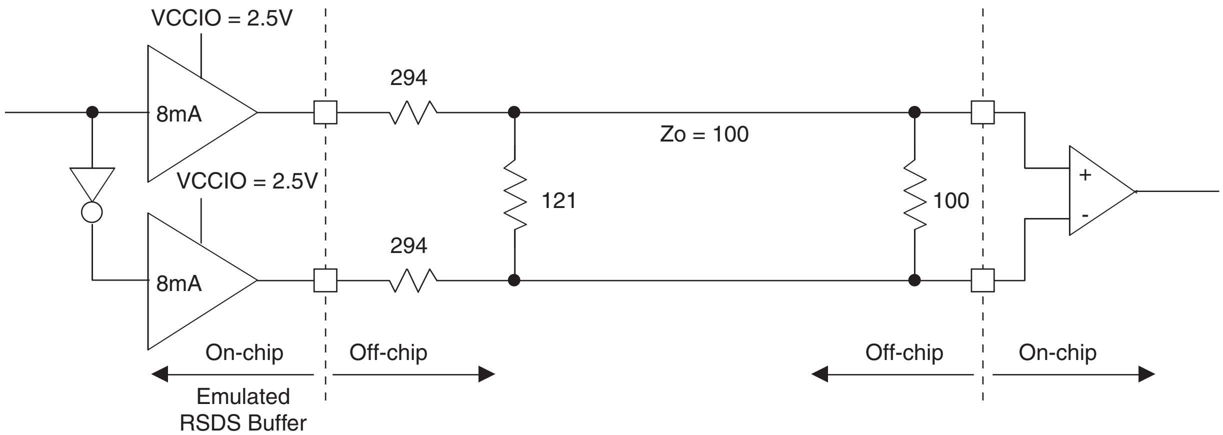


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

MachXO External Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Global Clock without PLL)[1]									
t_{PD}	Best Case t_{PD} Through 1 LUT	LCMXO256	—	3.5	—	4.2	—	4.9	ns
		LCMXO640	—	3.5	—	4.2	—	4.9	ns
		LCMXO1200	—	3.6	—	4.4	—	5.1	ns
		LCMXO2280	—	3.6	—	4.4	—	5.1	ns
t_{CO}	Best Case Clock to Output - From PFU	LCMXO256	—	4.0	—	4.8	—	5.6	ns
		LCMXO640	—	4.0	—	4.8	—	5.7	ns
		LCMXO1200	—	4.3	—	5.2	—	6.1	ns
		LCMXO2280	—	4.3	—	5.2	—	6.1	ns
t_{SU}	Clock to Data Setup - To PFU	LCMXO256	1.3	—	1.6	—	1.8	—	ns
		LCMXO640	1.1	—	1.3	—	1.5	—	ns
		LCMXO1200	1.1	—	1.3	—	1.6	—	ns
		LCMXO2280	1.1	—	1.3	—	1.5	—	ns
t_H	Clock to Data Hold - To PFU	LCMXO256	-0.3	—	-0.3	—	-0.3	—	ns
		LCMXO640	-0.1	—	-0.1	—	-0.1	—	ns
		LCMXO1200	0.0	—	0.0	—	0.0	—	ns
		LCMXO2280	-0.4	—	-0.4	—	-0.4	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LCMXO256	—	600	—	550	—	500	MHz
		LCMXO640	—	600	—	550	—	500	MHz
		LCMXO1200	—	600	—	550	—	500	MHz
		LCMXO2280	—	600	—	550	—	500	MHz
t_{SKEW_PRI}	Global Clock Skew Across Device	LCMXO256	—	200	—	220	—	240	ps
		LCMXO640	—	200	—	220	—	240	ps
		LCMXO1200	—	220	—	240	—	260	ps
		LCMXO2280	—	220	—	240	—	260	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA.

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MachXO Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25[4]	LVDS	0.44	0.53	0.61	ns
BLVDS25[4]	BLVDS	0.44	0.53	0.61	ns
LVPECL33[4]	LVPECL	0.42	0.50	0.59	ns
LVTTL33	LVTTL	0.01	0.01	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	0.01	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	0.07	0.08	0.10	ns
LVCMOS15	LVCMOS 1.5	0.14	0.17	0.19	ns
LVCMOS12	LVCMOS 1.2	0.40	0.48	0.56	ns
PCI33[4]	PCI	0.01	0.01	0.01	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E	-0.13	-0.15	-0.18	ns
LVDS25[4]	LVDS 2.5	-0.21	-0.26	-0.30	ns
BLVDS25	BLVDS 2.5	-0.03	-0.03	-0.04	ns
LVPECL33	LVPECL 3.3	0.04	0.04	0.05	ns
LVTTL33_4mA	LVTTL 4mA drive	0.04	0.04	0.05	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.07	0.08	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.01	-0.01	-0.01	ns
LVTTL33_16mA	LVTTL 16mA drive	0.50	0.60	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.04	0.04	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.06	0.07	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	-0.01	-0.01	-0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14mA drive	0.50	0.60	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.05	0.06	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.10	0.12	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14mA drive	0.34	0.40	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.11	0.13	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.05	0.06	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	-0.06	-0.07	-0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14mA drive	0.06	0.07	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.15	0.19	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.05	0.06	0.07	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.26	0.31	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.05	0.06	0.07	ns
PCI33[4]	PCI33	1.85	2.22	2.59	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

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sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6]	18	25	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f_{VCO}	PLL VCO Frequency		420	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6]	18	25	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	55	%
t_{PH}[4]	Output Phase Accuracy		—	0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	+/-120	ps
		f_{OUT} < 100 MHz	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	1	—	ns
t_{LOCK}[2]	PLL Lock-in Time		—	150	µs
t_{PA}	Programmable Delay Unit		100	450	ps
t_{IPJIT}	Input Clock Period Jitter	$f_{OUT} \geq$ 100 MHz	—	+/-200	ps
		f_{OUT} < 100 MHz	—	0.02	UI
t_{FBKDLY}	External Feedback Delay		—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST Pulse Width		10	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output.
5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.
6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.

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MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	SLEEPN Low to Power Down	All	—	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	LCMXO256	—	—	400	µs
		LCMXO640	—	—	600	µs
		LCMXO1200	—	—	800	µs
		LCMXO2280	—	—	1000	µs
$t_{WSLEEPN}$	SLEEPN Pulse Width	All	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	All	—	—	100	ns

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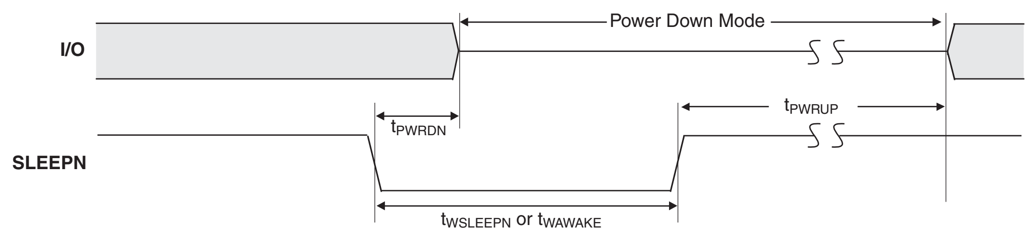
Flash Download Time



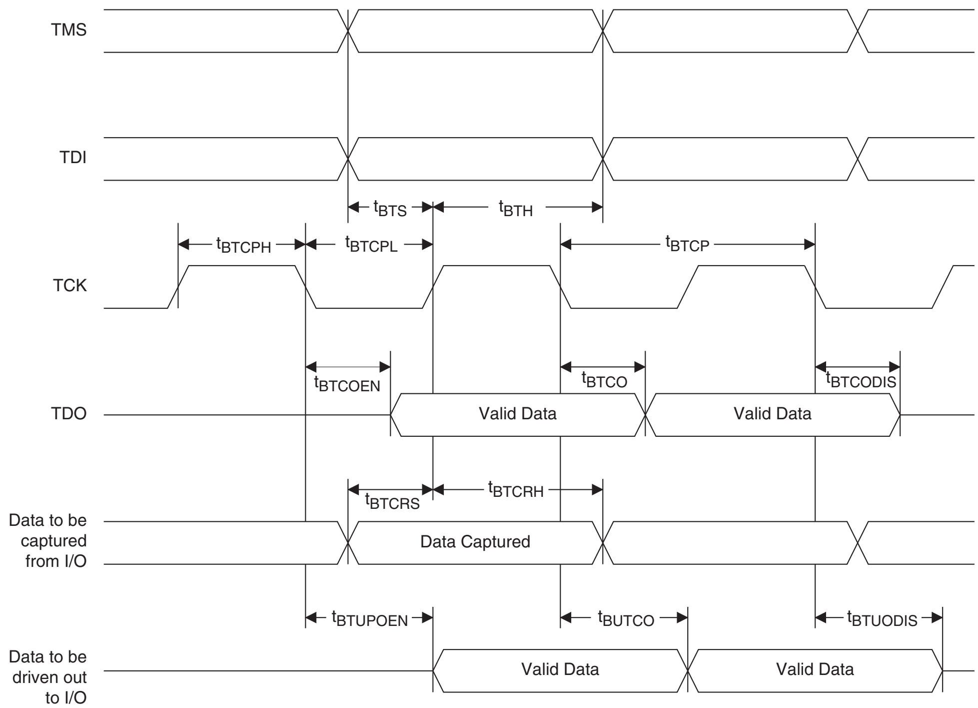
Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	Minimum V_{CC} or V_{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO256	—	—	0.4	ms
		LCMXO640	—	—	0.6	ms
		LCMXO1200	—	—	0.8	ms
		LCMXO2280	—	—	1.0	ms

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

Rev. A 0.19

Figure 3-5. JTAG Port Timing Waveforms



LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP

	LCMXO256				LCMXO640			
Pin Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	1		T	PL2A	3		T
2	PL2B	1		C	PL2C	3		T
3	PL3A	1		T	PL2B	3		C
4	PL3B	1		C	PL2D	3		C
5	PL3C	1		T	PL3A	3		T
6	PL3D	1		C	PL3B	3		C
7	PL4A	1		T	PL3C	3		T
8	PL4B	1		C	PL3D	3		C
9	PL5A	1		T	PL4A	3		
10	VCCIO1	1			VCCIO3	3		
11	PL5B	1		C	PL4C	3		T
12	GNDIO1	1			GNDIO3	3		
13	PL5C	1		T	PL4D	3		C
14	PL5D	1	GSRN	C	PL5B	3	GSRN	
15	PL6A	1		T	PL7B	3		
16	PL6B	1	TSALL	C	PL8C	3	TSALL	T
17	PL7A	1		T	PL8D	3		C
18	PL7B	1		C	PL9A	3		
19	PL7C	1		T	PL9C	3		
20	PL7D	1		C	PL10A	3		
21	PL8A	1		T	PL10C	3		
22	PL8B	1		C	PL11A	3		
23	PL9A	1		T	PL11C	3		
24	VCCIO1	1			VCCIO3	3		
25	GNDIO1	1			GNDIO3	3		
26	TMS	1	TMS		TMS	2	TMS	
27	PL9B	1		C	PB2C	2		
28	TCK	1	TCK		TCK	2	TCK	
29	PB2A	1		T	VCCIO2	2		
30	PB2B	1		C	GNDIO2	2		
31	TDO	1	TDO		TDO	2	TDO	
32	PB2C	1		T	PB4C	2		
33	TDI	1	TDI		TDI	2	TDI	
34	PB2D	1		C	PB4E	2		
35	VCC	-			VCC	-		
36	PB3A	1	PCLK1_1**	T	PB5B	2	PCLK2_1**	
37	PB3B	1		C	PB5D	2		
38	PB3C	1	PCLK1_0**	T	PB6B	2	PCLK2_0**	
39	PB3D	1		C	PB6C	2		
40	GND	-			GND	-		
41	VCCIO1	1			VCCIO2	2		
42	GNDIO1	1			GNDIO2	2		

LCMXO1200 and LCMXO2280 Logic Signal Connections: 100 TQFP

Pin Number	LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
4	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
5	PL4B	7			PL4B	7		
6	VCCIO7	7			VCCIO7	7		
7	PL6A	7		T*	PL7A	7		T*
8	PL6B	7	GSRN	C*	PL7B	7	GSRN	C*
9	GND	-			GND	-		
10	PL7C	7		T	PL9C	7		T
11	PL7D	7		C	PL9D	7		C
12	PL8C	7		T	PL10C	7		T
13	PL8D	7		C	PL10D	7		C
14	PL9C	6			PL11C	6		
15	PL10A	6		T*	PL13A	6		T*
16	PL10B	6		C*	PL13B	6		C*
17	VCC	-			VCC	-		
18	PL11B	6			PL14D	6		C
19	PL11C	6	TSALL		PL14C	6	TSALL	T
20	VCCIO6	6			VCCIO6	6		
21	PL13C	6			PL16C	6		
22	PL14A	6	LLM0_PLLT_FB_A	T*	PL17A	6	LLM0_PLLT_FB_A	T*
23	PL14B	6	LLM0_PLLC_FB_A	C*	PL17B	6	LLM0_PLLC_FB_A	C*
24	PL15A	6	LLM0_PLLT_IN_A	T*	PL18A	6	LLM0_PLLT_IN_A	T*
25	PL15B	6	LLM0_PLLC_IN_A	C*	PL18B	6	LLM0_PLLC_IN_A	C*
26**	GNDIO6 GNDIO5	-			GNDIO6 GNDIO5	-		
27	VCCIO5	5			VCCIO5	5		
28	TMS	5	TMS		TMS	5	TMS	
29	TCK	5	TCK		TCK	5	TCK	
30	PB3B	5			PB3B	5		
31	PB4A	5		T	PB4A	5		T
32	PB4B	5		C	PB4B	5		C
33	TDO	5	TDO		TDO	5	TDO	
34	TDI	5	TDI		TDI	5	TDI	
35	VCC	-			VCC	-		
36	VCCAUX	-			VCCAUX	-		
37	PB6E	5		T	PB8E	5		T
38	PB6F	5		C	PB8F	5		C
39	PB7B	4	PCLK4_1****		PB10F	4	PCLK4_1****	
40	PB7F	4	PCLK4_0****		PB10B	4	PCLK4_0****	
41	GND	-			GND	-		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B1	PL2A	3		T	B1	PL2A	7		T	B1	PL2A	7	LUM0_PLLT_FB_A	T
C1	PL2B	3		C	C1	PL3C	7		T	C1	PL3C	7	LUM0_PLLT_IN_A	T
B2	PL2C	3		T	B2	PL2B	7		C	B2	PL2B	7	LUM0_PLLC_FB_A	C
C2	PL2D	3		C	C2	PL4A	7		T*	C2	PL4A	7		T*
C3	PL3A	3		T	C3	PL3D	7		C	C3	PL3D	7	LUM0_PLLC_IN_A	C
D1	PL3B	3		C	D1	PL4B	7		C*	D1	PL4B	7		C*
D3	PL3D	3			D3	PL4C	7			D3	PL4C	7		
E1	GNDIO3	3			E1	GNDIO7	7			E1	GNDIO7	7		
E2	PL5A	3		T	E2	PL6A	7		T*	E2	PL7A	7		T*
E3	PL5B	3	GSRN	C	E3	PL6B	7	GSRN	C*	E3	PL7B	7	GSRN	C*
F2	PL5D	3			F2	PL6D	7			F2	PL7D	7		
F3	PL6B	3			F3	PL7C	7		T	F3	PL9C	7		T
G1	PL6C	3		T	G1	PL7D	7		C	G1	PL9D	7		C
G2	PL6D	3		C	G2	PL8C	7		T	G2	PL10C	7		T
G3	PL7A	3		T	G3	PL8D	7		C	G3	PL10D	7		C
H2	PL7B	3		C	H2	PL10A	6		T*	H2	PL12A	6		T*
H1	PL7C	3			H1	PL10B	6		C*	H1	PL12B	6		C*
H3	VCC	-			H3	VCC	-			H3	VCC	-		
J1	PL8A	3			J1	PL11B	6			J1	PL14D	6		C
J2	PL8C	3	TSALL		J2	PL11C	6	TSALL	T	J2	PL14C	6	TSALL	T
J3	PL9A	3		T	J3	PL11D	6		C	J3	PL14B	6		
K2	PL9B	3		C	K2	PL12A	6		T*	K2	PL15A	6		T*
K1	PL9C	3			K1	PL12B	6		C*	K1	PL15B	6		C*
L2	GNDIO3	3			L2	GNDIO6	6			L2	GNDIO6	6		
L1	PL10A	3		T	L1	PL14A	6	LLM0_PLLT_FB_A	T*	L1	PL17A	6	LLM0_PLLT_FB_A	T*
L3	PL10B	3		C	L3	PL14B	6	LLM0_PLLC_FB_A	C*	L3	PL17B	6	LLM0_PLLC_FB_A	C*
M1	PL11A	3		T	M1	PL15A	6	LLM0_PLLT_IN_A	T*	M1	PL18A	6	LLM0_PLLT_IN_A	T*
N1	PL11B	3		C	N1	PL16A	6		T	N1	PL19A	6		T
M2	PL11C	3		T	M2	PL15B	6	LLM0_PLLC_IN_A	C*	M2	PL18B	6	LLM0_PLLC_IN_A	C*
P1	PL11D	3		C	P1	PL16B	6		C	P1	PL19B	6		C
P2	GNDIO2	2			P2	GNDIO5	5			P2	GNDIO5	5		
P3	TMS	2	TMS		P3	TMS	5	TMS		P3	TMS	5	TMS	
M3	PB2C	2		T	M3	PB2C	5		T	M3	PB2A	5		T
N3	PB2D	2		C	N3	PB2D	5		C	N3	PB2B	5		C
P4	TCK	2	TCK		P4	TCK	5	TCK		P4	TCK	5	TCK	
M4	PB3B	2			M4	PB3B	5			M4	PB3B	5		
N4	PB3C	2		T	N4	PB4A	5		T	N4	PB4A	5		T
P5	PB3D	2		C	P5	PB4B	5		C	P5	PB4B	5		C
N5	TDO	2	TDO		N5	TDO	5	TDO		N5	TDO	5	TDO	
M5	TDI	2	TDI		M5	TDI	5	TDI		M5	TDI	5	TDI	
N6	PB4E	2		T	N6	PB5C	5			N6	PB6C	5		
P6	VCC	-			P6	VCC	-			P6	VCC	-		
M6	PB4F	2		C	M6	PB6A	5			M6	PB8A	5		
P7	VCCAUX	-			P7	VCCAUX	-			P7	VCCAUX	-		
N7	PB5A	2		T	N7	PB6F	5			N7	PB8F	5		
M7	PB5B	2	PCLK2_1***	C	M7	PB7B	4	PCLK4_1***		M7	PB10F	4	PCLK4_1***	
N8	PB5D	2			N8	PB7C	4		T	N8	PB10C	4		T
P8	PB6A	2		T	P8	PB7D	4		C	P8	PB10D	4		C
M8	PB6B	2	PCLK2_0***	C	M8	PB7F	4	PCLK4_0***		M8	PB10B	4	PCLK4_0***	
N9	PB7A	2		T	N9	PB9A	4		T	N9	PB12A	4		T

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
M9	PB7B	2		C	M9	PB9B	4		C	M9	PB12B	4		C
N10	PB7E	2		T	N10	PB9C	4		T	N10	PB12C	4		T
P10	PB7F	2		C	P10	PB9D	4		C	P10	PB12D	4		C
N11	GNDIO2	2			N11	GNDIO4	4			N11	GNDIO4	4		
P11	PB8C	2		T	P11	PB10A	4		T	P11	PB13C	4		T
M11	PB8D	2		C	M11	PB10B	4		C	M11	PB13D	4		C
P12	PB9C	2		T	P12	PB10C	4			P12	PB15B	4		
P13	PB9D	2		C	P13	PB11C	4		T	P13	PB16C	4		T
N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB11D	4		C	P14	PB16D	4		C
N14	PR11D	1		C	N14	PR16B	3		C	N14	PR19B	3		C
M14	PR11C	1		T	M14	PR15B	3		C*	M14	PR18B	3		C*
N13	PR11B	1		C	N13	PR16A	3		T	N13	PR19A	3		T
M12	PR11A	1		T	M12	PR15A	3		T*	M12	PR18A	3		T*
M13	PR10B	1		C	M13	PR14B	3		C*	M13	PR17B	3		C*
L14	PR10A	1		T	L14	PR14A	3		T*	L14	PR17A	3		T*
L13	GNDIO1	1			L13	GNDIO3	3			L13	GNDIO3	3		
K14	PR8D	1		C	K14	PR12B	3		C*	K14	PR15B	3		C*
K13	PR8C	1		T	K13	PR12A	3		T*	K13	PR15A	3		T*
K12	PR8B	1		C	K12	PR11B	3		C*	K12	PR14B	3		C*
J13	PR8A	1		T	J13	PR11A	3		T*	J13	PR14A	3		T*
J12	PR7C	1			J12	PR10B	3		C*	J12	PR13B	3		C*
H14	PR7B	1		C	H14	PR10A	3		T*	H14	PR13A	3		T*
H13	PR7A	1		T	H13	PR9B	3		C*	H13	PR11B	3		C*
H12	PR6D	1		C	H12	PR9A	3		T*	H12	PR11A	3		T*
G13	PR6C	1		T	G13	PR8B	2		C*	G13	PR10B	2		C*
G14	PR6B	1			G14	PR8A	2		T*	G14	PR10A	2		T*
G12	VCC	-			G12	VCC	-			G12	VCC	-		
F14	PR5D	1		C	F14	PR6C	2			F14	PR8C	2		
F13	PR5C	1		T	F13	PR6B	2		C*	F13	PR8B	2		C*
F12	PR4D	1		C	F12	PR6A	2		T*	F12	PR8A	2		T*
E13	PR4C	1		T	E13	PR5B	2		C*	E13	PR7B	2		C*
E14	PR4B	1			E14	PR5A	2		T*	E14	PR7A	2		T*
D13	GNDIO1	1			D13	GNDIO2	2			D13	GNDIO2	2		
D14	PR3D	1		C	D14	PR4B	2		C*	D14	PR5B	2		C*
D12	PR3C	1		T	D12	PR4A	2		T*	D12	PR5A	2		T*
C14	PR2D	1		C	C14	PR3D	2		C	C14	PR4D	2		C
B14	PR2C	1		T	B14	PR2B	2		C	B14	PR3B	2		C*
C13	PR2B	1		C	C13	PR3C	2		T	C13	PR4C	2		T
A14	PR2A	1		T	A14	PR2A	2		T	A14	PR3A	2		T*
A13	PT9F	0		C	A13	PT11D	1		C	A13	PT16D	1		C
A12	PT9E	0		T	A12	PT11B	1		C	A12	PT16B	1		C
B13	PT9D	0		C	B13	PT11C	1		T	B13	PT16C	1		T
B12	PT9C	0		T	B12	PT10F	1			B12	PT15D	1		
C12	PT9B	0		C	C12	PT11A	1		T	C12	PT16A	1		T
A11	PT9A	0		T	A11	PT10D	1		C	A11	PT14B	1		C
C11	PT8C	0			C11	PT10C	1		T	C11	PT14A	1		T
A10	GNDIO0	0			A10	GNDIO1	1			A10	GNDIO1	1		
B10	PT7F	0		C	B10	PT9F	1		C	B10	PT12F	1		C
C10	PT7E	0		T	C10	PT9E	1		T	C10	PT12E	1		T

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP (Cont.)

	LCMXO640				LCMXO1200				LCMXO2280			
Pin Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
101	PR3D	1		C	PR4B	2		C*	PR5B	2		C*
102	PR3C	1		T	PR4A	2		T*	PR5A	2		T*
103	PR3B	1		C	PR3D	2		C	PR4D	2		C
104	PR2D	1		C	PR3C	2		T	PR4C	2		T
105	PR3A	1		T	PR3B	2		C*	PR4B	2		C*
106	PR2B	1		C	PR3A	2		T*	PR4A	2		T*
107	PR2C	1		T	PR2B	2		C	PR3B	2		C*
108	PR2A	1		T	PR2A	2		T	PR3A	2		T*
109	PT9F	0		C	PT11D	1		C	PT16D	1		C
110	PT9D	0		C	PT11C	1		T	PT16C	1		T
111	PT9E	0		T	PT11B	1		C	PT16B	1		C
112	PT9B	0		C	PT11A	1		T	PT16A	1		T
113	PT9C	0		T	PT10F	1		C	PT15D	1		C
114	PT9A	0		T	PT10E	1		T	PT15C	1		T
115	PT8C	0			PT10D	1		C	PT14B	1		C
116	PT8B	0		C	PT10C	1		T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1			VCCIO1	1		
118	GNDIO0	0			GNDIO1	1			GNDIO1	1		
119	PT8A	0		T	PT9F	1		C	PT12F	1		C
120	PT7E	0			PT9E	1		T	PT12E	1		T
121	PT7C	0			PT9B	1		C	PT12D	1		C
122	PT7A	0			PT9A	1		T	PT12C	1		T
123	GND	-			GND	-			GND	-		
124	PT6B	0	PCLK0_1***	C	PT7D	1	PCLK1_1***		PT10B	1	PCLK1_1***	
125	PT6A	0		T	PT7B	1		C	PT9D	1		C
126	PT5C	0			PT7A	1		T	PT9C	1		T
127	PT5B	0	PCLK0_0***		PT6F	0	PCLK1_0***		PT9B	1	PCLK1_0***	
128	VCCAUX	-			VCCAUX	-			VCCAUX	-		
129	VCC	-			VCC	-			VCC	-		
130	PT4D	0			PT5D	0		C	PT7B	0		C
131	PT4B	0		C	PT5C	0		T	PT7A	0		T
132	PT4A	0		T	PT5B	0		C	PT6D	0		
133	PT3F	0			PT5A	0		T	PT6E	0		T
134	PT3D	0			PT4B	0			PT6F	0		C
135	VCCIO0	0			VCCIO0	0			VCCIO0	0		
136	GNDIO0	0			GNDIO0	0			GNDIO0	0		
137	PT3B	0		C	PT3D	0		C	PT4B	0		T
138	PT2F	0		C	PT3C	0		T	PT4A	0		C
139	PT3A	0		T	PT3B	0		C	PT3B	0		C
140	PT2D	0		C	PT3A	0		T	PT3A	0		T
141	PT2E	0		T	PT2D	0		C	PT2D	0		C
142	PT2B	0		C	PT2C	0		T	PT2C	0		T
143	PT2C	0		T	PT2B	0		C	PT2B	0		C
144	PT2A	0		T	PT2A	0		T	PT2A	0		T

*Supports true LVDS outputs.
**NC for “E” devices.
***Primary clock inputs arer single-ended.

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-3T100C	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMXO2280C-4T100C	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMXO2280C-5T100C	2280	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMXO2280C-3T144C	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO2280C-4T144C	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO2280C-5T144C	2280	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO2280C-3M132C	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO2280C-4M132C	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO2280C-5M132C	2280	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO2280C-3B256C	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMXO2280C-4B256C	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMXO2280C-5B256C	2280	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMXO2280C-3FT256C	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMXO2280C-4FT256C	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMXO2280C-5FT256C	2280	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM
LCMXO2280C-3FT324C	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	COM
LCMXO2280C-4FT324C	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	COM
LCMXO2280C-5FT324C	2280	1.8V/2.5V/3.3V	271	-5	ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3T100C	256	1.2V	78	-3	TQFP	100	COM
LCMXO256E-4T100C	256	1.2V	78	-4	TQFP	100	COM
LCMXO256E-5T100C	256	1.2V	78	-5	TQFP	100	COM
LCMXO256E-3M100C	256	1.2V	78	-3	csBGA	100	COM
LCMXO256E-4M100C	256	1.2V	78	-4	csBGA	100	COM
LCMXO256E-5M100C	256	1.2V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3T100C	640	1.2V	74	-3	TQFP	100	COM
LCMXO640E-4T100C	640	1.2V	74	-4	TQFP	100	COM
LCMXO640E-5T100C	640	1.2V	74	-5	TQFP	100	COM
LCMXO640E-3M100C	640	1.2V	74	-3	csBGA	100	COM
LCMXO640E-4M100C	640	1.2V	74	-4	csBGA	100	COM
LCMXO640E-5M100C	640	1.2V	74	-5	csBGA	100	COM
LCMXO640E-3T144C	640	1.2V	113	-3	TQFP	144	COM
LCMXO640E-4T144C	640	1.2V	113	-4	TQFP	144	COM
LCMXO640E-5T144C	640	1.2V	113	-5	TQFP	144	COM
LCMXO640E-3M132C	640	1.2V	101	-3	csBGA	132	COM
LCMXO640E-4M132C	640	1.2V	101	-4	csBGA	132	COM
LCMXO640E-5M132C	640	1.2V	101	-5	csBGA	132	COM
LCMXO640E-3B256C	640	1.2V	159	-3	caBGA	256	COM
LCMXO640E-4B256C	640	1.2V	159	-4	caBGA	256	COM
LCMXO640E-5B256C	640	1.2V	159	-5	caBGA	256	COM
LCMXO640E-3FT256C	640	1.2V	159	-3	ftBGA	256	COM
LCMXO640E-4FT256C	640	1.2V	159	-4	ftBGA	256	COM
LCMXO640E-5FT256C	640	1.2V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100C	1200	1.2V	73	-3	TQFP	100	COM
LCMXO1200E-4T100C	1200	1.2V	73	-4	TQFP	100	COM
LCMXO1200E-5T100C	1200	1.2V	73	-5	TQFP	100	COM
LCMXO1200E-3T144C	1200	1.2V	113	-3	TQFP	144	COM
LCMXO1200E-4T144C	1200	1.2V	113	-4	TQFP	144	COM
LCMXO1200E-5T144C	1200	1.2V	113	-5	TQFP	144	COM
LCMXO1200E-3M132C	1200	1.2V	101	-3	csBGA	132	COM
LCMXO1200E-4M132C	1200	1.2V	101	-4	csBGA	132	COM
LCMXO1200E-5M132C	1200	1.2V	101	-5	csBGA	132	COM
LCMXO1200E-3B256C	1200	1.2V	211	-3	caBGA	256	COM
LCMXO1200E-4B256C	1200	1.2V	211	-4	caBGA	256	COM
LCMXO1200E-5B256C	1200	1.2V	211	-5	caBGA	256	COM
LCMXO1200E-3FT256C	1200	1.2V	211	-3	ftBGA	256	COM
LCMXO1200E-4FT256C	1200	1.2V	211	-4	ftBGA	256	COM
LCMXO1200E-5FT256C	1200	1.2V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100C	2280	1.2V	73	-3	TQFP	100	COM
LCMXO2280E-4T100C	2280	1.2V	73	-4	TQFP	100	COM
LCMXO2280E-5T100C	2280	1.2V	73	-5	TQFP	100	COM
LCMXO2280E-3T144C	2280	1.2V	113	-3	TQFP	144	COM
LCMXO2280E-4T144C	2280	1.2V	113	-4	TQFP	144	COM
LCMXO2280E-5T144C	2280	1.2V	113	-5	TQFP	144	COM
LCMXO2280E-3M132C	2280	1.2V	101	-3	csBGA	132	COM
LCMXO2280E-4M132C	2280	1.2V	101	-4	csBGA	132	COM
LCMXO2280E-5M132C	2280	1.2V	101	-5	csBGA	132	COM
LCMXO2280E-3B256C	2280	1.2V	211	-3	caBGA	256	COM
LCMXO2280E-4B256C	2280	1.2V	211	-4	caBGA	256	COM
LCMXO2280E-5B256C	2280	1.2V	211	-5	caBGA	256	COM
LCMXO2280E-3FT256C	2280	1.2V	211	-3	ftBGA	256	COM
LCMXO2280E-4FT256C	2280	1.2V	211	-4	ftBGA	256	COM
LCMXO2280E-5FT256C	2280	1.2V	211	-5	ftBGA	256	COM
LCMXO2280E-3FT324C	2280	1.2V	271	-3	ftBGA	324	COM
LCMXO2280E-4FT324C	2280	1.2V	271	-4	ftBGA	324	COM
LCMXO2280E-5FT324C	2280	1.2V	271	-5	ftBGA	324	COM

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For Further Information

A variety of technical notes for the MachXO family are available on the Lattice web site.

- TN1091, MachXO sysIO Usage Guide
- TN1089, MachXO sysCLOCK Design and Usage Guide
- TN1092, Memory Usage Guide for MachXO Devices
- TN1090, Power Estimation and Management for MachXO Devices
- TN1086, MachXO JTAG Programming and Configuration User's Guide
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- TN1097, MachXO Density Migration
- AN8066, Boundary Scan Testability with Lattice sysIO Capability

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- PCI: www.pcisig.com