Welcome to [E-XFL.COM](#)**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

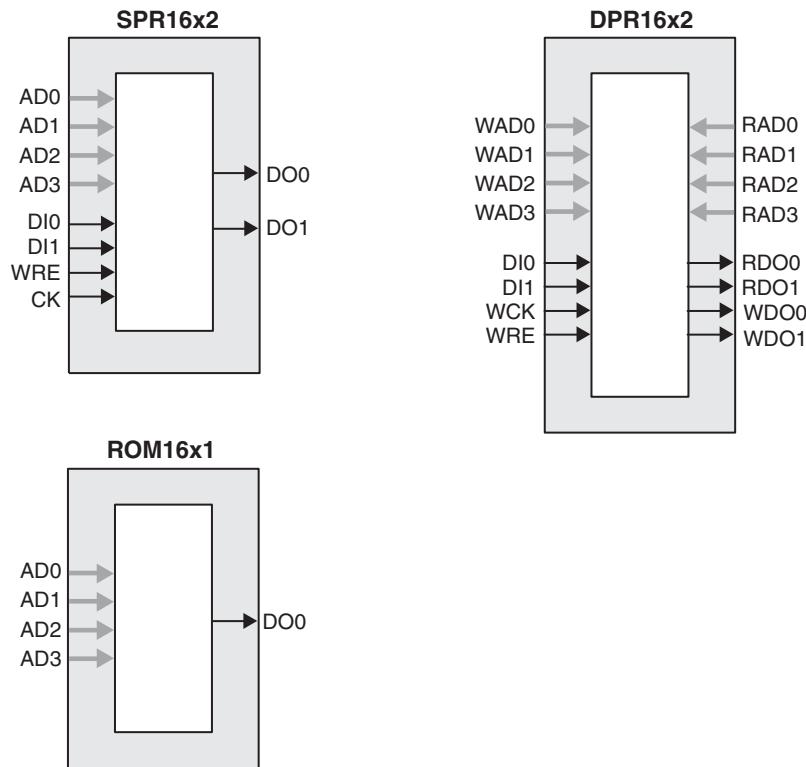
Details

Product Status	Obsolete
Number of LABs/CLBs	285
Number of Logic Elements/Cells	2280
Total RAM Bits	28262
Number of I/O	101
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280e-3m132i

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip, high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Popular logic synthesis tools provide synthesis library support for MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Figure 2-6. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

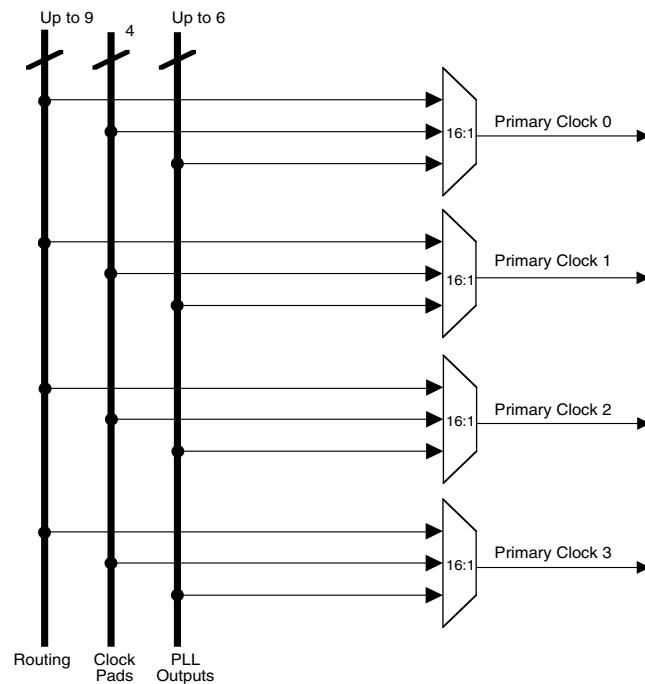
Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

Figure 2-8. Primary Clocks for MachXO1200 and MachXO2280 Devices



Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 2-9. Secondary Clocks for MachXO Devices

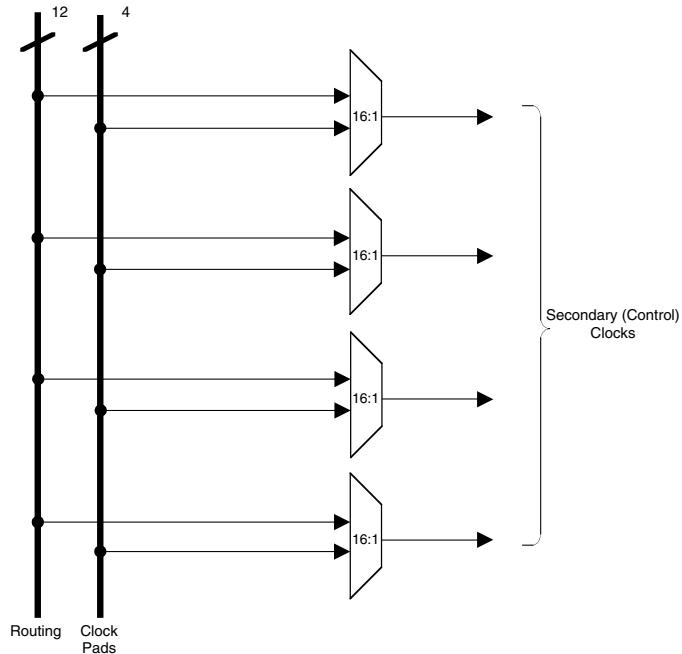


Table 2-8. I/O Support Device by Device

	MachXO256	MachXO640	MachXO1200	MachXO2280
Number of I/O Banks	2	4	8	8
Type of Input Buffers	Single-ended (all I/O Banks)	Single-ended (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)
Differential Output Emulation Capability	All I/O Banks	All I/O Banks	All I/O Banks	All I/O Banks
PCI Support	No	No	Top side only	Top side only

Table 2-9. Supported Input Standards

Input Standard	VCCIO (Typ.)				
	3.3V	2.5V	1.8V	1.5V	1.2V
Single Ended Interfaces					
LVTTL	Yes	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes	Yes
LVCMOS18			Yes		
LVCMOS15				Yes	
LVCMOS12	Yes	Yes	Yes	Yes	Yes
PCI ¹	Yes				
Differential Interfaces					
BLVDS ² , LVDS ² , LVPECL ² , RSDS ²	Yes	Yes	Yes	Yes	Yes

1. Top Banks of MachXO1200 and MachXO2280 devices only.

2. MachXO1200 and MachXO2280 devices only.

Initialization Supply Current^{1, 2, 3, 4}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I _{CC}	Core Power Supply	LCMxo256C	13	mA
		LCMxo640C	17	mA
		LCMxo1200C	21	mA
		LCMxo2280C	23	mA
		LCMxo256E	10	mA
		LCMxo640E	14	mA
		LCMxo1200E	18	mA
		LCMxo2280E	20	mA
I _{CCAUX}	Auxiliary Power Supply V _{CCAUX} = 3.3V	LCMxo256C/E	10	mA
		LCMxo640E/C	13	mA
		LCMxo1200E/C	24	mA
		LCMxo2280E/C	25	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Frequency = 0MHz.
4. Typical user pattern.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank, V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁵	Units
I _{CC}	Core Power Supply	LCMxo256C	9	mA
		LCMxo640C	11	mA
		LCMxo1200C	16	mA
		LCMxo2280C	22	mA
		LCMxo256E	6	mA
		LCMxo640E	8	mA
		LCMxo1200E	12	mA
		LCMxo2280E	14	mA
I _{CCAUX}	Auxiliary Power Supply V _{CCAUX} = 3.3V	LCMxo256C/E	8	mA
		LCMxo640C/E	10	mA
		LCMxo1200/E	15	mA
		LCMxo2280C/E	16	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Typical user pattern.
4. JTAG programming is at 25MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

MachXO Family Timing Adders^{1, 2, 3}

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25 ⁴	LVDS	0.44	0.53	0.61	ns
BLVDS25 ⁴	BLVDS	0.44	0.53	0.61	ns
LVPECL33 ⁴	LVPECL	0.42	0.50	0.59	ns
LVTTL33	LVTTL	0.01	0.01	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	0.01	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	0.07	0.08	0.10	ns
LVCMOS15	LVCMOS 1.5	0.14	0.17	0.19	ns
LVCMOS12	LVCMOS 1.2	0.40	0.48	0.56	ns
PCI33 ⁴	PCI	0.01	0.01	0.01	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E	-0.13	-0.15	-0.18	ns
LVDS25 ⁴	LVDS 2.5	-0.21	-0.26	-0.30	ns
BLVDS25	BLVDS 2.5	-0.03	-0.03	-0.04	ns
LVPECL33	LVPECL 3.3	0.04	0.04	0.05	ns
LVTTL33_4mA	LVTTL 4mA drive	0.04	0.04	0.05	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.07	0.08	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.01	-0.01	-0.01	ns
LVTTL33_16mA	LVTTL 16mA drive	0.50	0.60	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.04	0.04	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.06	0.07	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	-0.01	-0.01	-0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14mA drive	0.50	0.60	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.05	0.06	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.10	0.12	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14mA drive	0.34	0.40	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.11	0.13	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.05	0.06	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	-0.06	-0.07	-0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14mA drive	0.06	0.07	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.15	0.19	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.05	0.06	0.07	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.26	0.31	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.05	0.06	0.07	ns
PCI33 ⁴	PCI33	1.85	2.22	2.59	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

Rev. A 0.19

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D/E/F]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B/C/D/E/F] indicates the PIO within the group to which the pad is connected.</p> <p>Some of these user programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.</p> <p>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-up resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-up resistor enabled.</p>
GSRN	I	Global RESET signal (active low). Dedicated pad, when not in use it can be used as an I/O pin.
TSALL	I	TSALL is a dedicated pad for the global output enable signal. When TSALL is high all the outputs are tristated. It is a dual function pin. When not in use, it can be used as an I/O pin.
NC	—	No connect.
GND	—	GND - Ground. Dedicated pins.
V _{CC}	—	VCC - The power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	VCCAUX - the Auxiliary power supply pin. This pin powers up a variety of internal circuits including all the differential and referenced input buffers. Dedicated pins.
V _{CCIOx}	—	V _{CCIO} - The power supply pins for I/O Bank x. Dedicated pins.
SLEEPN ¹	I	Sleep Mode pin - Active low sleep pin. ^b When this pin is held high, the device operates normally. ^b This pin has a weak internal pull-up, but when unused, an external pull-up to V _{CC} is recommended. When driven low, the device moves into Sleep mode after a specified time.
PLL and Clock Functions (Used as user programmable I/O pins when not used for PLL or clock pins)		
[LOC][0]_PLL[T, C]_IN	—	Reference clock (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
[LOC][0]_PLL[T, C]_FB	—	Optional feedback (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
PCLK [n]_[1:0]	—	Primary Clock Pads, n per side.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin -Test Data output pin used to shift data out of the device using 1149.1.

¹. Applies to MachXO "C" devices only. NC for "E" devices.

Pin Information Summary

Pin Type	LCMxo256C/E		LCMxo640C/E				
	100 TQFP	100 csBGA	100 TQFP	144 TQFP	100 csBGA	132 csBGA	256 caBGA / 256 ftBGA
Single Ended User I/O	78	78	74	113	74	101	159
Differential Pair User I/O ¹	38	38	17	43	17	42	79
Muxed	6	6	6	6	6	6	6
TAP	4	4	4	4	4	4	4
Dedicated (Total Without Supplies)	5	5	5	5	5	5	5
VCC	2	2	2	4	2	4	4
VCCAUX	1	1	1	2	1	2	2
VCCIO	Bank0	3	3	2	2	2	4
	Bank1	3	3	2	2	2	4
	Bank2	—	—	2	2	2	4
	Bank3	—	—	2	2	2	4
GND	8	8	10	12	10	12	18
NC	0	0	0	0	0	0	52
Single Ended/Differential I/O per Bank	Bank0	41/20	41/20	18/5	29/10	18/5	26/11
	Bank1	37/18	37/18	21/4	30/11	21/4	27/12
	Bank2	—	—	14/2	24/9	14/2	21/9
	Bank3	—	—	21/6	30/13	21/6	27/10
							40/20

1. These devices support emulated LVDS outputs.pLVDS inputs are not supported.

Pin Type	LCMxo1200C/E				LCMxo2280C/E				
	100 TQFP	144 TQFP	132 csBGA	256 caBGA / 256 ftBGA	100 TQFP	144 TQFP	132 csBGA	256 caBGA / 256 ftBGA	324 ftBGA
Single Ended User I/O	73	113	101	211	73	113	101	211	271
Differential Pair User I/O ¹	27	48	42	105	30	47	41	105	134
Muxed	6	6	6	6	6	6	6	6	6
TAP	4	4	4	4	4	4	4	4	4
Dedicated (Total Without Supplies)	5	5	5	5	5	5	5	5	5
VCC	4	4	4	4	2	4	4	4	6
VCCAUX	2	2	2	2	2	2	2	2	2
VCCIO	Bank0	1	1	1	2	1	1	1	2
	Bank1	1	1	1	2	1	1	1	2
	Bank2	1	1	1	2	1	1	1	2
	Bank3	1	1	1	2	1	1	1	2
	Bank4	1	1	1	2	1	1	1	2
	Bank5	1	1	1	2	1	1	1	2
	Bank6	1	1	1	2	1	1	1	2
	Bank7	1	1	1	2	1	1	1	2
GND	8	12	12	18	8	12	12	18	24
NC	0	0	0	0	0	0	0	0	0
Single Ended/Differential I/O per Bank	Bank0	10/3	14/6	13/5	26/13	9/3	13/6	12/5	24/12
	Bank1	8/2	15/7	13/5	28/14	9/3	16/7	14/5	30/15
	Bank2	10/4	15/7	13/6	26/13	10/4	15/7	13/6	26/13
	Bank3	11/5	15/7	14/7	28/14	11/5	15/7	14/7	28/14
	Bank4	8/3	14/5	13/5	27/13	8/3	14/4	13/4	29/14
	Bank5	5/2	10/4	8/2	22/11	5/2	10/4	8/2	20/10
	Bank6	10/3	15/6	13/6	28/14	10/4	15/6	13/6	28/14
	Bank7	11/5	15/6	14/6	26/13	11/5	15/6	14/6	26/13

1. These devices support on-chip LVDS buffers for left and right I/O Banks.

LCMxo256 and LCMxo640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMxo256				LCMxo640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for "E" devices.

** Primary clock inputs are single-ended.

LCMxo1200 and LCMxo2280 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
82	PT9A	1			PT12C	1		T
83	GND	-			GND	-		
84	PT8B	1		C	PT11B	1		C
85	PT8A	1		T	PT11A	1		T
86	PT7D	1	PCLK1_1****		PT10B	1	PCLK1_1****	
87	PT6F	0	PCLK0_0****		PT9B	1	PCLK1_0****	
88	PT6D	0		C	PT8F	0		C
89	PT6C	0		T	PT8E	0		T
90	VCCAUX	-			VCCAUX	-		
91	VCC	-			VCC	-		
92	PT5B	0			PT6D	0		
93	PT4B	0			PT6F	0		
94	VCCIO0	0			VCCIO0	0		
95	PT3D	0		C	PT4B	0		C
96	PT3C	0		T	PT4A	0		T
97	PT3B	0			PT3B	0		
98	PT2B	0		C	PT2B	0		C
99	PT2A	0		T	PT2A	0		T
100**	GNDIO0 GNDIO7	-			GNDIO0 GNDIO7	-		

*Supports true LVDS outputs.

**Double bonded to the pin.

***NC for "E" devices.

****Primary clock inputs are single-ended.

LCMxo256 and LCMxo640 Logic Signal Connections: 100 csBGA

LCMxo256					LCMxo640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
B1	PL2A	1		T	B1	PL2A	3		T
C1	PL2B	1		C	C1	PL2C	3		T
D2	PL3A	1		T	D2	PL2B	3		C
D1	PL3B	1		C	D1	PL2D	3		C
C2	PL3C	1		T	C2	PL3A	3		T
E1	PL3D	1		C	E1	PL3B	3		C
E2	PL4A	1		T	E2	PL3C	3		T
F1	PL4B	1		C	F1	PL3D	3		C
F2	PL5A	1		T	F2	PL4A	3		
G2	PL5B	1		C	G2	PL4C	3		T
H1	GNDIO1	1			H1	GNDIO3	3		
H2	PL5C	1		T	H2	PL4D	3		C
J1	PL5D	1	GSRN	C	J1	PL5B	3	GSRN	
J2	PL6A	1		T	J2	PL7B	3		
K1	PL6B	1	TSALL	C	K1	PL8C	3	TSALL	T
K2	PL7A	1		T	K2	PL8D	3		C
L1	PL7B	1		C	L1	PL9A	3		
L2	PL7C	1		T	L2	PL9C	3		
M1	PL7D	1		C	M1	PL10A	3		
M2	PL8A	1		T	M2	PL10C	3		
N1	PL8B	1		C	N1	PL11A	3		
M3	PL9A	1		T	M3	PL11C	3		
N2	GNDIO1	1			N2	GNDIO3	3		
P2	TMS	1	TMS		P2	TMS	2	TMS	
P3	PL9B	1		C	P3	PB2C	2		
N4	TCK	1	TCK		N4	TCK	2	TCK	
P4	PB2A	1		T	P4	VCCIO2	2		
N3	PB2B	1		C	N3	GNDIO2	2		
P5	TDO	1	TDO		P5	TDO	2	TDO	
N5	PB2C	1		T	N5	PB4C	2		
P6	TDI	1	TDI		P6	TDI	2	TDI	
N6	PB2D	1		C	N6	PB4E	2		
P7	VCC	-			P7	VCC	-		
N7	PB3A	1	PCLK1_1**	T	N7	PB5B	2	PCLK2_1**	
P8	PB3B	1		C	P8	PB5D	2		
N8	PB3C	1	PCLK1_0**	T	N8	PB6B	2	PCLK2_0**	
P9	PB3D	1		C	P9	PB6C	2		
N10	GNDIO1	1			N10	GNDIO2	2		
P11	PB4A	1		T	P11	PB8B	2		
N11	PB4B	1		C	N11	PB8C	2		T
P12	PB4C	1		T	P12	PB8D	2		C
N12	PB4D	1		C	N12	PB9A	2		

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 144 TQFP (Cont.)**

Pin Number	LCMxo640				LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
51	TDI	2	TDI		TDI	5	TDI		TDI	5	TDI	
52	VCC	-			VCC	-			VCC	-		
53	VCCAUX	-			VCCAUX	-			VCCAUX	-		
54	PB5A	2		T	PB6F	5			PB8F	5		
55	PB5B	2	PCLKT2_1***	C	PB7B	4	PCLK4_1***		PB10F	4	PCLK4_1***	
56	PB5D	2			PB7C	4			PB10C	4		T
57	PB6A	2		T	PB7D	4			PB10D	4		C
58	PB6B	2	PCLKT2_0***	C	PB7F	4	PCLK4_0***		PB10B	4	PCLK4_0***	
59	GND	-			GND	-			GND	-		
60	PB7C	2			PB9A	4			PB12A	4		T
61	PB7E	2			PB9B	4			PB12B	4		C
62	PB8A	2			PB9E	4			PB12E	4		
63	VCCIO2	2			VCCIO4	4			VCCIO4	4		
64	GNDIO2	2			GNDIO4	4			GNDIO4	4		
65	PB8C	2		T	PB10A	4			PB13A	4		T
66	PB8D	2		C	PB10B	4			PB13B	4		C
67	PB9A	2		T	PB10C	4			PB13C	4		T
68	PB9C	2		T	PB10D	4			PB13D	4		C
69	PB9B	2		C	PB10F	4			PB14D	4		
70**	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
71	PB9D	2		C	PB11C	4			PB16C	4		T
72	PB9F	2			PB11D	4			PB16D	4		C
73	PR11D	1		C	PR16B	3			PR20B	3		C
74	PR11B	1		C	PR16A	3			PR20A	3		T
75	PR11C	1		T	PR15B	3			PR19B	3		C
76	PR10D	1		C	PR15A	3			PR19A	3		T
77	PR11A	1		T	PR14D	3			PR17D	3		C
78	PR10B	1		C	PR14C	3			PR17C	3		T
79	PR10C	1		T	PR14B	3			PR17B	3		C*
80	PR10A	1		T	PR14A	3			PR17A	3		T*
81	PR9D	1			PR13D	3			PR16D	3		
82	VCCIO1	1			VCCIO3	3			VCCIO3	3		
83	GNDIO1	1			GNDIO3	3			GNDIO3	3		
84	PR9A	1			PR12B	3			PR15B	3		C*
85	PR8C	1			PR12A	3			PR15A	3		T*
86	PR8A	1			PR11B	3			PR14B	3		C*
87	PR7D	1			PR11A	3			PR14A	3		T*
88	GND	-			GND	-			GND	-		
89	PR7B	1		C	PR10B	3			PR13B	3		C*
90	PR7A	1		T	PR10A	3			PR13A	3		T*
91	PR6D	1		C	PR8B	2			PR10B	2		C*
92	PR6C	1		T	PR8A	2			PR10A	2		T*
93	VCC	-			VCC	-			VCC	-		
94	PR5D	1			PR6B	2			PR8B	2		C*
95	PR5B	1			PR6A	2			PR8A	2		T*
96	PR4D	1			PR5B	2			PR7B	2		C*
97	PR4B	1		C	PR5A	2			PR7A	2		T*
98	VCCIO1	1			VCCIO2	2			VCCIO2	2		
99	GNDIO1	1			GNDIO2	2			GNDIO2	2		
100	PR4A	1		T	PR4C	2			PR5C	2		

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 144 TQFP (Cont.)**

Pin Number	LCMxo640				LCMxo1200				LCMxo2280				
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	
101	PR3D	1		C	PR4B	2			C*	PR5B	2		C*
102	PR3C	1		T	PR4A	2			T*	PR5A	2		T*
103	PR3B	1		C	PR3D	2			C	PR4D	2		C
104	PR2D	1		C	PR3C	2			T	PR4C	2		T
105	PR3A	1		T	PR3B	2			C*	PR4B	2		C*
106	PR2B	1		C	PR3A	2			T*	PR4A	2		T*
107	PR2C	1		T	PR2B	2			C	PR3B	2		C*
108	PR2A	1		T	PR2A	2			T	PR3A	2		T*
109	PT9F	0		C	PT11D	1			C	PT16D	1		C
110	PT9D	0		C	PT11C	1			T	PT16C	1		T
111	PT9E	0		T	PT11B	1			C	PT16B	1		C
112	PT9B	0		C	PT11A	1			T	PT16A	1		T
113	PT9C	0		T	PT10F	1			C	PT15D	1		C
114	PT9A	0		T	PT10E	1			T	PT15C	1		T
115	PT8C	0			PT10D	1			C	PT14B	1		C
116	PT8B	0		C	PT10C	1			T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1				VCCIO1	1		
118	GNDIO0	0			GNDIO1	1				GNDIO1	1		
119	PT8A	0		T	PT9F	1			C	PT12F	1		C
120	PT7E	0			PT9E	1			T	PT12E	1		T
121	PT7C	0			PT9B	1			C	PT12D	1		C
122	PT7A	0			PT9A	1			T	PT12C	1		T
123	GND	-			GND	-				GND	-		
124	PT6B	0	PCLK0_1***	C	PT7D	1	PCLK1_1***			PT10B	1	PCLK1_1***	
125	PT6A	0		T	PT7B	1			C	PT9D	1		C
126	PT5C	0			PT7A	1			T	PT9C	1		T
127	PT5B	0	PCLK0_0***		PT6F	0	PCLK1_0***			PT9B	1	PCLK1_0***	
128	VCCAUX	-			VCCAUX	-				VCCAUX	-		
129	VCC	-			VCC	-				VCC	-		
130	PT4D	0			PT5D	0			C	PT7B	0		C
131	PT4B	0		C	PT5C	0			T	PT7A	0		T
132	PT4A	0		T	PT5B	0			C	PT6D	0		
133	PT3F	0			PT5A	0			T	PT6E	0		T
134	PT3D	0			PT4B	0				PT6F	0		C
135	VCCIO0	0			VCCIO0	0				VCCIO0	0		
136	GNDIO0	0			GNDIO0	0				GNDIO0	0		
137	PT3B	0		C	PT3D	0			C	PT4B	0		T
138	PT2F	0		C	PT3C	0			T	PT4A	0		C
139	PT3A	0		T	PT3B	0			C	PT3B	0		C
140	PT2D	0		C	PT3A	0			T	PT3A	0		T
141	PT2E	0		T	PT2D	0			C	PT2D	0		C
142	PT2B	0		C	PT2C	0			T	PT2C	0		T
143	PT2C	0		T	PT2B	0			C	PT2B	0		C
144	PT2A	0		T	PT2A	0			T	PT2A	0		T

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
-	-				VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
-	-				GND	GNDIO4	4			GND	GNDIO4	4		
M10	PB6A	2		T	M10	PB7E	4			M10	PB10A	4		T
R9	PB6C	2		T	R9	PB8A	4			R9	PB11C	4		T
R10	PB6D	2		C	R10	PB8B	4			R10	PB11D	4		C
T10	PB7C	2		T	T10	PB8C	4			T10	PB12A	4		T
T11	PB7D	2		C	T11	PB8D	4			T11	PB12B	4		C
N10	NC				N10	PB8E	4			N10	PB12C	4		T
N11	NC				N11	PB8F	4			N11	PB12D	4		C
VCCIO2	VCCIO2	2			VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
GND	GNDIO2	2			GND	GNDIO4	4			GND	GNDIO4	4		
R11	PB7E	2		T	R11	PB9A	4			R11	PB13A	4		T
R12	PB7F	2		C	R12	PB9B	4			R12	PB13B	4		C
P11	PB8A	2		T	P11	PB9C	4			P11	PB13C	4		T
P12	PB8B	2		C	P12	PB9D	4			P12	PB13D	4		C
T13	PB8C	2		T	T13	PB9E	4			T13	PB14A	4		T
T12	PB8D	2		C	T12	PB9F	4			T12	PB14B	4		C
R13	PB9A	2		T	R13	PB10A	4			R13	PB14C	4		T
R14	PB9B	2		C	R14	PB10B	4			R14	PB14D	4		C
GND	GND	-			GND	GND	-			GND	GND	-		
T14	PB9C	2		T	T14	PB10C	4			T14	PB15A	4		T
T15	PB9D	2		C	T15	PB10D	4			T15	PB15B	4		C
P13**	SLEEPN	-	SLEEPN		P13**	SLEEPN	-	SLEEPN		P13**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB10F	4			P14	PB15D	4		
R15	NC				R15	PB11A	4			R15	PB16A	4		T
R16	NC				R16	PB11B	4			R16	PB16B	4		C
P15	NC				P15	PB11C	4			P15	PB16C	4		T
P16	NC				P16	PB11D	4			P16	PB16D	4		C
VCCIO2	VCCIO2	2			VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
GND	GNDIO2	2			GND	GNDIO4	4			GND	GNDIO4	4		
GND	GNDIO1	1			GND	GNDIO3	3			GND	GNDIO3	3		
VCCIO1	VCCIO1	1			VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
M11	NC				M11	PR16B	3			M11	PR20B	3		C
L11	NC				L11	PR16A	3			L11	PR20A	3		T
N12	NC				N12	PR15B	3			N12	PR18B	3		C*
N13	NC				N13	PR15A	3			N13	PR18A	3		T*
M13	NC				M13	PR14D	3			M13	PR17D	3		C
M12	NC				M12	PR14C	3			M12	PR17C	3		T
N14	PR11D	1		C	N14	PR14B	3			N14	PR17B	3		C*
N15	PR11C	1		T	N15	PR14A	3			N15	PR17A	3		T*
L13	PR11B	1		C	L13	PR13D	3			L13	PR16D	3		C
L12	PR11A	1		T	L12	PR13C	3			L12	PR16C	3		T
M14	PR10B	1		C	M14	PR13B	3			M14	PR16B	3		C*
VCCIO1	VCCIO1	1			VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
GND	GNDIO1	1			GND	GNDIO3	3			GND	GNDIO3	3		
L14	PR10A	1		T	L14	PR13A	3			L14	PR16A	3		T*
N16	PR10D	1		C	N16	PR12D	3			N16	PR15D	3		C
M16	PR10C	1		T	M16	PR12C	3			M16	PR15C	3		T
M15	PR9D	1		C	M15	PR12B	3			M15	PR15B	3		C*
L15	PR9C	1		T	L15	PR12A	3			L15	PR15A	3		T*
L16	PR9B	1		C	L16	PR11D	3			L16	PR14D	3		C
K16	PR9A	1		T	K16	PR11C	3			K16	PR14C	3		T
K13	PR8D	1		C	K13	PR11B	3			K13	PR14B	3		C*

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200				LCMxo2280					
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E11	NC				E11	PT10D	1		C	E11	PT15B	1		C
E10	NC				E10	PT10C	1		T	E10	PT15A	1		T
D12	PT9D	0		C	D12	PT10B	1		C	D12	PT14D	1		C
D11	PT9C	0		T	D11	PT10A	1		T	D11	PT14C	1		T
A14	PT7F	0		C	A14	PT9F	1		C	A14	PT14B	1		C
A13	PT7E	0		T	A13	PT9E	1		T	A13	PT14A	1		T
C12	PT8B	0		C	C12	PT9D	1		C	C12	PT13D	1		C
C11	PT8A	0		T	C11	PT9C	1		T	C11	PT13C	1		T
-	-			VCCIO1	VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-			GND	GNDIO1	GNDIO1	1			GND	GNDIO1	1		
B12	PT7B	0		C	B12	PT9B	1		C	B12	PT12D	1		C
B11	PT7A	0		T	B11	PT9A	1		T	B11	PT12C	1		T
A12	PT7D	0		C	A12	PT8F	1		C	A12	PT12B	1		C
A11	PT7C	0		T	A11	PT8E	1		T	A11	PT12A	1		T
GND	GND	-		GND	GND	GND	-			GND	GND	-		
B10	PT5D	0		C	B10	PT8D	1		C	B10	PT11B	1		C
B9	PT5C	0		T	B9	PT8C	1		T	B9	PT11A	1		T
D10	PT8D	0		C	D10	PT8B	1		C	D10	PT10F	1		C
D9	PT8C	0		T	D9	PT8A	1		T	D9	PT10E	1		T
-	-			VCCIO1	VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-			GND	GNDIO1	GNDIO1	1			GND	GNDIO1	1		
C10	PT6D	0		C	C10	PT7F	1		C	C10	PT10D	1		C
C9	PT6C	0		T	C9	PT7E	1		T	C9	PT10C	1		T
A9	PT6B	0	PCLK0_1***	C	A9	PT7D	1	PCLK1_1***	C	A9	PT10B	1	PCLK1_1***	C
A10	PT6A	0		T	A10	PT7C	1		T	A10	PT10A	1		T
E9	PT9B	0		C	E9	PT7B	1		C	E9	PT9D	1		C
E8	PT9A	0		T	E8	PT7A	1		T	E8	PT9C	1		T
D7	PT5B	0	PCLK0_0***	C	D7	PT6F	0	PCLK1_0***	C	D7	PT9B	1	PCLK1_0***	C
D8	PT5A	0		T	D8	PT6E	0		T	D8	PT9A	1		T
VCCIO0	VCCIO0	0		VCCIO0	VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0		GND	GNDIO0	GNDIO0	0			GND	GNDIO0	0		
C8	PT4F	0		C	C8	PT6D	0		C	C8	PT8D	0		C
B8	PT4E	0		T	B8	PT6C	0		T	B8	PT8C	0		T
A8	VCCAUX	-		A8	VCCAUX	VCCAUX	-			A8	VCCAUX	-		
A7	PT4D	0		C	A7	PT6B	0		C	A7	PT7D	0		C
A6	PT4C	0		T	A6	PT6A	0		T	A6	PT7C	0		T
VCC	VCC	-		VCC	VCC	VCC	-			VCC	VCC	-		
B7	PT4B	0		C	B7	PT5F	0		C	B7	PT7B	0		C
B6	PT4A	0		T	B6	PT5E	0		T	B6	PT7A	0		T
C6	PT3C	0		T	C6	PT5C	0		T	C6	PT6A	0		T
C7	PT3D	0		C	C7	PT5D	0		C	C7	PT6B	0		C
A5	PT3E	0		T	A5	PT5A	0		T	A5	PT6C	0		T
A4	PT3F	0		C	A4	PT5B	0		C	A4	PT6D	0		C
E7	NC			E7	PT4C	0		T	E7	PT6E	0		T	
E6	NC			E6	PT4D	0		C	E6	PT6F	0		C	
B5	PT3B	0		C	B5	PT3F	0		C	B5	PT5D	0		C
B4	PT3A	0		T	B4	PT3E	0		T	B4	PT5C	0		T
D5	PT2D	0		C	D5	PT3D	0		C	D5	PT5B	0		C
D6	PT2C	0		T	D6	PT3C	0		T	D6	PT5A	0		T
C4	PT2E	0		T	C4	PT4A	0		T	C4	PT4A	0		T
C5	PT2F	0		C	C5	PT4B	0		C	C5	PT4B	0		C
-	-	-		-	-	-	-			GND	GND	-		
D4	NC			D4	PT2D	0		C	D4	PT3D	0		C	

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280C-3T100C	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMxo2280C-4T100C	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMxo2280C-5T100C	2280	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMxo2280C-3T144C	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMxo2280C-4T144C	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMxo2280C-5T144C	2280	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMxo2280C-3M132C	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMxo2280C-4M132C	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMxo2280C-5M132C	2280	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMxo2280C-3B256C	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMxo2280C-4B256C	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMxo2280C-5B256C	2280	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMxo2280C-3FT256C	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMxo2280C-4FT256C	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMxo2280C-5FT256C	2280	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM
LCMxo2280C-3FT324C	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	COM
LCMxo2280C-4FT324C	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	COM
LCMxo2280C-5FT324C	2280	1.8V/2.5V/3.3V	271	-5	ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256E-3T100C	256	1.2V	78	-3	TQFP	100	COM
LCMxo256E-4T100C	256	1.2V	78	-4	TQFP	100	COM
LCMxo256E-5T100C	256	1.2V	78	-5	TQFP	100	COM
LCMxo256E-3M100C	256	1.2V	78	-3	csBGA	100	COM
LCMxo256E-4M100C	256	1.2V	78	-4	csBGA	100	COM
LCMxo256E-5M100C	256	1.2V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640E-3T100C	640	1.2V	74	-3	TQFP	100	COM
LCMxo640E-4T100C	640	1.2V	74	-4	TQFP	100	COM
LCMxo640E-5T100C	640	1.2V	74	-5	TQFP	100	COM
LCMxo640E-3M100C	640	1.2V	74	-3	csBGA	100	COM
LCMxo640E-4M100C	640	1.2V	74	-4	csBGA	100	COM
LCMxo640E-5M100C	640	1.2V	74	-5	csBGA	100	COM
LCMxo640E-3T144C	640	1.2V	113	-3	TQFP	144	COM
LCMxo640E-4T144C	640	1.2V	113	-4	TQFP	144	COM
LCMxo640E-5T144C	640	1.2V	113	-5	TQFP	144	COM
LCMxo640E-3M132C	640	1.2V	101	-3	csBGA	132	COM
LCMxo640E-4M132C	640	1.2V	101	-4	csBGA	132	COM
LCMxo640E-5M132C	640	1.2V	101	-5	csBGA	132	COM
LCMxo640E-3B256C	640	1.2V	159	-3	caBGA	256	COM
LCMxo640E-4B256C	640	1.2V	159	-4	caBGA	256	COM
LCMxo640E-5B256C	640	1.2V	159	-5	caBGA	256	COM
LCMxo640E-3FT256C	640	1.2V	159	-3	ftBGA	256	COM
LCMxo640E-4FT256C	640	1.2V	159	-4	ftBGA	256	COM
LCMxo640E-5FT256C	640	1.2V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200E-3T100C	1200	1.2V	73	-3	TQFP	100	COM
LCMxo1200E-4T100C	1200	1.2V	73	-4	TQFP	100	COM
LCMxo1200E-5T100C	1200	1.2V	73	-5	TQFP	100	COM
LCMxo1200E-3T144C	1200	1.2V	113	-3	TQFP	144	COM
LCMxo1200E-4T144C	1200	1.2V	113	-4	TQFP	144	COM
LCMxo1200E-5T144C	1200	1.2V	113	-5	TQFP	144	COM
LCMxo1200E-3M132C	1200	1.2V	101	-3	csBGA	132	COM
LCMxo1200E-4M132C	1200	1.2V	101	-4	csBGA	132	COM
LCMxo1200E-5M132C	1200	1.2V	101	-5	csBGA	132	COM
LCMxo1200E-3B256C	1200	1.2V	211	-3	caBGA	256	COM
LCMxo1200E-4B256C	1200	1.2V	211	-4	caBGA	256	COM
LCMxo1200E-5B256C	1200	1.2V	211	-5	caBGA	256	COM
LCMxo1200E-3FT256C	1200	1.2V	211	-3	ftBGA	256	COM
LCMxo1200E-4FT256C	1200	1.2V	211	-4	ftBGA	256	COM
LCMxo1200E-5FT256C	1200	1.2V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280E-3T100C	2280	1.2V	73	-3	TQFP	100	COM
LCMxo2280E-4T100C	2280	1.2V	73	-4	TQFP	100	COM
LCMxo2280E-5T100C	2280	1.2V	73	-5	TQFP	100	COM
LCMxo2280E-3T144C	2280	1.2V	113	-3	TQFP	144	COM
LCMxo2280E-4T144C	2280	1.2V	113	-4	TQFP	144	COM
LCMxo2280E-5T144C	2280	1.2V	113	-5	TQFP	144	COM
LCMxo2280E-3M132C	2280	1.2V	101	-3	csBGA	132	COM
LCMxo2280E-4M132C	2280	1.2V	101	-4	csBGA	132	COM
LCMxo2280E-5M132C	2280	1.2V	101	-5	csBGA	132	COM
LCMxo2280E-3B256C	2280	1.2V	211	-3	caBGA	256	COM
LCMxo2280E-4B256C	2280	1.2V	211	-4	caBGA	256	COM
LCMxo2280E-5B256C	2280	1.2V	211	-5	caBGA	256	COM
LCMxo2280E-3FT256C	2280	1.2V	211	-3	ftBGA	256	COM
LCMxo2280E-4FT256C	2280	1.2V	211	-4	ftBGA	256	COM
LCMxo2280E-5FT256C	2280	1.2V	211	-5	ftBGA	256	COM
LCMxo2280E-3FT324C	2280	1.2V	271	-3	ftBGA	324	COM
LCMxo2280E-4FT324C	2280	1.2V	271	-4	ftBGA	324	COM
LCMxo2280E-5FT324C	2280	1.2V	271	-5	ftBGA	324	COM

Conventional Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3T100I	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	IND
LCMxo256C-4T100I	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	IND
LCMxo256C-3M100I	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	IND
LCMxo256C-4M100I	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3T100I	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	IND
LCMxo640C-4T100I	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	IND
LCMxo640C-3M100I	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	IND
LCMxo640C-4M100I	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	IND
LCMxo640C-3T144I	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo640C-4T144I	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo640C-3M132I	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo640C-4M132I	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo640C-3B256I	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	IND
LCMxo640C-4B256I	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	IND
LCMxo640C-3FT256I	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	IND
LCMxo640C-4FT256I	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3T100I	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo1200C-4T100I	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo1200C-3T144I	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo1200C-4T144I	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo1200C-3M132I	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo1200C-4M132I	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo1200C-3B256I	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo1200C-4B256I	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo1200C-3FT256I	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo1200C-4FT256I	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280C-3T100I	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo2280C-4T100I	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo2280C-3T144I	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo2280C-4T144I	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo2280C-3M132I	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo2280C-4M132I	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo2280C-3B256I	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo2280C-4B256I	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo2280C-3FT256I	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo2280C-4FT256I	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND
LCMxo2280C-3FT324I	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	IND
LCMxo2280C-4FT324I	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256E-3TN100I	256	1.2V	78	-3	Lead-Free TQFP	100	IND
LCMxo256E-4TN100I	256	1.2V	78	-4	Lead-Free TQFP	100	IND
LCMxo256E-3MN100I	256	1.2V	78	-3	Lead-Free csBGA	100	IND
LCMxo256E-4MN100I	256	1.2V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640E-3TN100I	640	1.2V	74	-3	Lead-Free TQFP	100	IND
LCMxo640E-4TN100I	640	1.2V	74	-4	Lead-Free TQFP	100	IND
LCMxo640E-3MN100I	640	1.2V	74	-3	Lead-Free csBGA	100	IND
LCMxo640E-4MN100I	640	1.2V	74	-4	Lead-Free csBGA	100	IND
LCMxo640E-3TN144I	640	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMxo640E-4TN144I	640	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMxo640E-3MN132I	640	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMxo640E-4MN132I	640	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMxo640E-3BN256I	640	1.2V	159	-3	Lead-Free caBGA	256	IND
LCMxo640E-4BN256I	640	1.2V	159	-4	Lead-Free caBGA	256	IND
LCMxo640E-3FTN256I	640	1.2V	159	-3	Lead-Free ftBGA	256	IND
LCMxo640E-4FTN256I	640	1.2V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200E-3TN100I	1200	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMxo1200E-4TN100I	1200	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMxo1200E-3TN144I	1200	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMxo1200E-4TN144I	1200	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMxo1200E-3MN132I	1200	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMxo1200E-4MN132I	1200	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMxo1200E-3BN256I	1200	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMxo1200E-4BN256I	1200	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMxo1200E-3FTN256I	1200	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMxo1200E-4FTN256I	1200	1.2V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280E-3TN100I	2280	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMxo2280E-4TN100I	2280	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMxo2280E-3TN144I	2280	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMxo2280E-4TN144I	2280	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMxo2280E-3MN132I	2280	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMxo2280E-4MN132I	2280	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMxo2280E-3BN256I	2280	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMxo2280E-4BN256I	2280	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMxo2280E-3FTN256I	2280	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMxo2280E-4FTN256I	2280	1.2V	211	-4	Lead-Free ftBGA	256	IND
LCMxo2280E-3FTN324I	2280	1.2V	271	-3	Lead-Free ftBGA	324	IND
LCMxo2280E-4FTN324I	2280	1.2V	271	-4	Lead-Free ftBGA	324	IND



MachXO Family Data Sheet

Revision History

June 2013

Data Sheet DS1002

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
October 2005	01.1	Introduction	Distributed RAM information in family table updated. Added footnote 1 - fpBGA packaging to the family selection guide.
		Architecture	sysIO Buffer section updated.
			Hot Socketing section updated.
			Sleep Mode section updated.
			SLEEP Pin Characteristics section updated.
			Oscillator section updated.
		DC and Switching Characteristics	Security section updated.
			Recommended Operating Conditions table updated.
			DC Electrical Characteristics table updated.
			Supply Current (Sleep Mode) table added with LCMXO256/640 data.
			Supply Current (Standby) table updated with LCMXO256/640 data.
			Initialization Supply Current table updated with LCMXO256/640 data.
			Programming and Erase Flash Supply Current table updated with LCMXO256/640 data.
			Register-to-Register Performance table updated (rev. A 0.16).
			External Switching Characteristics table updated (rev. A 0.16).
			Internal Timing Parameter table updated (rev. A 0.16).
			Family Timing Adders updated (rev. A 0.16).
			sysCLOCK Timingupdated (rev. A 0.16).
			MachXO "C" Sleep Mode Timing updated (A 0.16).
		Pinout Information	JTAG Port Timing Specification updated (rev. A 0.16).
			SLEEPIN description updated.
			Pin Information Summary updated.
			Power Supply and NC Connection table has been updated.
		Ordering Information	Logic Signal Connection section has been updated to include all devices/packages.
			Part Number Description section has been updated.
			Ordering Part Number section has been updated (added LCMXO256C/ LCMXO640C "4W").
		Supplemental Information	MachXO Density Migration Technical Note (TN1097) added.
November 2005	01.2	Pinout Information	Added "Power Supply and NC Connections" summary information for LCMXO1200 and LCMXO2280 in 100 TQFP package.
December 2005	01.3	DC and Switching Characteristics	Supply Current (Standby) table updated with LCMXO1200/2280 data.
		Ordering Information	Ordering Part Number section updated (added LCMXO2280C "4W").
April 2006	02.0	Introduction	Introduction paragraphs updated.
		Architecture	Architecture Overview paragraphs updated.

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