



Welcome to [E·XFL.COM](https://www.e-xfl.com)

## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

|                                |                                                                                                                                                                           |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                                                    |
| Number of LABs/CLBs            | 285                                                                                                                                                                       |
| Number of Logic Elements/Cells | 2280                                                                                                                                                                      |
| Total RAM Bits                 | 28262                                                                                                                                                                     |
| Number of I/O                  | 73                                                                                                                                                                        |
| Number of Gates                | -                                                                                                                                                                         |
| Voltage - Supply               | 1.14V ~ 1.26V                                                                                                                                                             |
| Mounting Type                  | Surface Mount                                                                                                                                                             |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                                                        |
| Package / Case                 | 100-LQFP                                                                                                                                                                  |
| Supplier Device Package        | 100-TQFP (14x14)                                                                                                                                                          |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280e-3tn100i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280e-3tn100i</a> |

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- **Sleep Mode**
  - Allows up to 100x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **High I/O to Logic Density**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.7 Kbits distributed RAM
  - Dedicated FIFO control logic

- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTTL
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide, and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - Onboard oscillator
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
  - IEEE 1532 compliant in-system programming

## Introduction

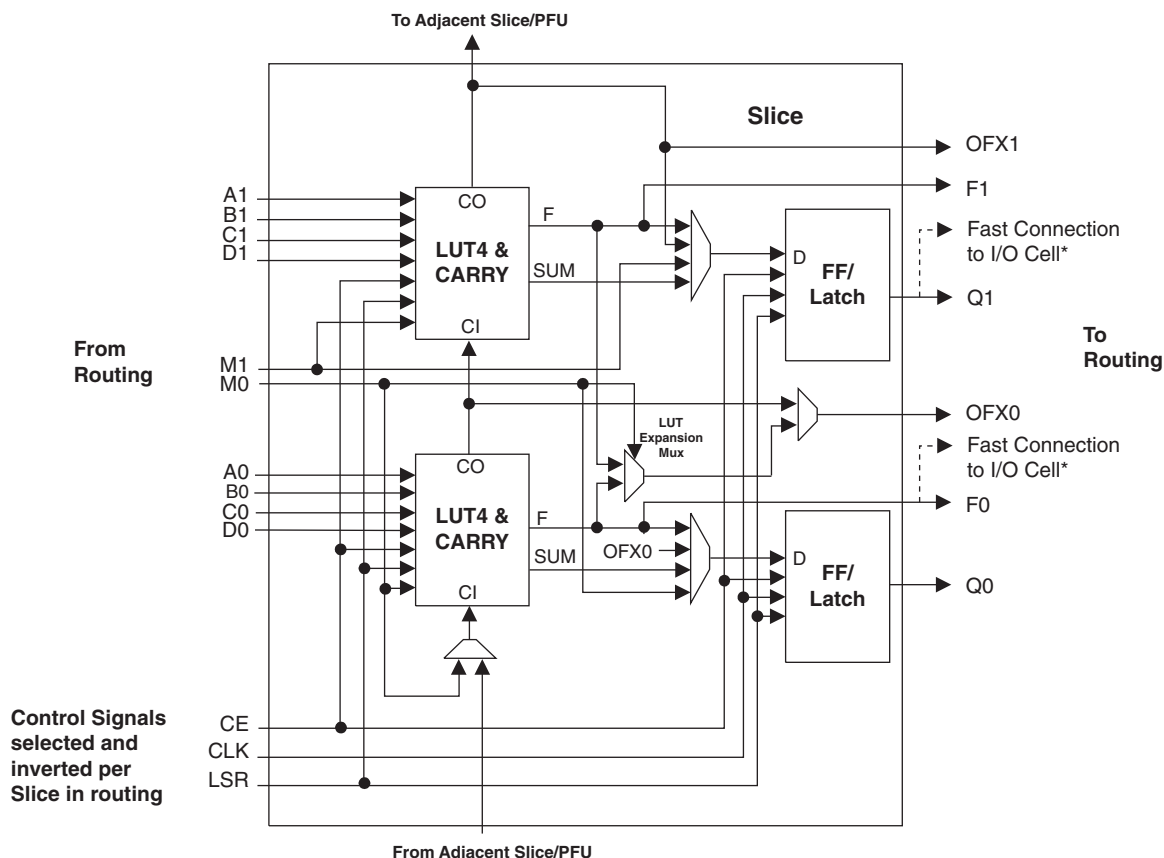
The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, and control logic. These devices bring together the best features of CPLD and FPGA devices on a single chip.

**Table 1-1. MachXO Family Selection Guide**

| Device                              | LCMXO256         | LCMXO640         | LCMXO1200        | LCMXO2280        |
|-------------------------------------|------------------|------------------|------------------|------------------|
| LUTs                                | 256              | 640              | 1200             | 2280             |
| Dist. RAM (Kbits)                   | 2.0              | 6.1              | 6.4              | 7.7              |
| EBR SRAM (Kbits)                    | 0                | 0                | 9.2              | 27.6             |
| Number of EBR SRAM Blocks (9 Kbits) | 0                | 0                | 1                | 3                |
| V <sub>CC</sub> Voltage             | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V |
| Number of PLLs                      | 0                | 0                | 1                | 2                |
| Max. I/O                            | 78               | 159              | 211              | 271              |
| <b>Packages</b>                     |                  |                  |                  |                  |
| 100-pin TQFP (14x14 mm)             | 78               | 74               | 73               | 73               |
| 144-pin TQFP (20x20 mm)             |                  | 113              | 113              | 113              |
| 100-ball csBGA (8x8 mm)             | 78               | 74               |                  |                  |
| 132-ball csBGA (8x8 mm)             |                  | 101              | 101              | 101              |
| 256-ball caBGA (14x14 mm)           |                  | 159              | 211              | 211              |
| 256-ball ftBGA (17x17 mm)           |                  | 159              | 211              | 211              |
| 324-ball ftBGA (19x19 mm)           |                  |                  |                  | 271              |

There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2-1 lists the signals associated with each Slice.

**Figure 2-5. Slice Diagram**



**Notes:**

Some inter-Slice signals are not shown.

\* Only PFUs at the edges have fast connections to the I/O cell.

**Table 2-1. Slice Signal Descriptions**

| Function | Type             | Signal Names   | Description                                                          |
|----------|------------------|----------------|----------------------------------------------------------------------|
| Input    | Data signal      | A0, B0, C0, D0 | Inputs to LUT4                                                       |
| Input    | Data signal      | A1, B1, C1, D1 | Inputs to LUT4                                                       |
| Input    | Multi-purpose    | M0/M1          | Multipurpose Input                                                   |
| Input    | Control signal   | CE             | Clock Enable                                                         |
| Input    | Control signal   | LSR            | Local Set/Reset                                                      |
| Input    | Control signal   | CLK            | System Clock                                                         |
| Input    | Inter-PFU signal | FCIN           | Fast Carry In <sup>1</sup>                                           |
| Output   | Data signals     | F0, F1         | LUT4 output register bypass signals                                  |
| Output   | Data signals     | Q0, Q1         | Register Outputs                                                     |
| Output   | Data signals     | OFX0           | Output of a LUT5 MUX                                                 |
| Output   | Data signals     | OFX1           | Output of a LUT6, LUT7, LUT8 <sup>2</sup> MUX depending on the Slice |
| Output   | Inter-PFU signal | FCO            | Fast Carry Out <sup>1</sup>                                          |

1. See Figure 2-4 for connection details.

2. Requires two PFUs.

### Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

**Table 2-2. Slice Modes**

|           | Logic              | Ripple                | RAM     | ROM          |
|-----------|--------------------|-----------------------|---------|--------------|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SP 16x2 | ROM 16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A     | ROM 16x1 x 2 |

**Logic Mode:** In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

**Table 2-3. Number of Slices Required For Implementing Distributed RAM**

|                  | SPR16x2 | DPR16x2 |
|------------------|---------|---------|
| Number of Slices | 1       | 2       |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

## sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL\_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the  $t_{LOCK}$  parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

**Figure 2-10. PLL Diagram**

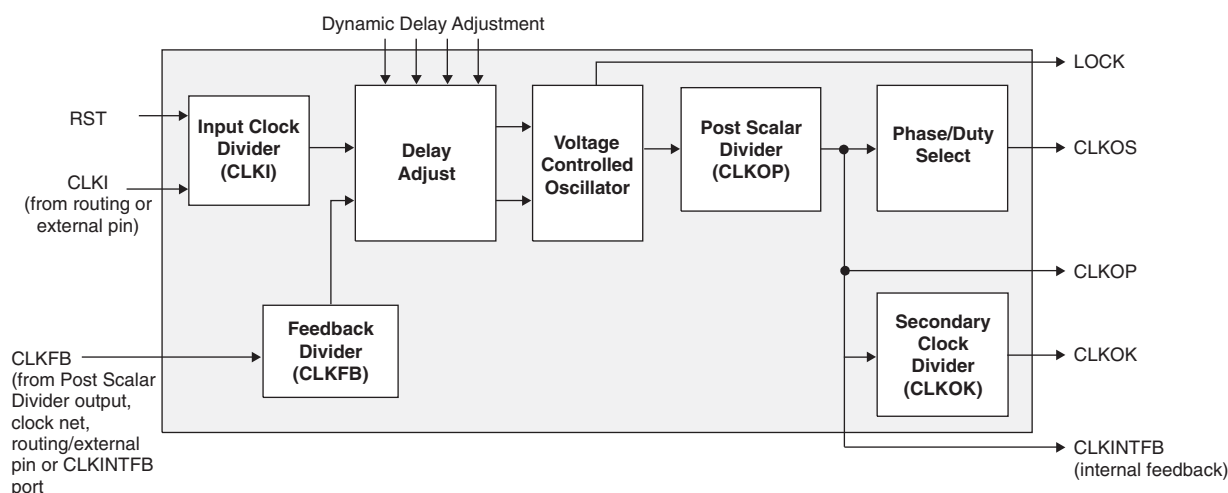
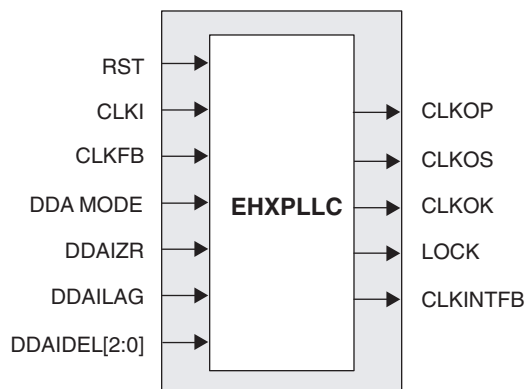


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

**Figure 2-11. PLL Primitive**



The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

### FIFO Configuration

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2-7.

**Table 2-7. Programmable FIFO Flag Ranges**

| Flag Name         | Programming Range     |
|-------------------|-----------------------|
| Full (FF)         | 1 to (up to $2^N-1$ ) |
| Almost Full (AF)  | 1 to Full-1           |
| Almost Empty (AE) | 1 to Full-1           |
| Empty (EF)        | 0                     |

N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

**Table 2-10. Supported Output Standards**

| Output Standard                | Drive                | V <sub>CCIO</sub> (Typ.) |
|--------------------------------|----------------------|--------------------------|
| <b>Single-ended Interfaces</b> |                      |                          |
| LVTTTL                         | 4mA, 8mA, 12mA, 16mA | 3.3                      |
| LVC MOS33                      | 4mA, 8mA, 12mA, 14mA | 3.3                      |
| LVC MOS25                      | 4mA, 8mA, 12mA, 14mA | 2.5                      |
| LVC MOS18                      | 4mA, 8mA, 12mA, 14mA | 1.8                      |
| LVC MOS15                      | 4mA, 8mA             | 1.5                      |
| LVC MOS12                      | 2mA, 6mA             | 1.2                      |
| LVC MOS33, Open Drain          | 4mA, 8mA, 12mA, 14mA | —                        |
| LVC MOS25, Open Drain          | 4mA, 8mA, 12mA, 14mA | —                        |
| LVC MOS18, Open Drain          | 4mA, 8mA, 12mA, 14mA | —                        |
| LVC MOS15, Open Drain          | 4mA, 8mA             | —                        |
| LVC MOS12, Open Drain          | 2mA, 6mA             | —                        |
| PCI33 <sup>3</sup>             | N/A                  | 3.3                      |
| <b>Differential Interfaces</b> |                      |                          |
| LVDS <sup>1, 2</sup>           | N/A                  | 2.5                      |
| BLVDS, RSDS <sup>2</sup>       | N/A                  | 2.5                      |
| LVPECL <sup>2</sup>            | N/A                  | 3.3                      |

1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

3. Top Banks of MachXO1200 and MachXO2280 devices only.

## sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the MachXO1200 and MachXO2280 (two Banks per side). The MachXO640 has four Banks (one Bank per side). The smallest member of this family, the MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V<sub>CCIO</sub>) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

Figure 2-18. MachXO2280 Banks

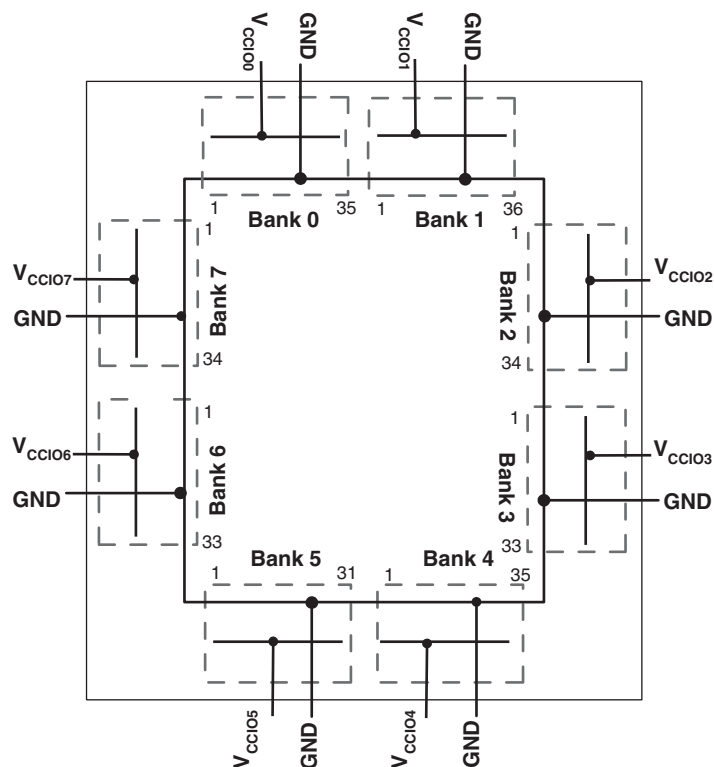


Figure 2-19. MachXO1200 Banks

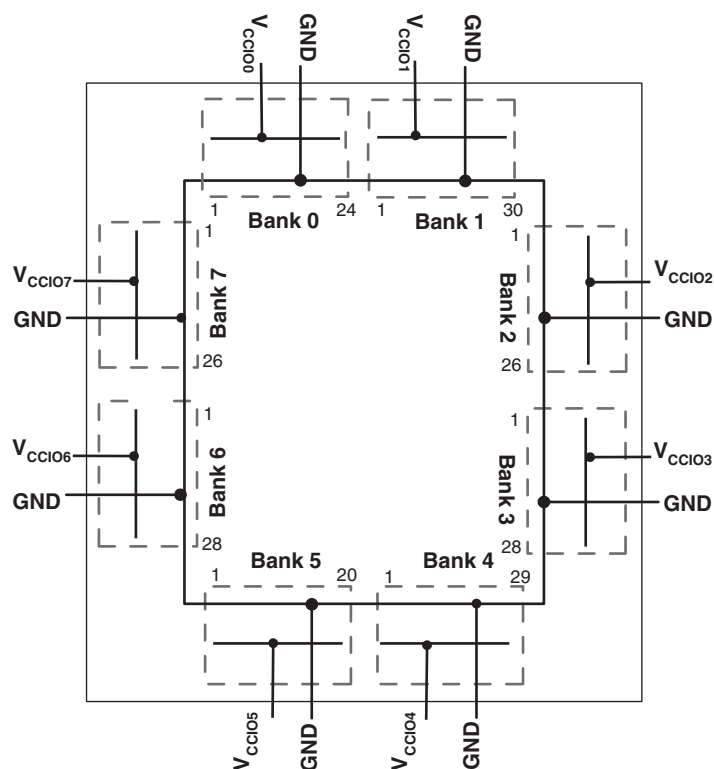




Figure 2-20. MachXO640 Banks

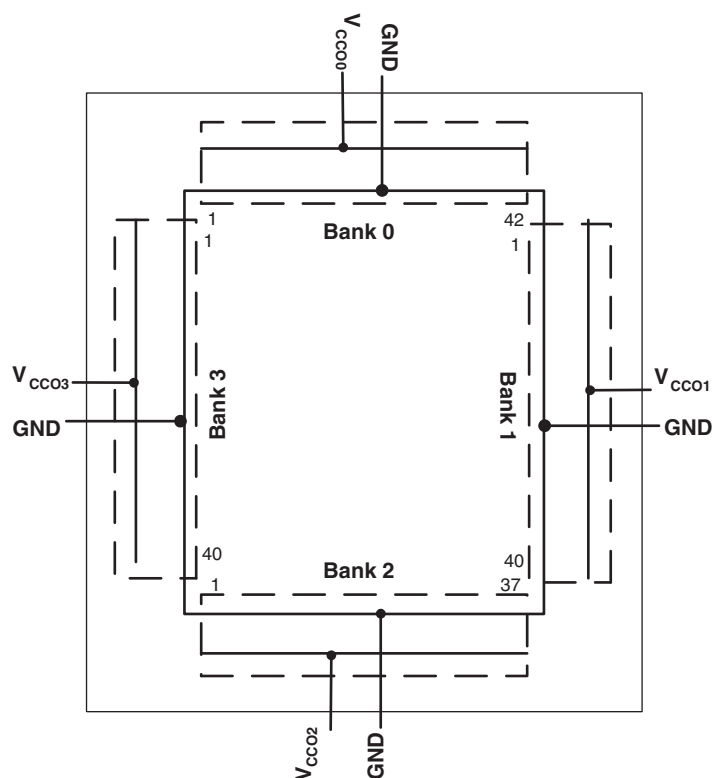
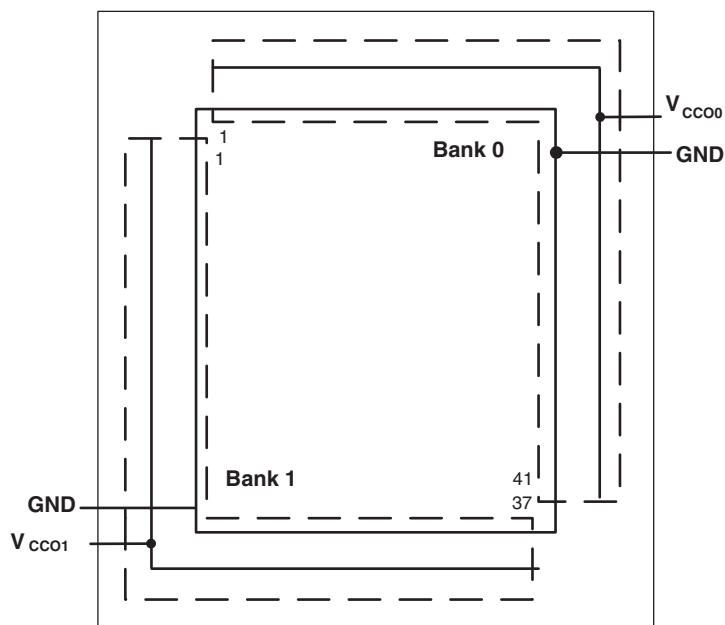


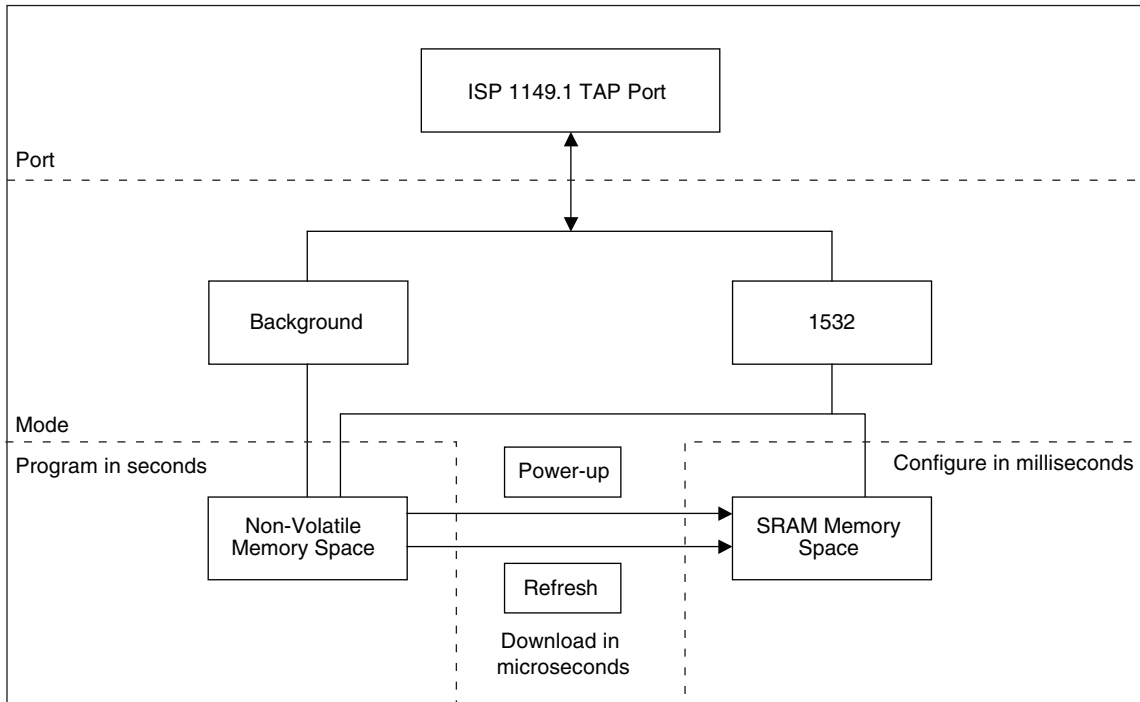
Figure 2-21. MachXO256 Banks



## Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of

**Figure 2-22. MachXO Configuration and Programming**



## Density Shifting

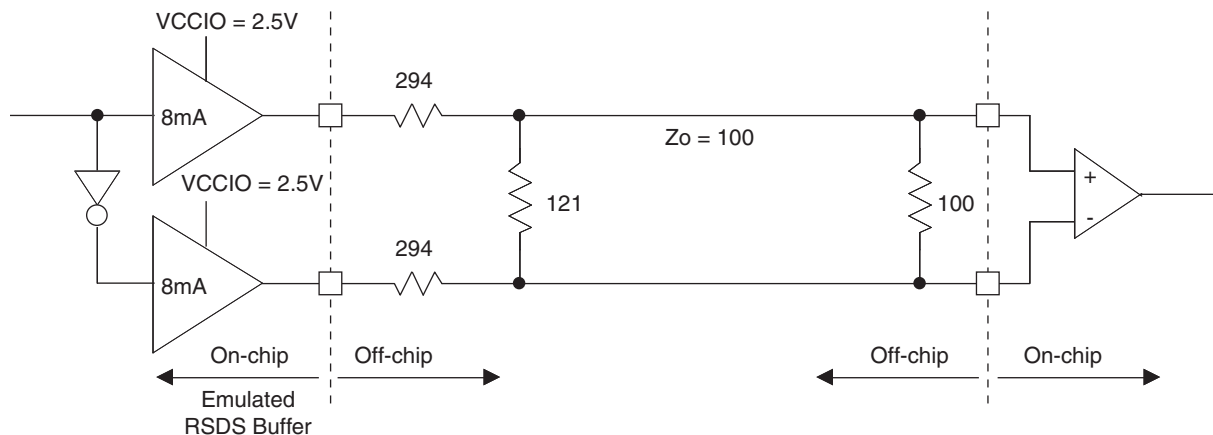
The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

### RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

**Figure 3-4. RSDS (Reduced Swing Differential Standard)**



**Table 3-4. RSDS DC Conditions**

| Parameter  | Description                 | Typical | Units |
|------------|-----------------------------|---------|-------|
| $Z_{OUT}$  | Output impedance            | 20      | Ohms  |
| $R_S$      | Driver series resistor      | 294     | Ohms  |
| $R_P$      | Driver parallel resistor    | 121     | Ohms  |
| $R_T$      | Receiver termination        | 100     | Ohms  |
| $V_{OH}$   | Output high voltage         | 1.35    | V     |
| $V_{OL}$   | Output low voltage          | 1.15    | V     |
| $V_{OD}$   | Output differential voltage | 0.20    | V     |
| $V_{CM}$   | Output common mode voltage  | 1.25    | V     |
| $Z_{BACK}$ | Back impedance              | 101.5   | Ohms  |
| $I_{DC}$   | DC output current           | 3.66    | mA    |

## MachXO Family Timing Adders<sup>1, 2, 3</sup>

Over Recommended Operating Conditions

| Buffer Type             | Description            | -5    | -4    | -3    | Units |
|-------------------------|------------------------|-------|-------|-------|-------|
| <b>Input Adjusters</b>  |                        |       |       |       |       |
| LVDS25 <sup>4</sup>     | LVDS                   | 0.44  | 0.53  | 0.61  | ns    |
| BLVDS25 <sup>4</sup>    | BLVDS                  | 0.44  | 0.53  | 0.61  | ns    |
| LVPECL33 <sup>4</sup>   | LVPECL                 | 0.42  | 0.50  | 0.59  | ns    |
| LVTTTL33                | LVTTTL                 | 0.01  | 0.01  | 0.01  | ns    |
| LVC MOS33               | LVC MOS 3.3            | 0.01  | 0.01  | 0.01  | ns    |
| LVC MOS25               | LVC MOS 2.5            | 0.00  | 0.00  | 0.00  | ns    |
| LVC MOS18               | LVC MOS 1.8            | 0.07  | 0.08  | 0.10  | ns    |
| LVC MOS15               | LVC MOS 1.5            | 0.14  | 0.17  | 0.19  | ns    |
| LVC MOS12               | LVC MOS 1.2            | 0.40  | 0.48  | 0.56  | ns    |
| PCI33 <sup>4</sup>      | PCI                    | 0.01  | 0.01  | 0.01  | ns    |
| <b>Output Adjusters</b> |                        |       |       |       |       |
| LVDS25E                 | LVDS 2.5 E             | -0.13 | -0.15 | -0.18 | ns    |
| LVDS25 <sup>4</sup>     | LVDS 2.5               | -0.21 | -0.26 | -0.30 | ns    |
| BLVDS25                 | BLVDS 2.5              | -0.03 | -0.03 | -0.04 | ns    |
| LVPECL33                | LVPECL 3.3             | 0.04  | 0.04  | 0.05  | ns    |
| LVTTTL33_4mA            | LVTTTL 4mA drive       | 0.04  | 0.04  | 0.05  | ns    |
| LVTTTL33_8mA            | LVTTTL 8mA drive       | 0.06  | 0.07  | 0.08  | ns    |
| LVTTTL33_12mA           | LVTTTL 12mA drive      | -0.01 | -0.01 | -0.01 | ns    |
| LVTTTL33_16mA           | LVTTTL 16mA drive      | 0.50  | 0.60  | 0.70  | ns    |
| LVC MOS33_4mA           | LVC MOS 3.3 4mA drive  | 0.04  | 0.04  | 0.05  | ns    |
| LVC MOS33_8mA           | LVC MOS 3.3 8mA drive  | 0.06  | 0.07  | 0.08  | ns    |
| LVC MOS33_12mA          | LVC MOS 3.3 12mA drive | -0.01 | -0.01 | -0.01 | ns    |
| LVC MOS33_14mA          | LVC MOS 3.3 14mA drive | 0.50  | 0.60  | 0.70  | ns    |
| LVC MOS25_4mA           | LVC MOS 2.5 4mA drive  | 0.05  | 0.06  | 0.07  | ns    |
| LVC MOS25_8mA           | LVC MOS 2.5 8mA drive  | 0.10  | 0.12  | 0.13  | ns    |
| LVC MOS25_12mA          | LVC MOS 2.5 12mA drive | 0.00  | 0.00  | 0.00  | ns    |
| LVC MOS25_14mA          | LVC MOS 2.5 14mA drive | 0.34  | 0.40  | 0.47  | ns    |
| LVC MOS18_4mA           | LVC MOS 1.8 4mA drive  | 0.11  | 0.13  | 0.15  | ns    |
| LVC MOS18_8mA           | LVC MOS 1.8 8mA drive  | 0.05  | 0.06  | 0.06  | ns    |
| LVC MOS18_12mA          | LVC MOS 1.8 12mA drive | -0.06 | -0.07 | -0.08 | ns    |
| LVC MOS18_14mA          | LVC MOS 1.8 14mA drive | 0.06  | 0.07  | 0.09  | ns    |
| LVC MOS15_4mA           | LVC MOS 1.5 4mA drive  | 0.15  | 0.19  | 0.22  | ns    |
| LVC MOS15_8mA           | LVC MOS 1.5 8mA drive  | 0.05  | 0.06  | 0.07  | ns    |
| LVC MOS12_2mA           | LVC MOS 1.2 2mA drive  | 0.26  | 0.31  | 0.36  | ns    |
| LVC MOS12_6mA           | LVC MOS 1.2 6mA drive  | 0.05  | 0.06  | 0.07  | ns    |
| PCI33 <sup>4</sup>      | PCI33                  | 1.85  | 2.22  | 2.59  | ns    |

1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing is measured with the load specified in Switching Test Conditions table.

3. All other standards tested according to the appropriate specifications.

4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

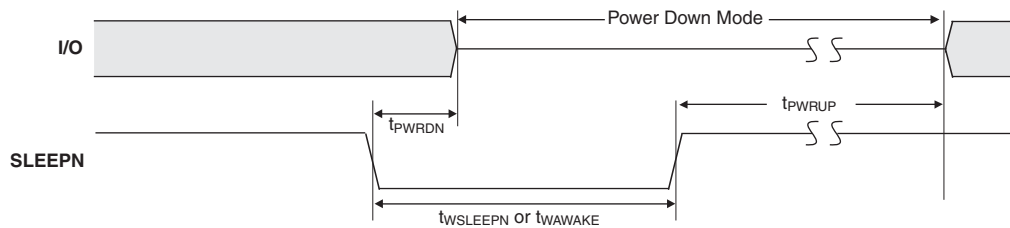
Rev. A 0.19

### MachXO “C” Sleep Mode Timing

| Symbol        | Parameter                | Device    | Min. | Typ. | Max  | Units |
|---------------|--------------------------|-----------|------|------|------|-------|
| $t_{PWRDN}$   | SLEEPN Low to Power Down | All       | —    | —    | 400  | ns    |
| $t_{PWRUP}$   | SLEEPN High to Power Up  | LCMXO256  | —    | —    | 400  | μs    |
|               |                          | LCMXO640  | —    | —    | 600  | μs    |
|               |                          | LCMXO1200 | —    | —    | 800  | μs    |
|               |                          | LCMXO2280 | —    | —    | 1000 | μs    |
| $t_{WSLEEPN}$ | SLEEPN Pulse Width       | All       | 400  | —    | —    | ns    |
| $t_{WAWAKE}$  | SLEEPN Pulse Rejection   | All       | —    | —    | 100  | ns    |

Rev. A 0.19

### Flash Download Time



| Symbol        | Parameter                                                                        | Min.      | Typ. | Max. | Units |
|---------------|----------------------------------------------------------------------------------|-----------|------|------|-------|
| $t_{REFRESH}$ | Minimum $V_{CC}$ or $V_{CCAUX}$ (later of the two supplies) to Device I/O Active | LCMXO256  | —    | 0.4  | ms    |
|               |                                                                                  | LCMXO640  | —    | 0.6  | ms    |
|               |                                                                                  | LCMXO1200 | —    | 0.8  | ms    |
|               |                                                                                  | LCMXO2280 | —    | 1.0  | ms    |

### JTAG Port Timing Specifications

| Symbol        | Parameter                                                            | Min. | Max. | Units |
|---------------|----------------------------------------------------------------------|------|------|-------|
| $f_{MAX}$     | TCK [BSCAN] clock frequency                                          | —    | 25   | MHz   |
| $t_{BTCP}$    | TCK [BSCAN] clock pulse width                                        | 40   | —    | ns    |
| $t_{BTCPH}$   | TCK [BSCAN] clock pulse width high                                   | 20   | —    | ns    |
| $t_{BTCPL}$   | TCK [BSCAN] clock pulse width low                                    | 20   | —    | ns    |
| $t_{BTS}$     | TCK [BSCAN] setup time                                               | 8    | —    | ns    |
| $t_{BTH}$     | TCK [BSCAN] hold time                                                | 10   | —    | ns    |
| $t_{BTRF}$    | TCK [BSCAN] rise/fall time                                           | 50   | —    | mV/ns |
| $t_{BTCO}$    | TAP controller falling edge of clock to output valid                 | —    | 10   | ns    |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to output disabled              | —    | 10   | ns    |
| $t_{BTCOEN}$  | TAP controller falling edge of clock to output enabled               | —    | 10   | ns    |
| $t_{BTCRS}$   | BSCAN test capture register setup time                               | 8    | —    | ns    |
| $t_{BTCRH}$   | BSCAN test capture register hold time                                | 25   | —    | ns    |
| $t_{BUTCO}$   | BSCAN test update register, falling edge of clock to output valid    | —    | 25   | ns    |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to output disabled | —    | 25   | ns    |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to output enabled  | —    | 25   | ns    |

Rev. A 0.19

**LCMX01200 and LCMX02280 Logic Signal Connections: 100 TQFP**

| Pin Number | LCMX01200        |      |                |              | LCMX02280        |      |                |              |
|------------|------------------|------|----------------|--------------|------------------|------|----------------|--------------|
|            | Ball Function    | Bank | Dual Function  | Differential | Ball Function    | Bank | Dual Function  | Differential |
| 1          | PL2A             | 7    |                | T            | PL2A             | 7    | LUM0_PLLT_FB_A | T            |
| 2          | PL2B             | 7    |                | C            | PL2B             | 7    | LUM0_PLLC_FB_A | C            |
| 3          | PL3C             | 7    |                | T            | PL3C             | 7    | LUM0_PLLT_IN_A | T            |
| 4          | PL3D             | 7    |                | C            | PL3D             | 7    | LUM0_PLLC_IN_A | C            |
| 5          | PL4B             | 7    |                |              | PL4B             | 7    |                |              |
| 6          | VCCIO7           | 7    |                |              | VCCIO7           | 7    |                |              |
| 7          | PL6A             | 7    |                | T*           | PL7A             | 7    |                | T*           |
| 8          | PL6B             | 7    | GSRN           | C*           | PL7B             | 7    | GSRN           | C*           |
| 9          | GND              | -    |                |              | GND              | -    |                |              |
| 10         | PL7C             | 7    |                | T            | PL9C             | 7    |                | T            |
| 11         | PL7D             | 7    |                | C            | PL9D             | 7    |                | C            |
| 12         | PL8C             | 7    |                | T            | PL10C            | 7    |                | T            |
| 13         | PL8D             | 7    |                | C            | PL10D            | 7    |                | C            |
| 14         | PL9C             | 6    |                |              | PL11C            | 6    |                |              |
| 15         | PL10A            | 6    |                | T*           | PL13A            | 6    |                | T*           |
| 16         | PL10B            | 6    |                | C*           | PL13B            | 6    |                | C*           |
| 17         | VCC              | -    |                |              | VCC              | -    |                |              |
| 18         | PL11B            | 6    |                |              | PL14D            | 6    |                | C            |
| 19         | PL11C            | 6    | TSALL          |              | PL14C            | 6    | TSALL          | T            |
| 20         | VCCIO6           | 6    |                |              | VCCIO6           | 6    |                |              |
| 21         | PL13C            | 6    |                |              | PL16C            | 6    |                |              |
| 22         | PL14A            | 6    | LLM0_PLLT_FB_A | T*           | PL17A            | 6    | LLM0_PLLT_FB_A | T*           |
| 23         | PL14B            | 6    | LLM0_PLLC_FB_A | C*           | PL17B            | 6    | LLM0_PLLC_FB_A | C*           |
| 24         | PL15A            | 6    | LLM0_PLLT_IN_A | T*           | PL18A            | 6    | LLM0_PLLT_IN_A | T*           |
| 25         | PL15B            | 6    | LLM0_PLLC_IN_A | C*           | PL18B            | 6    | LLM0_PLLC_IN_A | C*           |
| 26**       | GNDIO6<br>GNDIO5 | -    |                |              | GNDIO6<br>GNDIO5 | -    |                |              |
| 27         | VCCIO5           | 5    |                |              | VCCIO5           | 5    |                |              |
| 28         | TMS              | 5    | TMS            |              | TMS              | 5    | TMS            |              |
| 29         | TCK              | 5    | TCK            |              | TCK              | 5    | TCK            |              |
| 30         | PB3B             | 5    |                |              | PB3B             | 5    |                |              |
| 31         | PB4A             | 5    |                | T            | PB4A             | 5    |                | T            |
| 32         | PB4B             | 5    |                | C            | PB4B             | 5    |                | C            |
| 33         | TDO              | 5    | TDO            |              | TDO              | 5    | TDO            |              |
| 34         | TDI              | 5    | TDI            |              | TDI              | 5    | TDI            |              |
| 35         | VCC              | -    |                |              | VCC              | -    |                |              |
| 36         | VCCAUX           | -    |                |              | VCCAUX           | -    |                |              |
| 37         | PB6E             | 5    |                | T            | PB8E             | 5    |                | T            |
| 38         | PB6F             | 5    |                | C            | PB8F             | 5    |                | C            |
| 39         | PB7B             | 4    | PCLK4_1****    |              | PB10F            | 4    | PCLK4_1****    |              |
| 40         | PB7F             | 4    | PCLK4_0****    |              | PB10B            | 4    | PCLK4_0****    |              |
| 41         | GND              | -    |                |              | GND              | -    |                |              |

**LCMX0256 and LCMX0640 Logic Signal Connections: 100 csBGA (Cont.)**

| LCMX0256    |               |      |               |              | LCMX0640    |               |      |               |              |
|-------------|---------------|------|---------------|--------------|-------------|---------------|------|---------------|--------------|
| Ball Number | Ball Function | Bank | Dual Function | Differential | Ball Number | Ball Function | Bank | Dual Function | Differential |
| A4          | GNDIO0        | 0    |               |              | A4          | GNDIO0        | 0    |               |              |
| B4          | PT3A          | 0    |               | T            | B4          | PT3B          | 0    |               | C            |
| A3          | PT2F          | 0    |               | C            | A3          | PT3A          | 0    |               | T            |
| B3          | PT2E          | 0    |               | T            | B3          | PT2F          | 0    |               | C            |
| A2          | PT2D          | 0    |               | C            | A2          | PT2E          | 0    |               | T            |
| C3          | PT2C          | 0    |               | T            | C3          | PT2B          | 0    |               | C            |
| A1          | PT2B          | 0    |               | C            | A1          | PT2C          | 0    |               |              |
| B2          | PT2A          | 0    |               | T            | B2          | PT2A          | 0    |               | T            |
| N9          | GND           | -    |               |              | N9          | GND           | -    |               |              |
| B9          | GND           | -    |               |              | B9          | GND           | -    |               |              |
| B5          | VCCIO0        | 0    |               |              | B5          | VCCIO0        | 0    |               |              |
| A14         | VCCIO0        | 0    |               |              | A14         | VCCIO1        | 1    |               |              |
| H14         | VCCIO0        | 0    |               |              | H14         | VCCIO1        | 1    |               |              |
| P10         | VCCIO1        | 1    |               |              | P10         | VCCIO2        | 2    |               |              |
| G1          | VCCIO1        | 1    |               |              | G1          | VCCIO3        | 3    |               |              |
| P1          | VCCIO1        | 1    |               |              | P1          | VCCIO3        | 3    |               |              |

\*NC for "E" devices.

\*\*Primary clock inputs are single-ended.

**LCMX02280 Logic Signal Connections: 324 ftBGA (Cont.)**

| LCMX02280   |               |      |                |              |
|-------------|---------------|------|----------------|--------------|
| Ball Number | Ball Function | Bank | Dual Function  | Differential |
| G2          | PL11A         | 6    |                | T*           |
| H2          | PL11B         | 6    |                | C*           |
| L3          | PL11C         | 6    |                | T            |
| L5          | PL11D         | 6    |                | C            |
| H1          | PL12A         | 6    |                | T*           |
| VCCIO6      | VCCIO6        | 6    |                |              |
| GND         | GNDIO6        | 6    |                |              |
| J2          | PL12B         | 6    |                | C*           |
| L4          | PL12C         | 6    |                | T            |
| L6          | PL12D         | 6    |                | C            |
| K2          | PL13A         | 6    |                | T*           |
| K1          | PL13B         | 6    |                | C*           |
| J1          | PL13C         | 6    |                | T            |
| VCC         | VCC           | -    |                |              |
| L2          | PL13D         | 6    |                | C            |
| M5          | PL14D         | 6    |                | C            |
| M3          | PL14C         | 6    | TSALL          | T            |
| L1          | PL14B         | 6    |                | C*           |
| M2          | PL14A         | 6    |                | T*           |
| M1          | PL15A         | 6    |                | T*           |
| N1          | PL15B         | 6    |                | C*           |
| M6          | PL15C         | 6    |                | T            |
| M4          | PL15D         | 6    |                | C            |
| VCCIO6      | VCCIO6        | 6    |                |              |
| GND         | GNDIO6        | 6    |                |              |
| P1          | PL16A         | 6    |                | T*           |
| P2          | PL16B         | 6    |                | C*           |
| N3          | PL16C         | 6    |                | T            |
| N4          | PL16D         | 6    |                | C            |
| GND         | GND           | -    |                |              |
| T1          | PL17A         | 6    | LLM0_PLLT_FB_A | T*           |
| R1          | PL17B         | 6    | LLM0_PLLC_FB_A | C*           |
| P3          | PL17C         | 6    |                | T            |
| N5          | PL17D         | 6    |                | C            |
| R3          | PL18A         | 6    | LLM0_PLLT_IN_A | T*           |
| R2          | PL18B         | 6    | LLM0_PLLC_IN_A | C*           |
| P4          | PL19A         | 6    |                | T            |
| N6          | PL19B         | 6    |                | C            |
| U1          | PL20A         | 6    |                | T            |
| VCCIO6      | VCCIO6        | 6    |                |              |
| GND         | GNDIO6        | 6    |                |              |
| GND         | GNDIO5        | 5    |                |              |
| VCCIO5      | VCCIO5        | 5    |                |              |



**LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)**

| LCMXO2280   |               |      |               |              |
|-------------|---------------|------|---------------|--------------|
| Ball Number | Ball Function | Bank | Dual Function | Differential |
| T2          | PL20B         | 6    |               | C            |
| P6          | TMS           | 5    | TMS           |              |
| V1          | PB2A          | 5    |               | T            |
| U2          | PB2B          | 5    |               | C            |
| T3          | PB2C          | 5    |               | T            |
| N7          | TCK           | 5    | TCK           |              |
| R4          | PB2D          | 5    |               | C            |
| R5          | PB3A          | 5    |               | T            |
| T4          | PB3B          | 5    |               | C            |
| VCC         | VCC           | -    |               |              |
| R6          | PB3C          | 5    |               | T            |
| P7          | PB3D          | 5    |               | C            |
| U3          | PB4A          | 5    |               | T            |
| T5          | PB4B          | 5    |               | C            |
| V2          | PB4C          | 5    |               | T            |
| N8          | TDO           | 5    | TDO           |              |
| V3          | PB4D          | 5    |               | C            |
| T6          | PB5A          | 5    |               | T            |
| GND         | GNDIO5        | 5    |               |              |
| VCCIO5      | VCCIO5        | 5    |               |              |
| U4          | PB5B          | 5    |               | C            |
| P8          | PB5C          | 5    |               | T            |
| T7          | PB5D          | 5    |               | C            |
| V4          | TDI           | 5    | TDI           |              |
| R8          | PB6A          | 5    |               | T            |
| N9          | PB6B          | 5    |               | C            |
| U5          | PB6C          | 5    |               | T            |
| V5          | PB6D          | 5    |               | C            |
| U6          | PB7A          | 5    |               | T            |
| VCC         | VCC           | -    |               |              |
| V6          | PB7B          | 5    |               | C            |
| P9          | PB7C          | 5    |               | T            |
| T8          | PB7D          | 5    |               | C            |
| U7          | PB8A          | 5    |               | T            |
| V7          | PB8B          | 5    |               | C            |
| M10         | VCCAUX        | -    |               |              |
| U8          | PB8C          | 5    |               | T            |
| V8          | PB8D          | 5    |               | C            |
| VCCIO5      | VCCIO5        | 5    |               |              |
| GND         | GNDIO5        | 5    |               |              |
| T9          | PB8E          | 5    |               | T            |
| U9          | PB8F          | 5    |               | C            |
| V9          | PB9A          | 4    |               | T            |

**LCMX02280 Logic Signal Connections: 324 ftBGA (Cont.)**

| LCMX02280   |               |      |               |              |
|-------------|---------------|------|---------------|--------------|
| Ball Number | Ball Function | Bank | Dual Function | Differential |
| F16         | GND           | -    |               |              |
| H10         | GND           | -    |               |              |
| H11         | GND           | -    |               |              |
| H8          | GND           | -    |               |              |
| H9          | GND           | -    |               |              |
| J10         | GND           | -    |               |              |
| J11         | GND           | -    |               |              |
| J4          | GND           | -    |               |              |
| J8          | GND           | -    |               |              |
| J9          | GND           | -    |               |              |
| K10         | GND           | -    |               |              |
| K11         | GND           | -    |               |              |
| K17         | GND           | -    |               |              |
| K8          | GND           | -    |               |              |
| K9          | GND           | -    |               |              |
| L10         | GND           | -    |               |              |
| L11         | GND           | -    |               |              |
| L8          | GND           | -    |               |              |
| L9          | GND           | -    |               |              |
| N2          | GND           | -    |               |              |
| P14         | GND           | -    |               |              |
| P5          | GND           | -    |               |              |
| R7          | GND           | -    |               |              |
| F14         | VCC           | -    |               |              |
| G11         | VCC           | -    |               |              |
| G9          | VCC           | -    |               |              |
| H7          | VCC           | -    |               |              |
| L7          | VCC           | -    |               |              |
| M9          | VCC           | -    |               |              |
| H6          | VCCIO7        | 7    |               |              |
| J7          | VCCIO7        | 7    |               |              |
| M7          | VCCIO6        | 6    |               |              |
| K7          | VCCIO6        | 6    |               |              |
| M8          | VCCIO5        | 5    |               |              |
| R9          | VCCIO5        | 5    |               |              |
| M12         | VCCIO4        | 4    |               |              |
| M11         | VCCIO4        | 4    |               |              |
| L12         | VCCIO3        | 3    |               |              |
| K12         | VCCIO3        | 3    |               |              |
| J12         | VCCIO2        | 2    |               |              |
| H12         | VCCIO2        | 2    |               |              |
| G12         | VCCIO1        | 1    |               |              |
| G10         | VCCIO1        | 1    |               |              |

**Conventional Packaging**
**Commercial**

| Part Number      | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|------------------|------|----------------|------|-------|---------|------|-------|
| LCMXO256C-3T100C | 256  | 1.8V/2.5V/3.3V | 78   | -3    | TQFP    | 100  | COM   |
| LCMXO256C-4T100C | 256  | 1.8V/2.5V/3.3V | 78   | -4    | TQFP    | 100  | COM   |
| LCMXO256C-5T100C | 256  | 1.8V/2.5V/3.3V | 78   | -5    | TQFP    | 100  | COM   |
| LCMXO256C-3M100C | 256  | 1.8V/2.5V/3.3V | 78   | -3    | csBGA   | 100  | COM   |
| LCMXO256C-4M100C | 256  | 1.8V/2.5V/3.3V | 78   | -4    | csBGA   | 100  | COM   |
| LCMXO256C-5M100C | 256  | 1.8V/2.5V/3.3V | 78   | -5    | csBGA   | 100  | COM   |

| Part Number       | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|-------------------|------|----------------|------|-------|---------|------|-------|
| LCMXO640C-3T100C  | 640  | 1.8V/2.5V/3.3V | 74   | -3    | TQFP    | 100  | COM   |
| LCMXO640C-4T100C  | 640  | 1.8V/2.5V/3.3V | 74   | -4    | TQFP    | 100  | COM   |
| LCMXO640C-5T100C  | 640  | 1.8V/2.5V/3.3V | 74   | -5    | TQFP    | 100  | COM   |
| LCMXO640C-3M100C  | 640  | 1.8V/2.5V/3.3V | 74   | -3    | csBGA   | 100  | COM   |
| LCMXO640C-4M100C  | 640  | 1.8V/2.5V/3.3V | 74   | -4    | csBGA   | 100  | COM   |
| LCMXO640C-5M100C  | 640  | 1.8V/2.5V/3.3V | 74   | -5    | csBGA   | 100  | COM   |
| LCMXO640C-3T144C  | 640  | 1.8V/2.5V/3.3V | 113  | -3    | TQFP    | 144  | COM   |
| LCMXO640C-4T144C  | 640  | 1.8V/2.5V/3.3V | 113  | -4    | TQFP    | 144  | COM   |
| LCMXO640C-5T144C  | 640  | 1.8V/2.5V/3.3V | 113  | -5    | TQFP    | 144  | COM   |
| LCMXO640C-3M132C  | 640  | 1.8V/2.5V/3.3V | 101  | -3    | csBGA   | 132  | COM   |
| LCMXO640C-4M132C  | 640  | 1.8V/2.5V/3.3V | 101  | -4    | csBGA   | 132  | COM   |
| LCMXO640C-5M132C  | 640  | 1.8V/2.5V/3.3V | 101  | -5    | csBGA   | 132  | COM   |
| LCMXO640C-3B256C  | 640  | 1.8V/2.5V/3.3V | 159  | -3    | caBGA   | 256  | COM   |
| LCMXO640C-4B256C  | 640  | 1.8V/2.5V/3.3V | 159  | -4    | caBGA   | 256  | COM   |
| LCMXO640C-5B256C  | 640  | 1.8V/2.5V/3.3V | 159  | -5    | caBGA   | 256  | COM   |
| LCMXO640C-3FT256C | 640  | 1.8V/2.5V/3.3V | 159  | -3    | ftBGA   | 256  | COM   |
| LCMXO640C-4FT256C | 640  | 1.8V/2.5V/3.3V | 159  | -4    | ftBGA   | 256  | COM   |
| LCMXO640C-5FT256C | 640  | 1.8V/2.5V/3.3V | 159  | -5    | ftBGA   | 256  | COM   |

| Part Number        | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|--------------------|------|----------------|------|-------|---------|------|-------|
| LCMXO1200C-3T100C  | 1200 | 1.8V/2.5V/3.3V | 73   | -3    | TQFP    | 100  | COM   |
| LCMXO1200C-4T100C  | 1200 | 1.8V/2.5V/3.3V | 73   | -4    | TQFP    | 100  | COM   |
| LCMXO1200C-5T100C  | 1200 | 1.8V/2.5V/3.3V | 73   | -5    | TQFP    | 100  | COM   |
| LCMXO1200C-3T144C  | 1200 | 1.8V/2.5V/3.3V | 113  | -3    | TQFP    | 144  | COM   |
| LCMXO1200C-4T144C  | 1200 | 1.8V/2.5V/3.3V | 113  | -4    | TQFP    | 144  | COM   |
| LCMXO1200C-5T144C  | 1200 | 1.8V/2.5V/3.3V | 113  | -5    | TQFP    | 144  | COM   |
| LCMXO1200C-3M132C  | 1200 | 1.8V/2.5V/3.3V | 101  | -3    | csBGA   | 132  | COM   |
| LCMXO1200C-4M132C  | 1200 | 1.8V/2.5V/3.3V | 101  | -4    | csBGA   | 132  | COM   |
| LCMXO1200C-5M132C  | 1200 | 1.8V/2.5V/3.3V | 101  | -5    | csBGA   | 132  | COM   |
| LCMXO1200C-3B256C  | 1200 | 1.8V/2.5V/3.3V | 211  | -3    | caBGA   | 256  | COM   |
| LCMXO1200C-4B256C  | 1200 | 1.8V/2.5V/3.3V | 211  | -4    | caBGA   | 256  | COM   |
| LCMXO1200C-5B256C  | 1200 | 1.8V/2.5V/3.3V | 211  | -5    | caBGA   | 256  | COM   |
| LCMXO1200C-3FT256C | 1200 | 1.8V/2.5V/3.3V | 211  | -3    | ftBGA   | 256  | COM   |
| LCMXO1200C-4FT256C | 1200 | 1.8V/2.5V/3.3V | 211  | -4    | ftBGA   | 256  | COM   |
| LCMXO1200C-5FT256C | 1200 | 1.8V/2.5V/3.3V | 211  | -5    | ftBGA   | 256  | COM   |

| Part Number         | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|---------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO2280C-3TN100C  | 2280 | 1.8V/2.5V/3.3V | 73   | -3    | Lead-Free TQFP  | 100  | COM   |
| LCMXO2280C-4TN100C  | 2280 | 1.8V/2.5V/3.3V | 73   | -4    | Lead-Free TQFP  | 100  | COM   |
| LCMXO2280C-5TN100C  | 2280 | 1.8V/2.5V/3.3V | 73   | -5    | Lead-Free TQFP  | 100  | COM   |
| LCMXO2280C-3TN144C  | 2280 | 1.8V/2.5V/3.3V | 113  | -3    | Lead-Free TQFP  | 144  | COM   |
| LCMXO2280C-4TN144C  | 2280 | 1.8V/2.5V/3.3V | 113  | -4    | Lead-Free TQFP  | 144  | COM   |
| LCMXO2280C-5TN144C  | 2280 | 1.8V/2.5V/3.3V | 113  | -5    | Lead-Free TQFP  | 144  | COM   |
| LCMXO2280C-3MN132C  | 2280 | 1.8V/2.5V/3.3V | 101  | -3    | Lead-Free csBGA | 132  | COM   |
| LCMXO2280C-4MN132C  | 2280 | 1.8V/2.5V/3.3V | 101  | -4    | Lead-Free csBGA | 132  | COM   |
| LCMXO2280C-5MN132C  | 2280 | 1.8V/2.5V/3.3V | 101  | -5    | Lead-Free csBGA | 132  | COM   |
| LCMXO2280C-3BN256C  | 2280 | 1.8V/2.5V/3.3V | 211  | -3    | Lead-Free caBGA | 256  | COM   |
| LCMXO2280C-4BN256C  | 2280 | 1.8V/2.5V/3.3V | 211  | -4    | Lead-Free caBGA | 256  | COM   |
| LCMXO2280C-5BN256C  | 2280 | 1.8V/2.5V/3.3V | 211  | -5    | Lead-Free caBGA | 256  | COM   |
| LCMXO2280C-3FTN256C | 2280 | 1.8V/2.5V/3.3V | 211  | -3    | Lead-Free ftBGA | 256  | COM   |
| LCMXO2280C-4FTN256C | 2280 | 1.8V/2.5V/3.3V | 211  | -4    | Lead-Free ftBGA | 256  | COM   |
| LCMXO2280C-5FTN256C | 2280 | 1.8V/2.5V/3.3V | 211  | -5    | Lead-Free ftBGA | 256  | COM   |
| LCMXO2280C-3FTN324C | 2280 | 1.8V/2.5V/3.3V | 271  | -3    | Lead-Free ftBGA | 324  | COM   |
| LCMXO2280C-4FTN324C | 2280 | 1.8V/2.5V/3.3V | 271  | -4    | Lead-Free ftBGA | 324  | COM   |
| LCMXO2280C-5FTN324C | 2280 | 1.8V/2.5V/3.3V | 271  | -5    | Lead-Free ftBGA | 324  | COM   |

| Part Number       | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|-------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO256E-3TN100C | 256  | 1.2V           | 78   | -3    | Lead-Free TQFP  | 100  | COM   |
| LCMXO256E-4TN100C | 256  | 1.2V           | 78   | -4    | Lead-Free TQFP  | 100  | COM   |
| LCMXO256E-5TN100C | 256  | 1.2V           | 78   | -5    | Lead-Free TQFP  | 100  | COM   |
| LCMXO256E-3MN100C | 256  | 1.2V           | 78   | -3    | Lead-Free csBGA | 100  | COM   |
| LCMXO256E-4MN100C | 256  | 1.2V           | 78   | -4    | Lead-Free csBGA | 100  | COM   |
| LCMXO256E-5MN100C | 256  | 1.2V           | 78   | -5    | Lead-Free csBGA | 100  | COM   |

| Part Number        | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|--------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO640E-3TN100C  | 640  | 1.2V           | 74   | -3    | Lead-Free TQFP  | 100  | COM   |
| LCMXO640E-4TN100C  | 640  | 1.2V           | 74   | -4    | Lead-Free TQFP  | 100  | COM   |
| LCMXO640E-5TN100C  | 640  | 1.2V           | 74   | -5    | Lead-Free TQFP  | 100  | COM   |
| LCMXO640E-3MN100C  | 640  | 1.2V           | 74   | -3    | Lead-Free csBGA | 100  | COM   |
| LCMXO640E-4MN100C  | 640  | 1.2V           | 74   | -4    | Lead-Free csBGA | 100  | COM   |
| LCMXO640E-5MN100C  | 640  | 1.2V           | 74   | -5    | Lead-Free csBGA | 100  | COM   |
| LCMXO640E-3TN144C  | 640  | 1.2V           | 113  | -3    | Lead-Free TQFP  | 144  | COM   |
| LCMXO640E-4TN144C  | 640  | 1.2V           | 113  | -4    | Lead-Free TQFP  | 144  | COM   |
| LCMXO640E-5TN144C  | 640  | 1.2V           | 113  | -5    | Lead-Free TQFP  | 144  | COM   |
| LCMXO640E-3MN132C  | 640  | 1.2V           | 101  | -3    | Lead-Free csBGA | 132  | COM   |
| LCMXO640E-4MN132C  | 640  | 1.2V           | 101  | -4    | Lead-Free csBGA | 132  | COM   |
| LCMXO640E-5MN132C  | 640  | 1.2V           | 101  | -5    | Lead-Free csBGA | 132  | COM   |
| LCMXO640E-3BN256C  | 640  | 1.2V           | 159  | -3    | Lead-Free caBGA | 256  | COM   |
| LCMXO640E-4BN256C  | 640  | 1.2V           | 159  | -4    | Lead-Free caBGA | 256  | COM   |
| LCMXO640E-5BN256C  | 640  | 1.2V           | 159  | -5    | Lead-Free caBGA | 256  | COM   |
| LCMXO640E-3FTN256C | 640  | 1.2V           | 159  | -3    | Lead-Free ftBGA | 256  | COM   |
| LCMXO640E-4FTN256C | 640  | 1.2V           | 159  | -4    | Lead-Free ftBGA | 256  | COM   |
| LCMXO640E-5FTN256C | 640  | 1.2V           | 159  | -5    | Lead-Free ftBGA | 256  | COM   |

| Part Number       | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|-------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO256E-3TN100I | 256  | 1.2V           | 78   | -3    | Lead-Free TQFP  | 100  | IND   |
| LCMXO256E-4TN100I | 256  | 1.2V           | 78   | -4    | Lead-Free TQFP  | 100  | IND   |
| LCMXO256E-3MN100I | 256  | 1.2V           | 78   | -3    | Lead-Free csBGA | 100  | IND   |
| LCMXO256E-4MN100I | 256  | 1.2V           | 78   | -4    | Lead-Free csBGA | 100  | IND   |

| Part Number        | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|--------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO640E-3TN100I  | 640  | 1.2V           | 74   | -3    | Lead-Free TQFP  | 100  | IND   |
| LCMXO640E-4TN100I  | 640  | 1.2V           | 74   | -4    | Lead-Free TQFP  | 100  | IND   |
| LCMXO640E-3MN100I  | 640  | 1.2V           | 74   | -3    | Lead-Free csBGA | 100  | IND   |
| LCMXO640E-4MN100I  | 640  | 1.2V           | 74   | -4    | Lead-Free csBGA | 100  | IND   |
| LCMXO640E-3TN144I  | 640  | 1.2V           | 113  | -3    | Lead-Free TQFP  | 144  | IND   |
| LCMXO640E-4TN144I  | 640  | 1.2V           | 113  | -4    | Lead-Free TQFP  | 144  | IND   |
| LCMXO640E-3MN132I  | 640  | 1.2V           | 101  | -3    | Lead-Free csBGA | 132  | IND   |
| LCMXO640E-4MN132I  | 640  | 1.2V           | 101  | -4    | Lead-Free csBGA | 132  | IND   |
| LCMXO640E-3BN256I  | 640  | 1.2V           | 159  | -3    | Lead-Free caBGA | 256  | IND   |
| LCMXO640E-4BN256I  | 640  | 1.2V           | 159  | -4    | Lead-Free caBGA | 256  | IND   |
| LCMXO640E-3FTN256I | 640  | 1.2V           | 159  | -3    | Lead-Free ftBGA | 256  | IND   |
| LCMXO640E-4FTN256I | 640  | 1.2V           | 159  | -4    | Lead-Free ftBGA | 256  | IND   |

| Part Number         | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|---------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO1200E-3TN100I  | 1200 | 1.2V           | 73   | -3    | Lead-Free TQFP  | 100  | IND   |
| LCMXO1200E-4TN100I  | 1200 | 1.2V           | 73   | -4    | Lead-Free TQFP  | 100  | IND   |
| LCMXO1200E-3TN144I  | 1200 | 1.2V           | 113  | -3    | Lead-Free TQFP  | 144  | IND   |
| LCMXO1200E-4TN144I  | 1200 | 1.2V           | 113  | -4    | Lead-Free TQFP  | 144  | IND   |
| LCMXO1200E-3MN132I  | 1200 | 1.2V           | 101  | -3    | Lead-Free csBGA | 132  | IND   |
| LCMXO1200E-4MN132I  | 1200 | 1.2V           | 101  | -4    | Lead-Free csBGA | 132  | IND   |
| LCMXO1200E-3BN256I  | 1200 | 1.2V           | 211  | -3    | Lead-Free caBGA | 256  | IND   |
| LCMXO1200E-4BN256I  | 1200 | 1.2V           | 211  | -4    | Lead-Free caBGA | 256  | IND   |
| LCMXO1200E-3FTN256I | 1200 | 1.2V           | 211  | -3    | Lead-Free ftBGA | 256  | IND   |
| LCMXO1200E-4FTN256I | 1200 | 1.2V           | 211  | -4    | Lead-Free ftBGA | 256  | IND   |

| Part Number         | LUTs | Supply Voltage | I/Os | Grade | Package         | Pins | Temp. |
|---------------------|------|----------------|------|-------|-----------------|------|-------|
| LCMXO2280E-3TN100I  | 2280 | 1.2V           | 73   | -3    | Lead-Free TQFP  | 100  | IND   |
| LCMXO2280E-4TN100I  | 2280 | 1.2V           | 73   | -4    | Lead-Free TQFP  | 100  | IND   |
| LCMXO2280E-3TN144I  | 2280 | 1.2V           | 113  | -3    | Lead-Free TQFP  | 144  | IND   |
| LCMXO2280E-4TN144I  | 2280 | 1.2V           | 113  | -4    | Lead-Free TQFP  | 144  | IND   |
| LCMXO2280E-3MN132I  | 2280 | 1.2V           | 101  | -3    | Lead-Free csBGA | 132  | IND   |
| LCMXO2280E-4MN132I  | 2280 | 1.2V           | 101  | -4    | Lead-Free csBGA | 132  | IND   |
| LCMXO2280E-3BN256I  | 2280 | 1.2V           | 211  | -3    | Lead-Free caBGA | 256  | IND   |
| LCMXO2280E-4BN256I  | 2280 | 1.2V           | 211  | -4    | Lead-Free caBGA | 256  | IND   |
| LCMXO2280E-3FTN256I | 2280 | 1.2V           | 211  | -3    | Lead-Free ftBGA | 256  | IND   |
| LCMXO2280E-4FTN256I | 2280 | 1.2V           | 211  | -4    | Lead-Free ftBGA | 256  | IND   |
| LCMXO2280E-3FTN324I | 2280 | 1.2V           | 271  | -3    | Lead-Free ftBGA | 324  | IND   |
| LCMXO2280E-4FTN324I | 2280 | 1.2V           | 271  | -4    | Lead-Free ftBGA | 324  | IND   |