



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	285
Number of Logic Elements/Cells	2280
Total RAM Bits	28262
Number of I/O	101
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280e-5mn132c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MachXO Family Data Sheet Architecture

June 2013

Data Sheet DS1002

Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM[™] Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT use.

The MachXO registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO architecture provides up to two sysCLOCK[™] Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

^{© 2013} Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Figure 2-1. Top View of the MachXO1200 Device¹



1. Top view of the MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the MachXO640 Device





There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2-1 lists the signals associated with each Slice.

Figure 2-5. Slice Diagram



Notes:

Some inter-Slice signals are not shown. * Only PFUs at the edges have fast connections to the I/O cell.

Table 2-1. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the Slice
Output	Inter-PFU signal	FCO	Fast Carry Out ¹

1. See Figure 2-4 for connection details.

2. Requires two PFUs.







Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 2-9. Secondary Clocks for MachXO Devices





Figure 2-20. MachXO640 Banks



Figure 2-21. MachXO256 Banks



Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of



the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The MachXO "C" devices ($V_{CC} = 1.8/2.5/3.3V$) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tristated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <10mA	0	Typical <100uA
I/O Leakage	<10µA	<1mA	<10µA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

Table 2-11. Characteristics of Normal, Off and Sleep Modes

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1} ; MachXO640: V_{CCIO2} ; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.



For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)



Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	294	Ohms
R _P	Driver parallel resistor	121	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	1.35	V
V _{OL}	Output low voltage	1.15	V
V _{OD}	Output differential voltage	0.20	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	101.5	Ohms
IDC	DC output current	3.66	mA



MachXO Family Timing Adders^{1, 2, 3}

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters	-				
LVDS25 ⁴	LVDS	0.44	0.53	0.61	ns
BLVDS25 ^₄	BLVDS	0.44	0.53	0.61	ns
LVPECL33 ⁴	LVPECL	0.42	0.50	0.59	ns
LVTTL33	LVTTL	0.01	0.01	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	0.01	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	0.07	0.08	0.10	ns
LVCMOS15	LVCMOS 1.5	0.14	0.17	0.19	ns
LVCMOS12	LVCMOS 1.2	0.40	0.48	0.56	ns
PCI33 ^₄	PCI	0.01	0.01	0.01	ns
Output Adjusters	•		•		
LVDS25E	LVDS 2.5 E	-0.13	-0.15	-0.18	ns
LVDS25 ⁴	LVDS 2.5	-0.21	-0.26	-0.30	ns
BLVDS25	BLVDS 2.5	-0.03	-0.03	-0.04	ns
LVPECL33	LVPECL 3.3	0.04	0.04	0.05	ns
LVTTL33_4mA	LVTTL 4mA drive	0.04	0.04	0.05	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.07	0.08	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.01	-0.01	-0.01	ns
LVTTL33_16mA	LVTTL 16mA drive	0.50	0.60	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.04	0.04	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.06	0.07	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	-0.01	-0.01	-0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14mA drive	0.50	0.60	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.05	0.06	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.10	0.12	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	0.00	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14mA drive	0.34	0.40	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.11	0.13	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.05	0.06	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	-0.06	-0.07	-0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14mA drive	0.06	0.07	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.15	0.19	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.05	0.06	0.07	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.26	0.31	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.05	0.06	0.07	ns
PCI334	PCI33	1.85	2.22	2.59	ns

Over Recommended Operating Conditions

1. Timing adders are characterized but not tested on every device.

2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.

3. All other standards tested according to the appropriate specifications.

4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

Rev. A 0.19



MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Тур.	Max	Units
t _{PWRDN}	SLEEPN Low to Power Down	All	—		400	ns
		LCMXO256	—		400	μs
t _{PWRUP}	SI EEDN High to Power Up	LCMXO640	_		600	μs
	SLEEFN High to Fower op	LCMXO1200	_		800	μs
		LCMXO2280	—		1000	μs
t _{WSLEEPN}	SLEEPN Pulse Width	All	400	_		ns
t _{WAWAKE}	SLEEPN Pulse Rejection	All	_	—	100	ns

Rev. A 0.19

Flash Download Time



Symbol	Paran	neter	Min.	Тур.	Max.	Units
t _{REFRESH}		LCMXO256	_	_	0.4	ms
	Minimum V _{CC} or V _{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO640	_	_	0.6	ms
		LCMXO1200	_		0.8	ms
		LCMXO2280	_	_	1.0	ms

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t _{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t _{втсрн}	TCK [BSCAN] clock pulse width high	20	_	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	8	—	ns
t _{BTH}	TCK [BSCAN] hold time	10	—	ns
t _{BTRF}	TCK [BSCAN] rise/fall time	50	_	mV/ns
t _{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to output disabled	—	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	—	ns
t _{BTCRH}	BSCAN test capture register hold time	25	_	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

Rev. A 0.19



Figure 3-5. JTAG Port Timing Waveforms





MachXO Family Data Sheet Pinout Information

June 2013

Data Sheet DS1002

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designa- tions are L (Left), B (Bottom), R (Right), T (Top).
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.
P[Edge] [Row/Column	1/0	[A/B/C/D/E/F] indicates the PIO within the group to which the pad is connected.
Number]_[A/B/C/D/E/F]	1/0	Some of these user programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-up resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-up resistor enabled.
GSRN	I	Global RESET signal (active low). Dedicated pad, when not in use it can be used as an I/O pin.
TSALL	I	TSALL is a dedicated pad for the global output enable signal. When TSALL is high all the outputs are tristated. It is a dual function pin. When not in use, it can be used as an I/O pin.
NC	—	No connect.
GND	—	GND - Ground. Dedicated pins.
V _{CC}	—	VCC - The power supply pins for core logic. Dedicated pins.
V _{CCAUX}	_	VCCAUX - the Auxiliary power supply pin. This pin powers up a variety of internal circuits including all the differential and referenced input buffers. Dedicated pins.
V _{CCIOx}	_	V _{CCIO} - The power supply pins for I/O Bank x. Dedicated pins.
SLEEPN ¹	I	Sleep Mode pin - Active low sleep pin.b When this pin is held high, the device operates normally.b This pin has a weak internal pull-up, but when unused, an external pull-up to V_{CC} is recommended. When driven low, the device moves into Sleep mode after a specified time.
PLL and Clock Functions (Used	as user programmable I/O pins when not used for PLL or clock pins)
[LOC][0]_PLL[T, C]_IN	_	Reference clock (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
[LOC][0]_PLL[T, C]_FB	_	Optional feedback (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
PCLK [n]_[1:0]		Primary Clock Pads, n per side.
Test and Programming (De	dicate	d pins)
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	Ι	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	0	Output pin -Test Data output pin used to shift data out of the device using 1149.1.

1. Applies to MachXO "C" devices only. NC for "E" devices.

^{© 2013} Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.





Power Supply and NC (Cont.)

Signal	132 csBGA ¹	256 caBGA / 256 ftBGA ¹	324 ftBGA ¹
VCC	H3, P6, G12, C7	G7, G10, K7, K10	F14, G11, G9, H7, L7, M9
VCCIO0	LCMXO640: B11, C5 LCMXO1200/2280: C5	LCMXO640: F8, F7, F9, F10 LCMXO1200/2280: F8, F7	G8, G7
VCCIO1	LCMXO640: L12, E12 LCMXO1200/2280: B11	LCMXO640: H11, G11, K11, J11 LCMXO1200/2280: F9, F10	G12, G10
VCCIO2	LCMXO640: N2, M10 LCMXO1200/2280: E12	LCMXO640: L9, L10, L8, L7 LCMXO1200/2280: H11, G11	J12, H12
VCCIO3	LCMXO640: D2, K3 LCMXO1200/2280: L12	LCMXO640: K6, J6, H6, G6 LCMXO1200/2280: K11, J11	L12, K12
VCCIO4	LCMXO640: None LCMXO1200/2280: M10	LCMXO640: None LCMXO1200/2280: L9, L10	M12, M11
VCCIO5	LCMXO640: None LCMXO1200/2280: N2	LCMXO640: None LCMXO1200/2280: L8, L7	M8, R9
VCCIO6	LCMXO640: None LCMXO1200/2280: K3	LCMXO640: None LCMXO1200/2280: K6, J6	M7, K7
VCCIO7	LCMXO640: None LCMXO1200/2280: D2	LCMXO640: None LCMXO1200/2280: H6, G6	H6, J7
VCCAUX	P7, A7	T9, A8	M10, F9
GND ²	F1, P9, J14, C9, A10, B4, L13, D13, P2, N11, E1, L2	A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16	E14, F16, H10, H11, H8, H9, J10, J11, J4, J8, J9, K10, K11, K17, K8, K9, L10, L11, L8, L9, N2, P14, P5, R7
NC ³		LCMXO640: E4, E5, F5, F6, C3, C2, G4, G5, H4, H5, K5, K4, M5, M4, P2, P3, N5, N6, M7, M8, N10, N11, R15, R16, P15, P16, M11, L11, N12, N13, M13, M12, K12, J12, F12, F13, E12, E13, D13, D14, B15, A15, C14, B14, E11, E10, E7, E6, D4, D3, B3, B2 LCMXO1200: None LCMXO2280: None	

Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
NC pins should not be connected to any active signals, VCC or GND.



LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA (Cont.)

		LCMXO256			LCMXO640				
Ball Number	Ball Function	Bank	Dual Function	Differen- tial	Ball Number	Ball Function	Bank	Dual Function	Differen- tial
A4	GNDIO0	0			A4	GNDIO0	0		
B4	PT3A	0		Т	B4	PT3B	0		С
A3	PT2F	0		С	A3	PT3A	0		Т
B3	PT2E	0		Т	B3	PT2F	0		С
A2	PT2D	0		С	A2	PT2E	0		Т
C3	PT2C	0		Т	C3	PT2B	0		С
A1	PT2B	0		С	A1	PT2C	0		
B2	PT2A	0		Т	B2	PT2A	0		Т
N9	GND	-			N9	GND	-		
B9	GND	-			B9	GND	-		
B5	VCCIO0	0			B5	VCCIO0	0		
A14	VCCIO0	0			A14	VCCIO1	1		
H14	VCCIO0	0			H14	VCCIO1	1		
P10	VCCIO1	1			P10	VCCIO2	2		
G1	VCCIO1	1			G1	VCCIO3	3		
P1	VCCIO1	1			P1	VCCIO3	3		

*NC for "E" devices.

**Primary clock inputs are single-ended.



LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA

		LCM>	(O640			LCMXO1200					LCMXO2280			
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO3	VCCIO3	3			VCCI07	VCCI07	7			VCCI07	VCCI07	7		
E4	NC				E4	PL2A	7		Т	E4	PL2A	7	LUM0_PLLT_FB_A	Т
E5	NC				E5	PL2B	7		С	E5	PL2B	7	LUM0 PLLC FB A	С
F5	NC				F5	PL3A	7		T*	F5	PL3A	7		T*
F6	NC				F6	PL3B	7		C*	F6	PL3B	7		C*
F3	PL3A	3		т	F3	PL3C	7		Т	F3	PL3C	7	LUM0 PLLT IN A	Т
F4	PL3B	3		С	F4	PL3D	7		С	F4	PL3D	7	LUM0_PLLC_IN_A	С
E3	PL2C	3		т	E3	PL4A	7		T*	E3	PL4A	7		T*
E2	PL2D	3		С	E2	PL4B	7		C*	E2	PL4B	7		C*
C3	NC				C3	PL4C	7		Т	C3	PL4C	7		Т
C2	NC				C2	PL4D	7		С	C2	PL4D	7		С
B1	PL2A	3		т	B1	PL5A	7		T*	B1	PL5A	7		T*
C1	PL2B	3		С	C1	PL5B	7		C*	C1	PL5B	7		C*
VCCIO3	VCCIO3	3			VCCI07	VCCI07	7			VCCI07	VCCI07	7		
GND	GNDIO3	3			GND	GNDI07	7			GND	GNDIO7	7		
D2	PL3C	3		т	D2	PL5C	7		Т	D2	PL6C	7		Т
D1	PL3D	3		С	D1	PL5D	7		С	D1	PL6D	7		С
F2	PL5A	3		Т	F2	PL6A	7		T*	F2	PL7A	7		T*
G2	PL5B	3	GSRN	С	G2	PL6B	7	GSRN	C*	G2	PL7B	7	GSRN	C*
E1	PL4A	3		Т	E1	PL6C	7		Т	E1	PL7C	7		Т
F1	PL4B	3		С	F1	PL6D	7		С	F1	PL7D	7		С
G4	NC				G4	PL7A	7		T*	G4	PL8A	7		T*
G5	NC				G5	PL7B	7		C*	G5	PL8B	7		C*
GND	GND	-			GND	GND	-			GND	GND	-		
G3	PL4C	3		Т	G3	PL7C	7		Т	G3	PL8C	7		Т
H3	PL4D	3		С	H3	PL7D	7		С	H3	PL8D	7		С
H4	NC				H4	PL8A	7		T*	H4	PL9A	7		T*
H5	NC				H5	PL8B	7		C*	H5	PL9B	7		C*
-	-				VCCI07	VCCI07	7		_	VCCI07	VCCI07	7		-
-	-				GND	GNDIO7	7			GND	GNDIO7	7		
G1	PL5C	3		Т	G1	PL8C	7		Т	G1	PL10C	7		Т
H1	PL5D	3		С	H1	PL8D	7		С	H1	PL10D	7		С
H2	PL6A	3		т	H2	PL9A	6		T*	H2	PL11A	6		T*
J2	PL6B	3		С	J2	PL9B	6		C*	J2	PL11B	6		C*
J3	PL7C	3		Т	J3	PL9C	6		Т	J3	PL11C	6		Т
КЗ	PL7D	3		С	K3	PL9D	6		С	K3	PL11D	6		С
J1	PL6C	3		т	J1	PL10A	6		T*	J1	PL12A	6		T*
-	-				VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
-	-				GND	GNDIO6	6			GND	GNDIO6	6		
K1	PL6D	3		С	K1	PL10B	6		C*	K1	PL12B	6		C*
K2	PL9A	3		Т	K2	PL10C	6		т	K2	PL12C	6		Т
L2	PL9B	3		С	L2	PL10D	6		С	L2	PL12D	6		С
L1	PL7A	3		T	L1	PL11A	6		T*	L1	PL13A	6		T*
M1	PL7B	3		С	M1	PL11B	6		C*	M1	PL13B	6		C*
P1	PL8D	3		С	P1	PL11D	6		С	P1	PL14D	6		С
N1	PL8C	3	TSALL	T	N1	PL11C	6	TSALL	Т	N1	PL14C	6	TSALL	Т
L3	PL10A	3		т	L3	PL12A	6		T*	L3	PL15A	6		T*
M3	PL10B	3		С	M3	PL12B	6		C*	M3	PL15B	6		C*
M2	PL9C	3		Т	M2	PL12C	6		T	M2	PL15C	6		Т
N2	PL9D	3		C	N2	PL12D	6		C	N2	PL15D	6		C
VCCI03	VCCIO3	3		-	VCCIO6	VCCIO6	6		-	VCCIO6	VCCIO6	6		-
GND	GNDIO3	3	<u> </u>		GND	GNDIO6	6			GND	GNDIO6	6		
0.10	3.15100	, J		L	D	0	, J		I	3.10	0	, J		1



LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280								
Ball Number	Ball Function	Bank	Dual Function	Differential				
J13	PR10C	2		Т				
M18	PR10B	2		C*				
L18	PR10A	2		Τ*				
GND	GNDIO2	2						
VCCIO2	VCCIO2	2						
H16	PR9D	2		С				
H14	PR9C	2		Т				
K18	PR9B	2		C*				
J18	PR9A	2		Τ*				
J17	PR8D	2		С				
VCC	VCC	-						
H18	PR8C	2		Т				
H17	PR8B	2		C*				
G17	PR8A	2		T*				
H13	PR7D	2		С				
H15	PR7C	2		Т				
G18	PR7B	2		C*				
F18	PR7A	2		T*				
G14	PR6D	2		С				
G16	PR6C	2		Т				
VCCIO2	VCCIO2	2						
GND	GNDIO2	2						
E18	PR6B	2		C*				
F17	PR6A	2		Τ*				
G13	PR5D	2		С				
G15	PR5C	2		Т				
E17	PR5B	2		C*				
E16	PR5A	2		Τ*				
GND	GND	-						
F15	PR4D	2		С				
E15	PR4C	2		Т				
D17	PR4B	2		C*				
D18	PR4A	2		Τ*				
B18	PR3D	2		С				
C18	PR3C	2		Т				
C16	PR3B	2		C*				
D16	PR3A	2		Τ*				
C17	PR2B	2		С				
D15	PR2A	2		Т				
VCCIO2	VCCIO2	2						
GND	GNDIO2	2						
GND	GNDIO1	1						
VCCIO1	VCCIO1	1						



LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280								
Ball Number	Ball Function	Bank	Dual Function	Differential				
E13	PT16D	1		С				
C15	PT16C	1		Т				
F13	PT16B	1		С				
D14	PT16A	1		Т				
A18	PT15D	1		С				
B17	PT15C	1		Т				
A16	PT15B	1		С				
A17	PT15A	1		Т				
VCC	VCC	-						
D13	PT14D	1		С				
F12	PT14C	1		Т				
C14	PT14B	1		С				
E12	PT14A	1		Т				
C13	PT13D	1		С				
B16	PT13C	1		Т				
B15	PT13B	1		С				
A15	PT13A	1		Т				
VCCIO1	VCCIO1	1						
GND	GNDIO1	1						
B14	PT12F	1		С				
A14	PT12E	1		Т				
D12	PT12D	1		С				
F11	PT12C	1		Т				
B13	PT12B	1		С				
A13	PT12A	1		Т				
C12	PT11D	1		С				
GND	GND	-						
B12	PT11C	1		Т				
E11	PT11B	1		С				
D11	PT11A	1		Т				
C11	PT10F	1		С				
A12	PT10E	1		Т				
VCCIO1	VCCIO1	1						
GND	GNDIO1	1						
F10	PT10D	1		С				
D10	PT10C	1		Т				
B11	PT10B	1	PCLK1_1***	С				
A11	PT10A	1		Т				
E10	PT9D	1		С				
C10	PT9C	1		Т				
D9	PT9B	1	PCLK1_0***	С				
E9	PT9A	1		Т				
B10	PT8F	0		С				



Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the <u>Thermal Management</u> document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1090 Power Estimation and Management for MachXO Devices
- Power Calculator tool included with the Lattice ispLEVER design tool, or as a standalone download from <u>www.latticesemi.com/software</u>



Conventional Packaging

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.	
LCMXO256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM	
LCMXO256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM	
LCMXO256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM	
LCMXO256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM	
LCMXO256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM	
LCMXO256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM	

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMXO640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMXO640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMXO640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMXO640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMXO640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMXO640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMXO640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMXO640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMXO640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMXO640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMXO640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMXO1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMXO1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMXO1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMXO1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMXO1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMXO1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMXO1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMXO1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM



Part Number	LUTs	Supply Voltage	l/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100C	1200	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200E-4TN100C	1200	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200E-5TN100C	1200	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200E-3TN144C	1200	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200E-4TN144C	1200	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200E-5TN144C	1200	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200E-3MN132C	1200	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200E-4MN132C	1200	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200E-5MN132C	1200	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200E-3BN256C	1200	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200E-4BN256C	1200	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200E-5BN256C	1200	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200E-3FTN256C	1200	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200E-4FTN256C	1200	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200E-5FTN256C	1200	1.2V	211	-5	Lead-Free ftBGA	256	COM
·			•	•			•

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100C	2280	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280E-4TN100C	2280	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280E-5TN100C	2280	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280E-3TN144C	2280	1.2V	113	-3	Lead-Free TQFP	144	СОМ
LCMXO2280E-4TN144C	2280	1.2V	113	-4	Lead-Free TQFP	144	СОМ
LCMXO2280E-5TN144C	2280	1.2V	113	-5	Lead-Free TQFP	144	СОМ
LCMXO2280E-3MN132C	2280	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280E-4MN132C	2280	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280E-5MN132C	2280	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280E-3BN256C	2280	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280E-4BN256C	2280	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280E-5BN256C	2280	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280E-3FTN256C	2280	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280E-4FTN256C	2280	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280E-5FTN256C	2280	1.2V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280E-3FTN324C	2280	1.2V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280E-4FTN324C	2280	1.2V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280E-5FTN324C	2280	1.2V	271	-5	Lead-Free ftBGA	324	COM



Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3TN100I	256	1.2V	78	-3	Lead-Free TQFP	100	IND
LCMXO256E-4TN100I	256	1.2V	78	-4	Lead-Free TQFP	100	IND
LCMXO256E-3MN100I	256	1.2V	78	-3	Lead-Free csBGA	100	IND
LCMXO256E-4MN100I	256	1.2V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	l/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN100I	640	1.2V	74	-3	Lead-Free TQFP	100	IND
LCMXO640E-4TN100I	640	1.2V	74	-4	Lead-Free TQFP	100	IND
LCMXO640E-3MN100I	640	1.2V	74	-3	Lead-Free csBGA	100	IND
LCMXO640E-4MN100I	640	1.2V	74	-4	Lead-Free csBGA	100	IND
LCMXO640E-3TN144I	640	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO640E-4TN144I	640	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO640E-3MN132I	640	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO640E-4MN132I	640	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO640E-3BN256I	640	1.2V	159	-3	Lead-Free caBGA	256	IND
LCMXO640E-4BN256I	640	1.2V	159	-4	Lead-Free caBGA	256	IND
LCMXO640E-3FTN256I	640	1.2V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640E-4FTN256I	640	1.2V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	l/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100I	1200	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200E-4TN100I	1200	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200E-3TN144I	1200	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200E-4TN144I	1200	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200E-3MN132I	1200	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200E-4MN132I	1200	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200E-3BN256I	1200	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200E-4BN256I	1200	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200E-3FTN256I	1200	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200E-4FTN256I	1200	1.2V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100I	2280	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280E-4TN100I	2280	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280E-3TN144I	2280	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280E-4TN144I	2280	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280E-3MN132I	2280	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280E-4MN132I	2280	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280E-3BN256I	2280	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280E-4BN256I	2280	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280E-3FTN256I	2280	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280E-4FTN256I	2280	1.2V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280E-3FTN324I	2280	1.2V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280E-4FTN324I	2280	1.2V	271	-4	Lead-Free ftBGA	324	IND