# Lattice Semiconductor Corporation - LCMXO2280E-5TN144C Datasheet

**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 285 |
| Number of Logic Elements/Cells | 2280 |
| Total RAM Bits | 28262 |
| Number of I/O | 113 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2280e-5tn144c |

# MachXO Family Data Sheet Introduction

June 2013 Data Sheet DS1002

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- **Sleep Mode**
  - Allows up to 100x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **High I/O to Logic Density**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.7 Kbits distributed RAM
  - Dedicated FIFO control logic
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide, and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - Onboard oscillator
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
  - IEEE 1532 compliant in-system programming

## Introduction

The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, and control logic. These devices bring together the best features of CPLD and FPGA devices on a single chip.

***Table 1-1. MachXO Family Selection Guide***

| Device | LCMXO256 | LCMXO640 | LCMXO1200 | LCMXO2280 |
|---|---|---|---|---|
| LUTs | 256 | 640 | 1200 | 2280 |
| Dist. RAM (Kbits) | 2.0 | 6.1 | 6.4 | 7.7 |
| EBR SRAM (Kbits) | 0 | 0 | 9.2 | 27.6 |
| Number of EBR SRAM Blocks (9 Kbits) | 0 | 0 | 1 | 3 |
| $V_{CC}$ Voltage | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V |
| Number of PLLs | 0 | 0 | 1 | 2 |
| Max. I/O | 78 | 159 | 211 | 271 |
| **Packages** | | | | |
| 100-pin TQFP (14x14 mm) | 78 | 74 | 73 | 73 |
| 144-pin TQFP (20x20 mm) | | 113 | 113 | 113 |
| 100-ball csBGA (8x8 mm) | 78 | 74 | | |
| 132-ball csBGA (8x8 mm) | | 101 | 101 | 101 |
| 256-ball caBGA (14x14 mm) | | 159 | 211 | 211 |
| 256-ball ftBGA (17x17 mm) | | 159 | 211 | 211 |
| 324-ball ftBGA (19x19 mm) | | | | 271 |

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip, high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Popular logic synthesis tools provide synthesis library support for MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

## sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

***Figure 2-10. PLL Diagram***

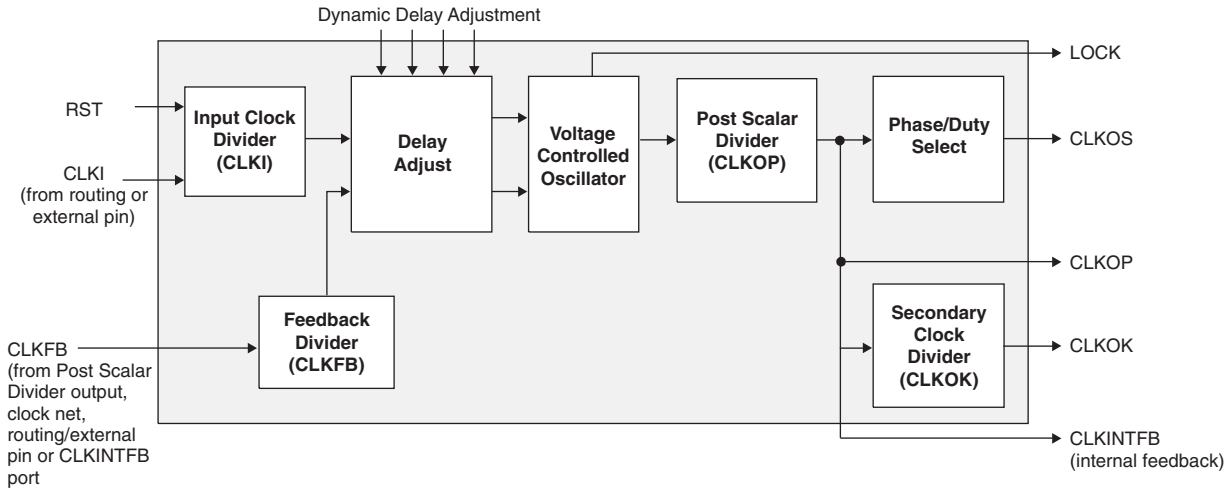
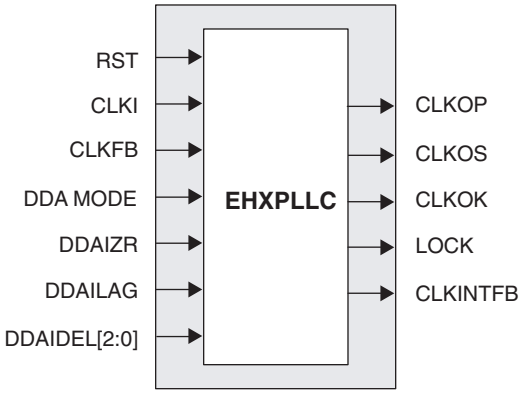



Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

***Figure 2-11. PLL Primitive***



The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

**FIFO Configuration**

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2-7.

***Table 2-7. Programmable FIFO Flag Ranges***

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

**Memory Core Reset**

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

*Table 2-8. I/O Support Device by Device*

| | MachXO256 | MachXO640 | MachXO1200 | MachXO2280 |
|---|---|---|---|---|
| Number of I/O Banks | 2 | 4 | 8 | 8 |
| Type of Input Buffers | Single-ended (all I/O Banks) | Single-ended (all I/O Banks) | Single-ended (all I/O Banks)<br><br>Differential Receivers (all I/O Banks) | Single-ended (all I/O Banks)<br><br>Differential Receivers (all I/O Banks) |
| Types of Output Buffers | Single-ended buffers with complementary outputs (all I/O Banks) | Single-ended buffers with complementary outputs (all I/O Banks) | Single-ended buffers with complementary outputs (all I/O Banks)<br><br>Differential buffers with true LVDS outputs (50% on left and right side) | Single-ended buffers with complementary outputs (all I/O Banks)<br><br>Differential buffers with true LVDS outputs (50% on left and right side) |
| Differential Output Emulation Capability | All I/O Banks | All I/O Banks | All I/O Banks | All I/O Banks |
| PCI Support | No | No | Top side only | Top side only |

*Table 2-9. Supported Input Standards*

| | VCCIO (Typ.) | | | | |
|---|---|---|---|---|---|
| **Input Standard** | **3.3V** | **2.5V** | **1.8V** | **1.5V** | **1.2V** |
| **Single Ended Interfaces** | | | | | |
| LVTTL | Yes | Yes | Yes | Yes | Yes |
| LVCMOS33 | Yes | Yes | Yes | Yes | Yes |
| LVCMOS25 | Yes | Yes | Yes | Yes | Yes |
| LVCMOS18 | | | Yes | | |
| LVCMOS15 | | | | Yes | |
| LVCMOS12 | Yes | Yes | Yes | Yes | Yes |
| PCI[1] | Yes | | | | |
| **Differential Interfaces** | | | | | |
| BLVDS[2], LVDS[2], LVPECL[2], RSDS[2] | Yes | Yes | Yes | Yes | Yes |

1. Top Banks of MachXO1200 and MachXO2280 devices only.
2. MachXO1200 and MachXO2280 devices only.

## Initialization Supply Current[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | 13 | mA |
| | | LCMXO640C | 17 | mA |
| | | LCMXO1200C | 21 | mA |
| | | LCMXO2280C | 23 | mA |
| | | LCMXO256E | 10 | mA |
| | | LCMXO640E | 14 | mA |
| | | LCMXO1200E | 18 | mA |
| | | LCMXO2280E | 20 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256E/C | 10 | mA |
| | | LCMXO640E/C | 13 | mA |
| | | LCMXO1200E/C | 24 | mA |
| | | LCMXO2280E/C | 25 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All devices | 2 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at $V_{CCIO}$ or GND.
3. Frequency = 0MHz.
4. Typical user pattern.
5. $T_J$ = 25°C, power supplies at nominal voltage.
6. Per Bank, $V_{CCIO}$ = 2.5V. Does not include pull-up/pull-down.

## Programming and Erase Flash Supply Current[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | 9 | mA |
| | | LCMXO640C | 11 | mA |
| | | LCMXO1200C | 16 | mA |
| | | LCMXO2280C | 22 | mA |
| | | LCMXO256E | 6 | mA |
| | | LCMXO640E | 8 | mA |
| | | LCMXO1200E | 12 | mA |
| | | LCMXO2280E | 14 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256C/E | 8 | mA |
| | | LCMXO640C/E | 10 | mA |
| | | LCMXO1200/E | 15 | mA |
| | | LCMXO2280C/E | 16 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All devices | 2 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at $V_{CCIO}$ or GND.
3. Typical user pattern.
4. JTAG programming is at 25MHz.
5. $T_J$ = 25°C, power supplies at nominal voltage.
6. Per Bank. $V_{CCIO}$ = 2.5V. Does not include pull-up/pull-down.

*Table 3-1. LVDS DC Conditions*

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ω |
| $R_S$ | Driver series resistor | 294 | Ω |
| $R_P$ | Driver parallel resistor | 121 | Ω |
| $R_T$ | Receiver termination | 100 | Ω |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | Ω |
| $I_{DC}$ | DC output current | 3.66 | mA |

## BLVDS

The MachXO family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. The input standard is supported by the LVDS differential input buffer on certain devices. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

*Figure 3-2. BLVDS Multi-point Output Example*

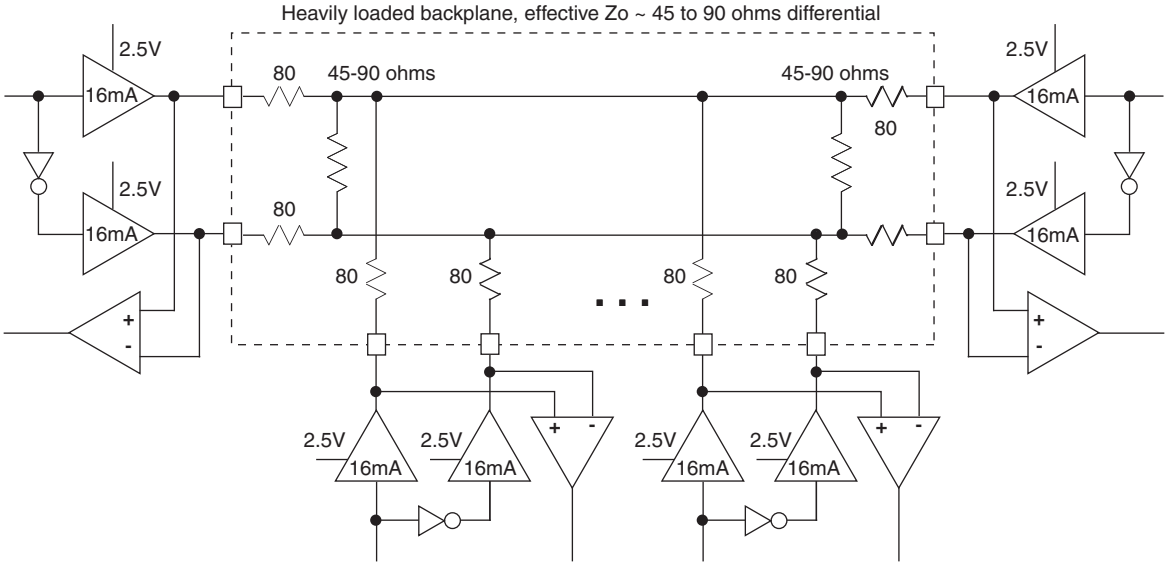


*Table 3-2. BLVDS DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | Ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ohms |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

## LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

*Figure 3-3. Differential LVPECL*

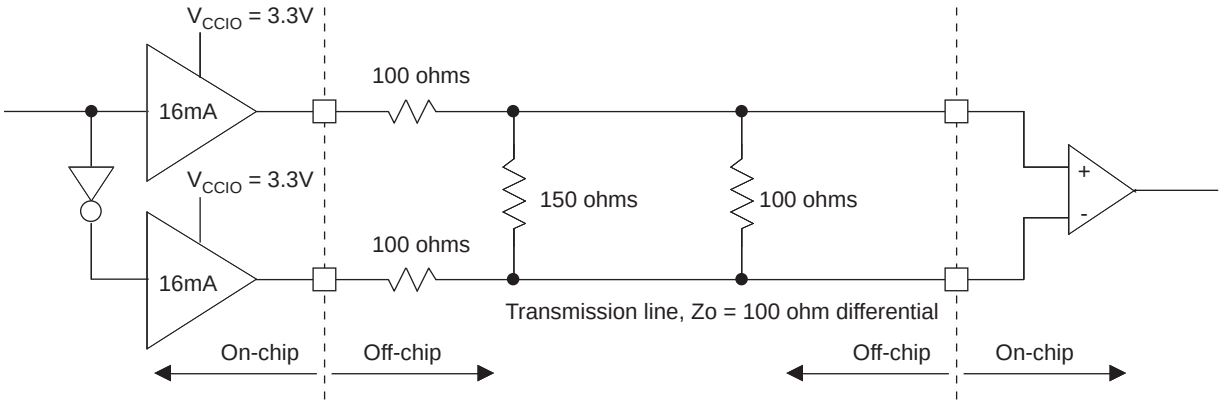



*Table 3-3. LVPECL DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | Ohms |
| $R_P$ | Driver parallel resistor | 150 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | Ohms |
| $I_{DC}$ | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

# MachXO External Switching Characteristics[1]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (Using Global Clock without PLL)[1]** | | | | | | | | | |
| $t_{PD}$ | Best Case $t_{PD}$ Through 1 LUT | LCMXO256 | — | 3.5 | — | 4.2 | — | 4.9 | ns |
| | | LCMXO640 | — | 3.5 | — | 4.2 | — | 4.9 | ns |
| | | LCMXO1200 | — | 3.6 | — | 4.4 | — | 5.1 | ns |
| | | LCMXO2280 | — | 3.6 | — | 4.4 | — | 5.1 | ns |
| $t_{CO}$ | Best Case Clock to Output - From PFU | LCMXO256 | — | 4.0 | — | 4.8 | — | 5.6 | ns |
| | | LCMXO640 | — | 4.0 | — | 4.8 | — | 5.7 | ns |
| | | LCMXO1200 | — | 4.3 | — | 5.2 | — | 6.1 | ns |
| | | LCMXO2280 | — | 4.3 | — | 5.2 | — | 6.1 | ns |
| $t_{SU}$ | Clock to Data Setup - To PFU | LCMXO256 | 1.3 | — | 1.6 | — | 1.8 | — | ns |
| | | LCMXO640 | 1.1 | — | 1.3 | — | 1.5 | — | ns |
| | | LCMXO1200 | 1.1 | — | 1.3 | — | 1.6 | — | ns |
| | | LCMXO2280 | 1.1 | — | 1.3 | — | 1.5 | — | ns |
| $t_{H}$ | Clock to Data Hold - To PFU | LCMXO256 | -0.3 | — | -0.3 | — | -0.3 | — | ns |
| | | LCMXO640 | -0.1 | — | -0.1 | — | -0.1 | — | ns |
| | | LCMXO1200 | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| | | LCMXO2280 | -0.4 | — | -0.4 | — | -0.4 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | LCMXO256 | — | 600 | — | 550 | — | 500 | MHz |
| | | LCMXO640 | — | 600 | — | 550 | — | 500 | MHz |
| | | LCMXO1200 | — | 600 | — | 550 | — | 500 | MHz |
| | | LCMXO2280 | — | 600 | — | 550 | — | 500 | MHz |
| $t_{SKEW\_PRI}$ | Global Clock Skew Across Device | LCMXO256 | — | 200 | — | 220 | — | 240 | ps |
| | | LCMXO640 | — | 200 | — | 220 | — | 240 | ps |
| | | LCMXO1200 | — | 220 | — | 240 | — | 260 | ps |
| | | LCMXO2280 | — | 220 | — | 240 | — | 260 | ps |

1. General timing numbers based on LVCMOS2.5V, 12 mA.

# MachXO Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4\_PFU}$ | LUT4 delay (A to D inputs to F output) | — | 0.28 | — | 0.34 | — | 0.39 | ns |
| $t_{LUT6\_PFU}$ | LUT6 delay (A to D inputs to OFX output) | — | 0.44 | — | 0.53 | — | 0.62 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to output of PFU | — | 0.90 | — | 1.08 | — | 1.26 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) input setup time | 0.10 | — | 0.13 | — | 0.15 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) input hold time | -0.05 | — | -0.06 | — | -0.07 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D input setup time | 0.13 | — | 0.16 | — | 0.18 | — | ns |
| $t_{HD\_PFU}$ | Clock to D input hold time | -0.03 | — | -0.03 | — | -0.04 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q delay, D-type register configuration | — | 0.40 | — | 0.48 | — | 0.56 | ns |
| $t_{LE2Q\_PFU}$ | Clock to Q delay latch configuration | — | 0.53 | — | 0.64 | — | 0.74 | ns |
| $t_{LD2Q\_PFU}$ | D to Q throughput delay when latch is enabled | — | 0.55 | — | 0.66 | — | 0.77 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output | — | 0.40 | — | 0.48 | — | 0.56 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | -0.18 | — | -0.22 | — | -0.25 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.28 | — | 0.34 | — | 0.39 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | -0.46 | — | -0.56 | — | -0.65 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.71 | — | 0.85 | — | 0.99 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | -0.22 | — | -0.26 | — | -0.30 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.33 | — | 0.40 | — | 0.47 | — | ns |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay | — | 0.75 | — | 0.90 | — | 1.06 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay | — | 1.29 | — | 1.54 | — | 1.80 | ns |
| **EBR Timing (1200 and 2280 Devices Only)** | | | | | | | | |
| $t_{CO\_EBR}$ | Clock to output from Address or Data with no output register | — | 2.24 | — | 2.69 | — | 3.14 | ns |
| $t_{COO\_EBR}$ | Clock to output from EBR output Register | — | 0.54 | — | 0.64 | — | 0.75 | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory | -0.26 | — | -0.31 | — | -0.37 | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory | 0.41 | — | 0.49 | — | 0.57 | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory | -0.26 | — | -0.31 | — | -0.37 | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory | 0.41 | — | 0.49 | — | 0.57 | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to EBR Memory | -0.17 | — | -0.20 | — | -0.23 | — | ns |
| $t_{HWREN\_EBR}$ | Hold Write/Read Enable to EBR Memory | 0.26 | — | 0.31 | — | 0.36 | — | ns |
| $t_{SUCE\_EBR}$ | Clock Enable Setup Time to EBR Output Register | 0.19 | — | 0.23 | — | 0.27 | — | ns |
| $t_{HCE\_EBR}$ | Clock Enable Hold Time to EBR Output Register | -0.13 | — | -0.16 | — | -0.18 | — | ns |
| $t_{RSTO\_EBR}$ | Reset To Output Delay Time from EBR Output Register | — | 1.03 | — | 1.23 | — | 1.44 | ns |
| **PLL Parameters (1200 and 2280 Devices Only)** | | | | | | | | |
| $t_{RSTREC}$ | Reset Recovery to Rising Clock | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| $t_{RSTSU}$ | Reset Signal Setup Time | 1.00 | — | 1.00 | — | 1.00 | — | ns |

1. Internal parameters are characterized but not tested on every device.

Rev. A 0.19

## LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | LCMXO256 | | | | LCMXO640 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 85 | PT4B | 0 | PCLK0_1** | C | PT6B | 0 | PCLK0_1** | |
| 86 | PT4A | 0 | PCLK0_0** | T | PT5B | 0 | PCLK0_0** | C |
| 87 | PT3D | 0 | | C | PT5A | 0 | | T |
| 88 | VCCAUX | - | | | VCCAUX | - | | |
| 89 | PT3C | 0 | | T | PT4F | 0 | | |
| 90 | VCC | - | | | VCC | - | | |
| 91 | PT3B | 0 | | C | PT3F | 0 | | |
| 92 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 93 | GNDIO0 | 0 | | | GNDIO0 | 0 | | |
| 94 | PT3A | 0 | | T | PT3B | 0 | | C |
| 95 | PT2F | 0 | | C | PT3A | 0 | | T |
| 96 | PT2E | 0 | | T | PT2F | 0 | | C |
| 97 | PT2D | 0 | | C | PT2E | 0 | | T |
| 98 | PT2C | 0 | | T | PT2B | 0 | | C |
| 99 | PT2B | 0 | | C | PT2C | 0 | | |
| 100 | PT2A | 0 | | T | PT2A | 0 | | T |

* NC for “E” devices.
** Primary clock inputs are single-ended.

## LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA (Cont.)

| LCMXO256 | | | | | LCMXO640 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Dual Function | Differen-tial | Ball Number | Ball Function | Bank | Dual Function | Differen-tial |
| P13 | PB5A | 1 | | | P13 | PB9C | 2 | | T |
| M12* | SLEEPN | - | SLEEPN | | M12* | SLEEPN | - | SLEEPN | |
| P14 | PB5C | 1 | | T | P14 | PB9D | 2 | | C |
| N13 | PB5D | 1 | | C | N13 | PB9F | 2 | | |
| N14 | PR9B | 0 | | C | N14 | PR11D | 1 | | C |
| M14 | PR9A | 0 | | T | M14 | PR11B | 1 | | C |
| L13 | PR8B | 0 | | C | L13 | PR11C | 1 | | T |
| L14 | PR8A | 0 | | T | L14 | PR11A | 1 | | T |
| M13 | PR7D | 0 | | C | M13 | PR10D | 1 | | C |
| K14 | PR7C | 0 | | T | K14 | PR10C | 1 | | T |
| K13 | PR7B | 0 | | C | K13 | PR10B | 1 | | C |
| J14 | PR7A | 0 | | T | J14 | PR10A | 1 | | T |
| J13 | PR6B | 0 | | C | J13 | PR9D | 1 | | |
| H13 | PR6A | 0 | | T | H13 | PR9B | 1 | | |
| G14 | GNDIO0 | 0 | | | G14 | GNDIO1 | 1 | | |
| G13 | PR5D | 0 | | C | G13 | PR7B | 1 | | |
| F14 | PR5C | 0 | | T | F14 | PR6C | 1 | | |
| F13 | PR5B | 0 | | C | F13 | PR6B | 1 | | |
| E14 | PR5A | 0 | | T | E14 | PR5D | 1 | | |
| E13 | PR4B | 0 | | C | E13 | PR5B | 1 | | |
| D14 | PR4A | 0 | | T | D14 | PR4D | 1 | | |
| D13 | PR3D | 0 | | C | D13 | PR4B | 1 | | |
| C14 | PR3C | 0 | | T | C14 | PR3D | 1 | | |
| C13 | PR3B | 0 | | C | C13 | PR3B | 1 | | |
| B14 | PR3A | 0 | | T | B14 | PR2D | 1 | | |
| C12 | PR2B | 0 | | C | C12 | PR2B | 1 | | |
| B13 | GNDIO0 | 0 | | | B13 | GNDIO1 | 1 | | |
| A13 | PR2A | 0 | | T | A13 | PT9F | 0 | | C |
| A12 | PT5C | 0 | | | A12 | PT9E | 0 | | T |
| B11 | PT5B | 0 | | C | B11 | PT9C | 0 | | |
| A11 | PT5A | 0 | | T | A11 | PT9A | 0 | | |
| B12 | PT4F | 0 | | C | B12 | VCCIO0 | 0 | | |
| A10 | PT4E | 0 | | T | A10 | GNDIO0 | 0 | | |
| B10 | PT4D | 0 | | C | B10 | PT7E | 0 | | |
| A9 | PT4C | 0 | | T | A9 | PT7A | 0 | | |
| A8 | PT4B | 0 | PCLK0_1** | C | A8 | PT6B | 0 | PCLK0_1** | |
| B8 | PT4A | 0 | PCLK0_0** | T | B8 | PT5B | 0 | PCLK0_0** | C |
| A7 | PT3D | 0 | | C | A7 | PT5A | 0 | | T |
| B7 | VCCAUX | - | | | B7 | VCCAUX | - | | |
| A6 | PT3C | 0 | | T | A6 | PT4F | 0 | | |
| B6 | VCC | - | | | B6 | VCC | - | | |
| A5 | PT3B | 0 | | C | A5 | PT3F | 0 | | |

## LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA (Cont.)

| LCMXO256 | | | | | LCMXO640 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Dual Function | Differen-tial | Ball Number | Ball Function | Bank | Dual Function | Differen-tial |
| A4 | GNDIO0 | 0 | | | A4 | GNDIO0 | 0 | | |
| B4 | PT3A | 0 | | T | B4 | PT3B | 0 | | C |
| A3 | PT2F | 0 | | C | A3 | PT3A | 0 | | T |
| B3 | PT2E | 0 | | T | B3 | PT2F | 0 | | C |
| A2 | PT2D | 0 | | C | A2 | PT2E | 0 | | T |
| C3 | PT2C | 0 | | T | C3 | PT2B | 0 | | C |
| A1 | PT2B | 0 | | C | A1 | PT2C | 0 | | |
| B2 | PT2A | 0 | | T | B2 | PT2A | 0 | | T |
| N9 | GND | - | | | N9 | GND | - | | |
| B9 | GND | - | | | B9 | GND | - | | |
| B5 | VCCIO0 | 0 | | | B5 | VCCIO0 | 0 | | |
| A14 | VCCIO0 | 0 | | | A14 | VCCIO1 | 1 | | |
| H14 | VCCIO0 | 0 | | | H14 | VCCIO1 | 1 | | |
| P10 | VCCIO1 | 1 | | | P10 | VCCIO2 | 2 | | |
| G1 | VCCIO1 | 1 | | | G1 | VCCIO3 | 3 | | |
| P1 | VCCIO1 | 1 | | | P1 | VCCIO3 | 3 | | |

*NC for “E” devices.
**Primary clock inputs are single-ended.

# LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

| LCMXO640 | | | | | LCMXO1200 | | | | | LCMXO2280 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball # | Ball Function | Bank | Dual Function | Differential | Ball # | Ball Function | Bank | Dual Function | Differential | Ball # | Ball Function | Bank | Dual Function | Differential |
| B9 | PT7B | 0 | | C | B9 | PT9B | 1 | | C | B9 | PT12D | 1 | | C |
| A9 | PT7A | 0 | | T | A9 | PT9A | 1 | | T | A9 | PT12C | 1 | | T |
| A8 | PT6B | 0 | PCLK0_1*** | C | A8 | PT7D | 1 | PCLK1_1*** | | A8 | PT10B | 1 | PCLK1_1*** | |
| B8 | PT6A | 0 | | T | B8 | PT7B | 1 | | | B8 | PT9D | 1 | | |
| C8 | PT5B | 0 | PCLK0_0*** | C | C8 | PT6F | 0 | PCLK1_0*** | | C8 | PT9B | 1 | PCLK1_0*** | |
| B7 | PT5A | 0 | | T | B7 | PT6D | 0 | | | B7 | PT8D | 0 | | |
| A7 | VCCAUX | - | | | A7 | VCCAUX | - | | | A7 | VCCAUX | - | | |
| C7 | VCC | - | | | C7 | VCC | - | | | C7 | VCC | - | | |
| A6 | PT4D | 0 | | C | A6 | PT5D | 0 | | C | A6 | PT7B | 0 | | C |
| B6 | PT4C | 0 | | T | B6 | PT5C | 0 | | T | B6 | PT7A | 0 | | T |
| C6 | PT3F | 0 | | C | C6 | PT5B | 0 | | C | C6 | PT6D | 0 | | |
| B5 | PT3E | 0 | | T | B5 | PT5A | 0 | | T | B5 | PT6E | 0 | | T |
| A5 | PT3D | 0 | | | A5 | PT4B | 0 | | | A5 | PT6F | 0 | | C |
| B4 | GNDIO0 | 0 | | | B4 | GNDIO0 | 0 | | | B4 | GNDIO0 | 0 | | |
| A4 | PT3B | 0 | | | A4 | PT3D | 0 | | C | A4 | PT4B | 0 | | C |
| C4 | PT2F | 0 | | | C4 | PT3C | 0 | | T | C4 | PT4A | 0 | | T |
| A3 | PT2D | 0 | | C | A3 | PT3B | 0 | | C | A3 | PT3B | 0 | | C |
| A2 | PT2C | 0 | | T | A2 | PT2B | 0 | | C | A2 | PT2B | 0 | | C |
| B3 | PT2B | 0 | | C | B3 | PT3A | 0 | | T | B3 | PT3A | 0 | | T |
| A1 | PT2A | 0 | | T | A1 | PT2A | 0 | | T | A1 | PT2A | 0 | | T |
| F1 | GND | - | | | F1 | GND | - | | | F1 | GND | - | | |
| P9 | GND | - | | | P9 | GND | - | | | P9 | GND | - | | |
| J14 | GND | - | | | J14 | GND | - | | | J14 | GND | - | | |
| C9 | GND | - | | | C9 | GND | - | | | C9 | GND | - | | |
| C5 | VCCIO0 | 0 | | | C5 | VCCIO0 | 0 | | | C5 | VCCIO0 | 0 | | |
| B11 | VCCIO0 | 0 | | | B11 | VCCIO1 | 1 | | | B11 | VCCIO1 | 1 | | |
| E12 | VCCIO1 | 1 | | | E12 | VCCIO2 | 2 | | | E12 | VCCIO2 | 2 | | |
| L12 | VCCIO1 | 1 | | | L12 | VCCIO3 | 3 | | | L12 | VCCIO3 | 3 | | |
| M10 | VCCIO2 | 2 | | | M10 | VCCIO4 | 4 | | | M10 | VCCIO4 | 4 | | |
| N2 | VCCIO2 | 2 | | | N2 | VCCIO5 | 5 | | | N2 | VCCIO5 | 5 | | |
| D2 | VCCIO3 | 3 | | | D2 | VCCIO7 | 7 | | | D2 | VCCIO7 | 7 | | |
| K3 | VCCIO3 | 3 | | | K3 | VCCIO6 | 6 | | | K3 | VCCIO6 | 6 | | |

*Supports true LVDS outputs.
**NC for “E” devices.
***Primary clock inputs arer single-ended.

# LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | LCMXO640 | | | | LCMXO1200 | | | | LCMXO2280 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 101 | PR3D | 1 | | C | PR4B | 2 | | C* | PR5B | 2 | | C* |
| 102 | PR3C | 1 | | T | PR4A | 2 | | T* | PR5A | 2 | | T* |
| 103 | PR3B | 1 | | C | PR3D | 2 | | C | PR4D | 2 | | C |
| 104 | PR2D | 1 | | C | PR3C | 2 | | T | PR4C | 2 | | T |
| 105 | PR3A | 1 | | T | PR3B | 2 | | C* | PR4B | 2 | | C* |
| 106 | PR2B | 1 | | C | PR3A | 2 | | T* | PR4A | 2 | | T* |
| 107 | PR2C | 1 | | T | PR2B | 2 | | C | PR3B | 2 | | C* |
| 108 | PR2A | 1 | | T | PR2A | 2 | | T | PR3A | 2 | | T* |
| 109 | PT9F | 0 | | C | PT11D | 1 | | C | PT16D | 1 | | C |
| 110 | PT9D | 0 | | C | PT11C | 1 | | T | PT16C | 1 | | T |
| 111 | PT9E | 0 | | T | PT11B | 1 | | C | PT16B | 1 | | C |
| 112 | PT9B | 0 | | C | PT11A | 1 | | T | PT16A | 1 | | T |
| 113 | PT9C | 0 | | T | PT10F | 1 | | C | PT15D | 1 | | C |
| 114 | PT9A | 0 | | T | PT10E | 1 | | T | PT15C | 1 | | T |
| 115 | PT8C | 0 | | | PT10D | 1 | | C | PT14B | 1 | | C |
| 116 | PT8B | 0 | | C | PT10C | 1 | | T | PT14A | 1 | | T |
| 117 | VCCIO0 | 0 | | | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 118 | GNDIO0 | 0 | | | GNDIO1 | 1 | | | GNDIO1 | 1 | | |
| 119 | PT8A | 0 | | T | PT9F | 1 | | C | PT12F | 1 | | C |
| 120 | PT7E | 0 | | | PT9E | 1 | | T | PT12E | 1 | | T |
| 121 | PT7C | 0 | | | PT9B | 1 | | C | PT12D | 1 | | C |
| 122 | PT7A | 0 | | | PT9A | 1 | | T | PT12C | 1 | | T |
| 123 | GND | - | | | GND | - | | | GND | - | | |
| 124 | PT6B | 0 | PCLK0_1*** | C | PT7D | 1 | PCLK1_1*** | | PT10B | 1 | PCLK1_1*** | |
| 125 | PT6A | 0 | | T | PT7B | 1 | | C | PT9D | 1 | | C |
| 126 | PT5C | 0 | | | PT7A | 1 | | T | PT9C | 1 | | T |
| 127 | PT5B | 0 | PCLK0_0*** | | PT6F | 0 | PCLK1_0*** | | PT9B | 1 | PCLK1_0*** | |
| 128 | VCCAUX | - | | | VCCAUX | - | | | VCCAUX | - | | |
| 129 | VCC | - | | | VCC | - | | | VCC | - | | |
| 130 | PT4D | 0 | | | PT5D | 0 | | C | PT7B | 0 | | C |
| 131 | PT4B | 0 | | C | PT5C | 0 | | T | PT7A | 0 | | T |
| 132 | PT4A | 0 | | T | PT5B | 0 | | C | PT6D | 0 | | |
| 133 | PT3F | 0 | | | PT5A | 0 | | T | PT6E | 0 | | T |
| 134 | PT3D | 0 | | | PT4B | 0 | | | PT6F | 0 | | C |
| 135 | VCCIO0 | 0 | | | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 136 | GNDIO0 | 0 | | | GNDIO0 | 0 | | | GNDIO0 | 0 | | |
| 137 | PT3B | 0 | | C | PT3D | 0 | | C | PT4B | 0 | | T |
| 138 | PT2F | 0 | | C | PT3C | 0 | | T | PT4A | 0 | | C |
| 139 | PT3A | 0 | | T | PT3B | 0 | | C | PT3B | 0 | | C |
| 140 | PT2D | 0 | | C | PT3A | 0 | | T | PT3A | 0 | | T |
| 141 | PT2E | 0 | | T | PT2D | 0 | | C | PT2D | 0 | | C |
| 142 | PT2B | 0 | | C | PT2C | 0 | | T | PT2C | 0 | | T |
| 143 | PT2C | 0 | | T | PT2B | 0 | | C | PT2B | 0 | | C |
| 144 | PT2A | 0 | | T | PT2A | 0 | | T | PT2A | 0 | | T |

*Supports true LVDS outputs.
**NC for “E” devices.
***Primary clock inputs arer single-ended.

# LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA

| LCMXO640 | | | | | LCMXO1200 | | | | | LCMXO2280 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Dual Function | Differential | Ball Number | Ball Function | Bank | Dual Function | Differential | Ball Number | Ball Function | Bank | Dual Function | Differential |
| GND | GNDIO3 | 3 | | | GND | GNDIO7 | 7 | | | GND | GNDIO7 | 7 | | |
| VCCIO3 | VCCIO3 | 3 | | | VCCIO7 | VCCIO7 | 7 | | | VCCIO7 | VCCIO7 | 7 | | |
| E4 | NC | | | | E4 | PL2A | 7 | | T | E4 | PL2A | 7 | LUM0_PLLT_FB_A | T |
| E5 | NC | | | | E5 | PL2B | 7 | | C | E5 | PL2B | 7 | LUM0_PLLC_FB_A | C |
| F5 | NC | | | | F5 | PL3A | 7 | | T* | F5 | PL3A | 7 | | T* |
| F6 | NC | | | | F6 | PL3B | 7 | | C* | F6 | PL3B | 7 | | C* |
| F3 | PL3A | 3 | | T | F3 | PL3C | 7 | | T | F3 | PL3C | 7 | LUM0_PLLT_IN_A | T |
| F4 | PL3B | 3 | | C | F4 | PL3D | 7 | | C | F4 | PL3D | 7 | LUM0_PLLC_IN_A | C |
| E3 | PL2C | 3 | | T | E3 | PL4A | 7 | | T* | E3 | PL4A | 7 | | T* |
| E2 | PL2D | 3 | | C | E2 | PL4B | 7 | | C* | E2 | PL4B | 7 | | C* |
| C3 | NC | | | | C3 | PL4C | 7 | | T | C3 | PL4C | 7 | | T |
| C2 | NC | | | | C2 | PL4D | 7 | | C | C2 | PL4D | 7 | | C |
| B1 | PL2A | 3 | | T | B1 | PL5A | 7 | | T* | B1 | PL5A | 7 | | T* |
| C1 | PL2B | 3 | | C | C1 | PL5B | 7 | | C* | C1 | PL5B | 7 | | C* |
| VCCIO3 | VCCIO3 | 3 | | | VCCIO7 | VCCIO7 | 7 | | | VCCIO7 | VCCIO7 | 7 | | |
| GND | GNDIO3 | 3 | | | GND | GNDIO7 | 7 | | | GND | GNDIO7 | 7 | | |
| D2 | PL3C | 3 | | T | D2 | PL5C | 7 | | T | D2 | PL6C | 7 | | T |
| D1 | PL3D | 3 | | C | D1 | PL5D | 7 | | C | D1 | PL6D | 7 | | C |
| F2 | PL5A | 3 | | T | F2 | PL6A | 7 | | T* | F2 | PL7A | 7 | | T* |
| G2 | PL5B | 3 | GSRN | C | G2 | PL6B | 7 | GSRN | C* | G2 | PL7B | 7 | GSRN | C* |
| E1 | PL4A | 3 | | T | E1 | PL6C | 7 | | T | E1 | PL7C | 7 | | T |
| F1 | PL4B | 3 | | C | F1 | PL6D | 7 | | C | F1 | PL7D | 7 | | C |
| G4 | NC | | | | G4 | PL7A | 7 | | T* | G4 | PL8A | 7 | | T* |
| G5 | NC | | | | G5 | PL7B | 7 | | C* | G5 | PL8B | 7 | | C* |
| GND | GND | - | | | GND | GND | - | | | GND | GND | - | | |
| G3 | PL4C | 3 | | T | G3 | PL7C | 7 | | T | G3 | PL8C | 7 | | T |
| H3 | PL4D | 3 | | C | H3 | PL7D | 7 | | C | H3 | PL8D | 7 | | C |
| H4 | NC | | | | H4 | PL8A | 7 | | T* | H4 | PL9A | 7 | | T* |
| H5 | NC | | | | H5 | PL8B | 7 | | C* | H5 | PL9B | 7 | | C* |
| - | - | | | | VCCIO7 | VCCIO7 | 7 | | | VCCIO7 | VCCIO7 | 7 | | |
| - | - | | | | GND | GNDIO7 | 7 | | | GND | GNDIO7 | 7 | | |
| G1 | PL5C | 3 | | T | G1 | PL8C | 7 | | T | G1 | PL10C | 7 | | T |
| H1 | PL5D | 3 | | C | H1 | PL8D | 7 | | C | H1 | PL10D | 7 | | C |
| H2 | PL6A | 3 | | T | H2 | PL9A | 6 | | T* | H2 | PL11A | 6 | | T* |
| J2 | PL6B | 3 | | C | J2 | PL9B | 6 | | C* | J2 | PL11B | 6 | | C* |
| J3 | PL7C | 3 | | T | J3 | PL9C | 6 | | T | J3 | PL11C | 6 | | T |
| K3 | PL7D | 3 | | C | K3 | PL9D | 6 | | C | K3 | PL11D | 6 | | C |
| J1 | PL6C | 3 | | T | J1 | PL10A | 6 | | T* | J1 | PL12A | 6 | | T* |
| - | - | | | | VCCIO6 | VCCIO6 | 6 | | | VCCIO6 | VCCIO6 | 6 | | |
| - | - | | | | GND | GNDIO6 | 6 | | | GND | GNDIO6 | 6 | | |
| K1 | PL6D | 3 | | C | K1 | PL10B | 6 | | C* | K1 | PL12B | 6 | | C* |
| K2 | PL9A | 3 | | T | K2 | PL10C | 6 | | T | K2 | PL12C | 6 | | T |
| L2 | PL9B | 3 | | C | L2 | PL10D | 6 | | C | L2 | PL12D | 6 | | C |
| L1 | PL7A | 3 | | T | L1 | PL11A | 6 | | T* | L1 | PL13A | 6 | | T* |
| M1 | PL7B | 3 | | C | M1 | PL11B | 6 | | C* | M1 | PL13B | 6 | | C* |
| P1 | PL8D | 3 | | C | P1 | PL11D | 6 | | C | P1 | PL14D | 6 | | C |
| N1 | PL8C | 3 | TSALL | T | N1 | PL11C | 6 | TSALL | T | N1 | PL14C | 6 | TSALL | T |
| L3 | PL10A | 3 | | T | L3 | PL12A | 6 | | T* | L3 | PL15A | 6 | | T* |
| M3 | PL10B | 3 | | C | M3 | PL12B | 6 | | C* | M3 | PL15B | 6 | | C* |
| M2 | PL9C | 3 | | T | M2 | PL12C | 6 | | T | M2 | PL15C | 6 | | T |
| N2 | PL9D | 3 | | C | N2 | PL12D | 6 | | C | N2 | PL15D | 6 | | C |
| VCCIO3 | VCCIO3 | 3 | | | VCCIO6 | VCCIO6 | 6 | | | VCCIO6 | VCCIO6 | 6 | | |
| GND | GNDIO3 | 3 | | | GND | GNDIO6 | 6 | | | GND | GNDIO6 | 6 | | |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| GND | GNDIO3 | 3 | | |
| VCCIO3 | VCCIO3 | 3 | | |
| P15 | PR20B | 3 | | C |
| N14 | PR20A | 3 | | T |
| N15 | PR19B | 3 | | C |
| M13 | PR19A | 3 | | T |
| R15 | PR18B | 3 | | C* |
| T16 | PR18A | 3 | | T* |
| N16 | PR17D | 3 | | C |
| M14 | PR17C | 3 | | T |
| U17 | PR17B | 3 | | C* |
| VCC | VCC | - | | |
| U18 | PR17A | 3 | | T* |
| R17 | PR16D | 3 | | C |
| R16 | PR16C | 3 | | T |
| P16 | PR16B | 3 | | C* |
| VCCIO3 | VCCIO3 | 3 | | |
| GND | GNDIO3 | 3 | | |
| P17 | PR16A | 3 | | T* |
| L13 | PR15D | 3 | | C |
| M15 | PR15C | 3 | | T |
| T17 | PR15B | 3 | | C* |
| T18 | PR15A | 3 | | T* |
| L14 | PR14D | 3 | | C |
| L15 | PR14C | 3 | | T |
| R18 | PR14B | 3 | | C* |
| P18 | PR14A | 3 | | T* |
| GND | GND | - | | |
| K15 | PR13D | 3 | | C |
| K13 | PR13C | 3 | | T |
| N17 | PR13B | 3 | | C* |
| N18 | PR13A | 3 | | T* |
| K16 | PR12D | 3 | | C |
| K14 | PR12C | 3 | | T |
| M16 | PR12B | 3 | | C* |
| L16 | PR12A | 3 | | T* |
| GND | GNDIO3 | 3 | | |
| VCCIO3 | VCCIO3 | 3 | | |
| J16 | PR11D | 3 | | C |
| J14 | PR11C | 3 | | T |
| M17 | PR11B | 3 | | C* |
| L17 | PR11A | 3 | | T* |
| J15 | PR10D | 2 | | C |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| E13 | PT16D | 1 | | C |
| C15 | PT16C | 1 | | T |
| F13 | PT16B | 1 | | C |
| D14 | PT16A | 1 | | T |
| A18 | PT15D | 1 | | C |
| B17 | PT15C | 1 | | T |
| A16 | PT15B | 1 | | C |
| A17 | PT15A | 1 | | T |
| VCC | VCC | - | | |
| D13 | PT14D | 1 | | C |
| F12 | PT14C | 1 | | T |
| C14 | PT14B | 1 | | C |
| E12 | PT14A | 1 | | T |
| C13 | PT13D | 1 | | C |
| B16 | PT13C | 1 | | T |
| B15 | PT13B | 1 | | C |
| A15 | PT13A | 1 | | T |
| VCCIO1 | VCCIO1 | 1 | | |
| GND | GNDIO1 | 1 | | |
| B14 | PT12F | 1 | | C |
| A14 | PT12E | 1 | | T |
| D12 | PT12D | 1 | | C |
| F11 | PT12C | 1 | | T |
| B13 | PT12B | 1 | | C |
| A13 | PT12A | 1 | | T |
| C12 | PT11D | 1 | | C |
| GND | GND | - | | |
| B12 | PT11C | 1 | | T |
| E11 | PT11B | 1 | | C |
| D11 | PT11A | 1 | | T |
| C11 | PT10F | 1 | | C |
| A12 | PT10E | 1 | | T |
| VCCIO1 | VCCIO1 | 1 | | |
| GND | GNDIO1 | 1 | | |
| F10 | PT10D | 1 | | C |
| D10 | PT10C | 1 | | T |
| B11 | PT10B | 1 | PCLK1_1*** | C |
| A11 | PT10A | 1 | | T |
| E10 | PT9D | 1 | | C |
| C10 | PT9C | 1 | | T |
| D9 | PT9B | 1 | PCLK1_0*** | C |
| E9 | PT9A | 1 | | T |
| B10 | PT8F | 0 | | C |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| G8 | VCCIO0 | 0 | | |
| G7 | VCCIO0 | 0 | | |

* Supports true LVDS outputs.
** NC for “E” devices.
*** Primary clock inputs are single-ended.

# MachXO Family Data Sheet Ordering Information

June 2013 Data Sheet DS1002

## Part Number Description

LCMXO XXXX X – X XXXXXX X XX

**Device Family**
MachXO PLD

**Logic Capacity**
256 LUTs = 256
640 LUTs = 640
1200 LUTs = 1200
2280 LUTs = 2280

**Supply Voltage**
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked as described.

**Speed**
3 = Slowest
4
5 = Fastest

**Package**
T100 = 100-pin TQFP
T144 = 144-pin TQFP
M100 = 100-ball csBGA
M132 = 132-ball csBGA
B256 = 256-ball caBGA
FT256 = 256-ball ftBGA
FT324 = 324-ball ftBGA

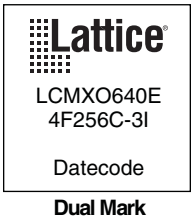
TN100 = 100-pin Lead-Free TQFP
TN144 = 144-pin Lead-Free TQFP
MN100 = 100-ball Lead-Free csBGA
MN132 = 132-ball Lead-Free csBGA
BN256 = 256-ball Lead-Free caBGA
FTN256 = 256-ball Lead-Free ftBGA
FTN324 = 324-ball Lead-Free ftBGA

**Grade**
C = Commercial
I = Industrial

ES = Engineering Sample
Blank = Production Device

## Ordering Information

Note: MachXO devices are dual marked except the slowest commercial speed grade device.þFor example the commercial speed grade LCMXO640E-4F256C is also marked with industrial grade -3I grade.þThe slowest commercial speed grade does not have industrial markings.þ The markings appears as follows:




**Dual Mark**