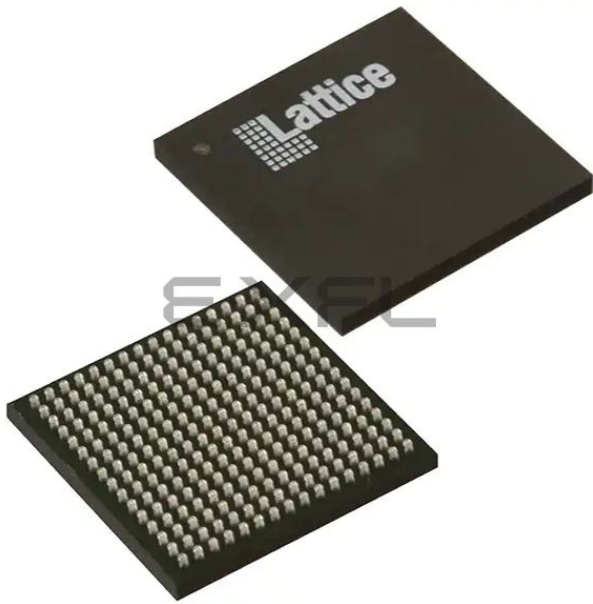




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

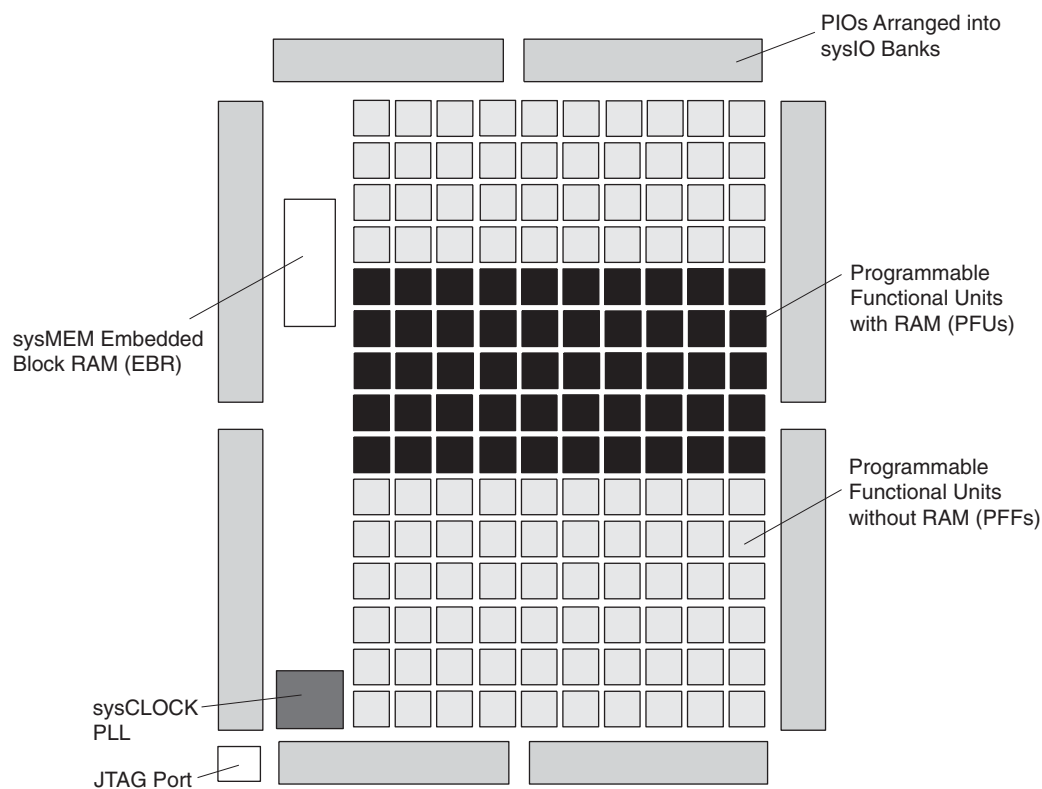
Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	-
Number of I/O	159
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA, CSPBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo640c-3bn256c

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip, high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Popular logic synthesis tools provide synthesis library support for MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Figure 2-1. Top View of the MachXO1200 Device¹



1. Top view of the MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the MachXO640 Device

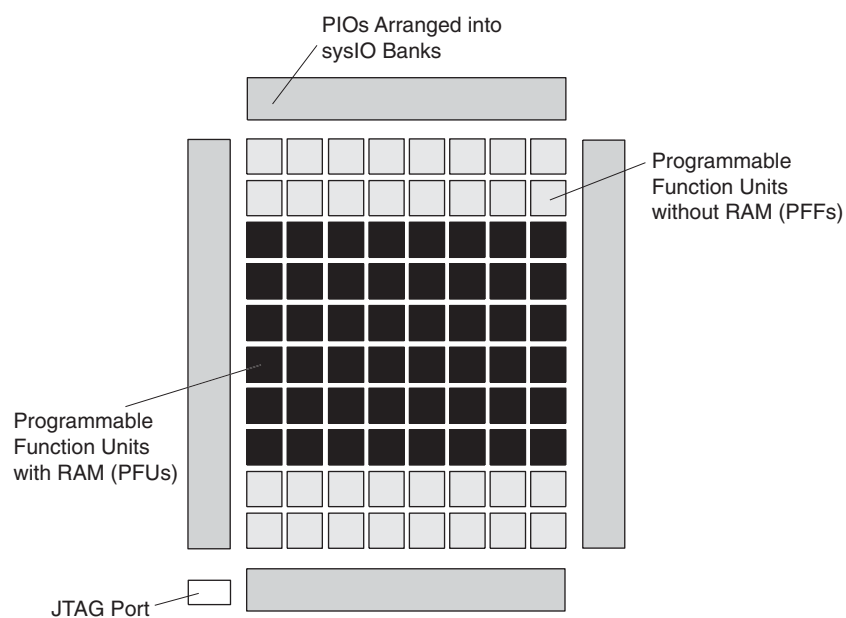
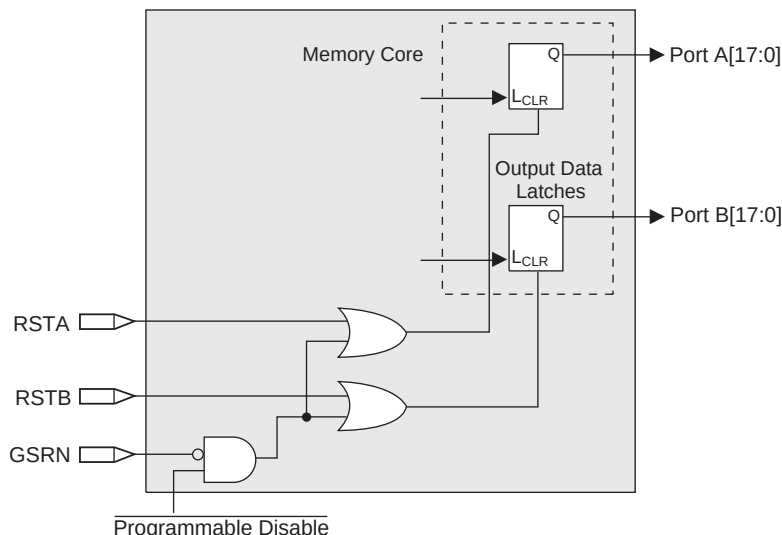


Figure 2-13. Memory Core Reset

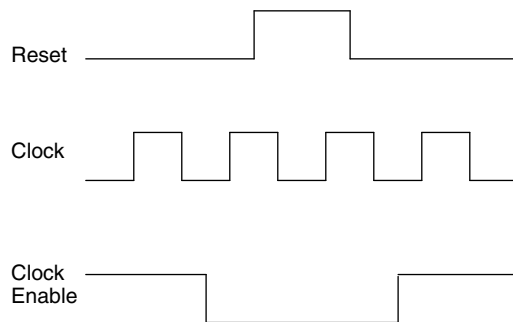


For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPRreset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled

Table 2-10. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Typ.)
Single-ended Interfaces		
LVTTTL	4mA, 8mA, 12mA, 16mA	3.3
LVC MOS33	4mA, 8mA, 12mA, 14mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 14mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 14mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33 ³	N/A	3.3
Differential Interfaces		
LVDS ^{1, 2}	N/A	2.5
BLVDS, RSDS ²	N/A	2.5
LVPECL ²	N/A	3.3

1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

3. Top Banks of MachXO1200 and MachXO2280 devices only.

sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the MachXO1200 and MachXO2280 (two Banks per side). The MachXO640 has four Banks (one Bank per side). The smallest member of this family, the MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V_{CCIO}) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

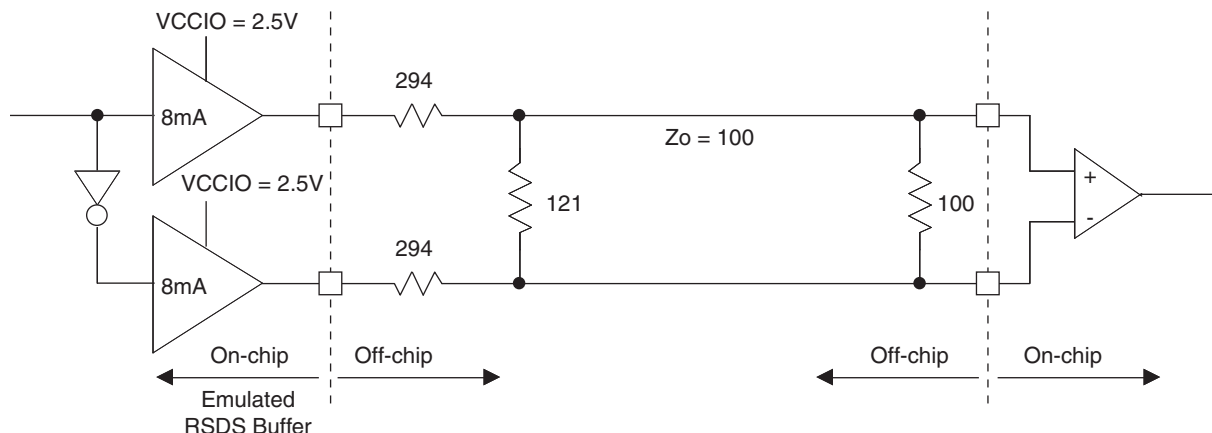


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4 ^{5, 6}	18	25	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f _{VCO}	PLL VCO Frequency		420	840	MHz
f _{PFD}	Phase Detector Input Frequency		25	—	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4 ^{5, 6}	18	25	MHz
AC Characteristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	55	%
t _{PH} ⁴	Output Phase Accuracy		—	0.05	UI
t _{OPJIT} ¹	Output Clock Period Jitter	f _{OUT} >= 100 MHz	—	+/-120	ps
		f _{OUT} < 100 MHz	—	0.02	UIPP
t _{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	1	—	ns
t _{LOCK} ²	PLL Lock-in Time		—	150	μs
t _{PA}	Programmable Delay Unit		100	450	ps
t _{IPJIT}	Input Clock Period Jitter	f _{OUT} ≥ 100 MHz	—	+/-200	ps
		f _{OUT} < 100 MHz	—	0.02	UI
t _{FBKDLY}	External Feedback Delay		—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t _{RST}	RST Pulse Width		10	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output.

5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.

6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.

Rev. A 0.19

LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for "E" devices.

** Primary clock inputs are single-ended.

LCMX0256 and LCMX0640 Logic Signal Connections: 100 csBGA

LCMX0256					LCMX0640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
B1	PL2A	1		T	B1	PL2A	3		T
C1	PL2B	1		C	C1	PL2C	3		T
D2	PL3A	1		T	D2	PL2B	3		C
D1	PL3B	1		C	D1	PL2D	3		C
C2	PL3C	1		T	C2	PL3A	3		T
E1	PL3D	1		C	E1	PL3B	3		C
E2	PL4A	1		T	E2	PL3C	3		T
F1	PL4B	1		C	F1	PL3D	3		C
F2	PL5A	1		T	F2	PL4A	3		
G2	PL5B	1		C	G2	PL4C	3		T
H1	GNDIO1	1			H1	GNDIO3	3		
H2	PL5C	1		T	H2	PL4D	3		C
J1	PL5D	1	GSRN	C	J1	PL5B	3	GSRN	
J2	PL6A	1		T	J2	PL7B	3		
K1	PL6B	1	TSALL	C	K1	PL8C	3	TSALL	T
K2	PL7A	1		T	K2	PL8D	3		C
L1	PL7B	1		C	L1	PL9A	3		
L2	PL7C	1		T	L2	PL9C	3		
M1	PL7D	1		C	M1	PL10A	3		
M2	PL8A	1		T	M2	PL10C	3		
N1	PL8B	1		C	N1	PL11A	3		
M3	PL9A	1		T	M3	PL11C	3		
N2	GNDIO1	1			N2	GNDIO3	3		
P2	TMS	1	TMS		P2	TMS	2	TMS	
P3	PL9B	1		C	P3	PB2C	2		
N4	TCK	1	TCK		N4	TCK	2	TCK	
P4	PB2A	1		T	P4	VCCIO2	2		
N3	PB2B	1		C	N3	GNDIO2	2		
P5	TDO	1	TDO		P5	TDO	2	TDO	
N5	PB2C	1		T	N5	PB4C	2		
P6	TDI	1	TDI		P6	TDI	2	TDI	
N6	PB2D	1		C	N6	PB4E	2		
P7	VCC	-			P7	VCC	-		
N7	PB3A	1	PCLK1_1**	T	N7	PB5B	2	PCLK2_1**	
P8	PB3B	1		C	P8	PB5D	2		
N8	PB3C	1	PCLK1_0**	T	N8	PB6B	2	PCLK2_0**	
P9	PB3D	1		C	P9	PB6C	2		
N10	GNDIO1	1			N10	GNDIO2	2		
P11	PB4A	1		T	P11	PB8B	2		
N11	PB4B	1		C	N11	PB8C	2		T
P12	PB4C	1		T	P12	PB8D	2		C
N12	PB4D	1		C	N12	PB9A	2		

LCMX0256 and LCMX0640 Logic Signal Connections: 100 csBGA (Cont.)

LCMX0256					LCMX0640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
P13	PB5A	1			P13	PB9C	2		T
M12*	SLEEPN	-	SLEEPN		M12*	SLEEPN	-	SLEEPN	
P14	PB5C	1		T	P14	PB9D	2		C
N13	PB5D	1		C	N13	PB9F	2		
N14	PR9B	0		C	N14	PR11D	1		C
M14	PR9A	0		T	M14	PR11B	1		C
L13	PR8B	0		C	L13	PR11C	1		T
L14	PR8A	0		T	L14	PR11A	1		T
M13	PR7D	0		C	M13	PR10D	1		C
K14	PR7C	0		T	K14	PR10C	1		T
K13	PR7B	0		C	K13	PR10B	1		C
J14	PR7A	0		T	J14	PR10A	1		T
J13	PR6B	0		C	J13	PR9D	1		
H13	PR6A	0		T	H13	PR9B	1		
G14	GNDIO0	0			G14	GNDIO1	1		
G13	PR5D	0		C	G13	PR7B	1		
F14	PR5C	0		T	F14	PR6C	1		
F13	PR5B	0		C	F13	PR6B	1		
E14	PR5A	0		T	E14	PR5D	1		
E13	PR4B	0		C	E13	PR5B	1		
D14	PR4A	0		T	D14	PR4D	1		
D13	PR3D	0		C	D13	PR4B	1		
C14	PR3C	0		T	C14	PR3D	1		
C13	PR3B	0		C	C13	PR3B	1		
B14	PR3A	0		T	B14	PR2D	1		
C12	PR2B	0		C	C12	PR2B	1		
B13	GNDIO0	0			B13	GNDIO1	1		
A13	PR2A	0		T	A13	PT9F	0		C
A12	PT5C	0			A12	PT9E	0		T
B11	PT5B	0		C	B11	PT9C	0		
A11	PT5A	0		T	A11	PT9A	0		
B12	PT4F	0		C	B12	VCCIO0	0		
A10	PT4E	0		T	A10	GNDIO0	0		
B10	PT4D	0		C	B10	PT7E	0		
A9	PT4C	0		T	A9	PT7A	0		
A8	PT4B	0	PCLK0_1**	C	A8	PT6B	0	PCLK0_1**	
B8	PT4A	0	PCLK0_0**	T	B8	PT5B	0	PCLK0_0**	C
A7	PT3D	0		C	A7	PT5A	0		T
B7	VCCAUX	-			B7	VCCAUX	-		
A6	PT3C	0		T	A6	PT4F	0		
B6	VCC	-			B6	VCC	-		
A5	PT3B	0		C	A5	PT3F	0		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B1	PL2A	3		T	B1	PL2A	7		T	B1	PL2A	7	LUM0_PLLT_FB_A	T
C1	PL2B	3		C	C1	PL3C	7		T	C1	PL3C	7	LUM0_PLLT_IN_A	T
B2	PL2C	3		T	B2	PL2B	7		C	B2	PL2B	7	LUM0_PLLC_FB_A	C
C2	PL2D	3		C	C2	PL4A	7		T*	C2	PL4A	7		T*
C3	PL3A	3		T	C3	PL3D	7		C	C3	PL3D	7	LUM0_PLLC_IN_A	C
D1	PL3B	3		C	D1	PL4B	7		C*	D1	PL4B	7		C*
D3	PL3D	3			D3	PL4C	7			D3	PL4C	7		
E1	GNDIO3	3			E1	GNDIO7	7			E1	GNDIO7	7		
E2	PL5A	3		T	E2	PL6A	7		T*	E2	PL7A	7		T*
E3	PL5B	3	GSRN	C	E3	PL6B	7	GSRN	C*	E3	PL7B	7	GSRN	C*
F2	PL5D	3			F2	PL6D	7			F2	PL7D	7		
F3	PL6B	3			F3	PL7C	7		T	F3	PL9C	7		T
G1	PL6C	3		T	G1	PL7D	7		C	G1	PL9D	7		C
G2	PL6D	3		C	G2	PL8C	7		T	G2	PL10C	7		T
G3	PL7A	3		T	G3	PL8D	7		C	G3	PL10D	7		C
H2	PL7B	3		C	H2	PL10A	6		T*	H2	PL12A	6		T*
H1	PL7C	3			H1	PL10B	6		C*	H1	PL12B	6		C*
H3	VCC	-			H3	VCC	-			H3	VCC	-		
J1	PL8A	3			J1	PL11B	6			J1	PL14D	6		C
J2	PL8C	3	TSALL		J2	PL11C	6	TSALL	T	J2	PL14C	6	TSALL	T
J3	PL9A	3		T	J3	PL11D	6		C	J3	PL14B	6		
K2	PL9B	3		C	K2	PL12A	6		T*	K2	PL15A	6		T*
K1	PL9C	3			K1	PL12B	6		C*	K1	PL15B	6		C*
L2	GNDIO3	3			L2	GNDIO6	6			L2	GNDIO6	6		
L1	PL10A	3		T	L1	PL14A	6	LLM0_PLLT_FB_A	T*	L1	PL17A	6	LLM0_PLLT_FB_A	T*
L3	PL10B	3		C	L3	PL14B	6	LLM0_PLLC_FB_A	C*	L3	PL17B	6	LLM0_PLLC_FB_A	C*
M1	PL11A	3		T	M1	PL15A	6	LLM0_PLLT_IN_A	T*	M1	PL18A	6	LLM0_PLLT_IN_A	T*
N1	PL11B	3		C	N1	PL16A	6		T	N1	PL19A	6		T
M2	PL11C	3		T	M2	PL15B	6	LLM0_PLLC_IN_A	C*	M2	PL18B	6	LLM0_PLLC_IN_A	C*
P1	PL11D	3		C	P1	PL16B	6		C	P1	PL19B	6		C
P2	GNDIO2	2			P2	GNDIO5	5			P2	GNDIO5	5		
P3	TMS	2	TMS		P3	TMS	5	TMS		P3	TMS	5	TMS	
M3	PB2C	2		T	M3	PB2C	5		T	M3	PB2A	5		T
N3	PB2D	2		C	N3	PB2D	5		C	N3	PB2B	5		C
P4	TCK	2	TCK		P4	TCK	5	TCK		P4	TCK	5	TCK	
M4	PB3B	2			M4	PB3B	5			M4	PB3B	5		
N4	PB3C	2		T	N4	PB4A	5		T	N4	PB4A	5		T
P5	PB3D	2		C	P5	PB4B	5		C	P5	PB4B	5		C
N5	TDO	2	TDO		N5	TDO	5	TDO		N5	TDO	5	TDO	
M5	TDI	2	TDI		M5	TDI	5	TDI		M5	TDI	5	TDI	
N6	PB4E	2		T	N6	PB5C	5			N6	PB6C	5		
P6	VCC	-			P6	VCC	-			P6	VCC	-		
M6	PB4F	2		C	M6	PB6A	5			M6	PB8A	5		
P7	VCCAUX	-			P7	VCCAUX	-			P7	VCCAUX	-		
N7	PB5A	2		T	N7	PB6F	5			N7	PB8F	5		
M7	PB5B	2	PCLK2_1***	C	M7	PB7B	4	PCLK4_1***		M7	PB10F	4	PCLK4_1***	
N8	PB5D	2			N8	PB7C	4		T	N8	PB10C	4		T
P8	PB6A	2		T	P8	PB7D	4		C	P8	PB10D	4		C
M8	PB6B	2	PCLK2_0***	C	M8	PB7F	4	PCLK4_0***		M8	PB10B	4	PCLK4_0***	
N9	PB7A	2		T	N9	PB9A	4		T	N9	PB12A	4		T

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO3	VCCIO3	3			VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
E4	NC				E4	PL2A	7		T	E4	PL2A	7	LUM0_PLLT_FB_A	T
E5	NC				E5	PL2B	7		C	E5	PL2B	7	LUM0_PLLC_FB_A	C
F5	NC				F5	PL3A	7		T*	F5	PL3A	7		T*
F6	NC				F6	PL3B	7		C*	F6	PL3B	7		C*
F3	PL3A	3		T	F3	PL3C	7		T	F3	PL3C	7	LUM0_PLLT_IN_A	T
F4	PL3B	3		C	F4	PL3D	7		C	F4	PL3D	7	LUM0_PLLC_IN_A	C
E3	PL2C	3		T	E3	PL4A	7		T*	E3	PL4A	7		T*
E2	PL2D	3		C	E2	PL4B	7		C*	E2	PL4B	7		C*
C3	NC				C3	PL4C	7		T	C3	PL4C	7		T
C2	NC				C2	PL4D	7		C	C2	PL4D	7		C
B1	PL2A	3		T	B1	PL5A	7		T*	B1	PL5A	7		T*
C1	PL2B	3		C	C1	PL5B	7		C*	C1	PL5B	7		C*
VCCIO3	VCCIO3	3			VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
D2	PL3C	3		T	D2	PL5C	7		T	D2	PL6C	7		T
D1	PL3D	3		C	D1	PL5D	7		C	D1	PL6D	7		C
F2	PL5A	3		T	F2	PL6A	7		T*	F2	PL7A	7		T*
G2	PL5B	3	GSRN	C	G2	PL6B	7	GSRN	C*	G2	PL7B	7	GSRN	C*
E1	PL4A	3		T	E1	PL6C	7		T	E1	PL7C	7		T
F1	PL4B	3		C	F1	PL6D	7		C	F1	PL7D	7		C
G4	NC				G4	PL7A	7		T*	G4	PL8A	7		T*
G5	NC				G5	PL7B	7		C*	G5	PL8B	7		C*
GND	GND	-			GND	GND	-			GND	GND	-		
G3	PL4C	3		T	G3	PL7C	7		T	G3	PL8C	7		T
H3	PL4D	3		C	H3	PL7D	7		C	H3	PL8D	7		C
H4	NC				H4	PL8A	7		T*	H4	PL9A	7		T*
H5	NC				H5	PL8B	7		C*	H5	PL9B	7		C*
-	-				VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
-	-				GND	GNDIO7	7			GND	GNDIO7	7		
G1	PL5C	3		T	G1	PL8C	7		T	G1	PL10C	7		T
H1	PL5D	3		C	H1	PL8D	7		C	H1	PL10D	7		C
H2	PL6A	3		T	H2	PL9A	6		T*	H2	PL11A	6		T*
J2	PL6B	3		C	J2	PL9B	6		C*	J2	PL11B	6		C*
J3	PL7C	3		T	J3	PL9C	6		T	J3	PL11C	6		T
K3	PL7D	3		C	K3	PL9D	6		C	K3	PL11D	6		C
J1	PL6C	3		T	J1	PL10A	6		T*	J1	PL12A	6		T*
-	-				VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
-	-				GND	GNDIO6	6			GND	GNDIO6	6		
K1	PL6D	3		C	K1	PL10B	6		C*	K1	PL12B	6		C*
K2	PL9A	3		T	K2	PL10C	6		T	K2	PL12C	6		T
L2	PL9B	3		C	L2	PL10D	6		C	L2	PL12D	6		C
L1	PL7A	3		T	L1	PL11A	6		T*	L1	PL13A	6		T*
M1	PL7B	3		C	M1	PL11B	6		C*	M1	PL13B	6		C*
P1	PL8D	3		C	P1	PL11D	6		C	P1	PL14D	6		C
N1	PL8C	3	TSALL	T	N1	PL11C	6	TSALL	T	N1	PL14C	6	TSALL	T
L3	PL10A	3		T	L3	PL12A	6		T*	L3	PL15A	6		T*
M3	PL10B	3		C	M3	PL12B	6		C*	M3	PL15B	6		C*
M2	PL9C	3		T	M2	PL12C	6		T	M2	PL15C	6		T
N2	PL9D	3		C	N2	PL12D	6		C	N2	PL15D	6		C
VCCIO3	VCCIO3	3			VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
GND	GNDIO3	3			GND	GNDIO6	6			GND	GNDIO6	6		

LCMXO2280 Logic Signal Connections: 324 ftBGA

LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO7	7		
VCCIO7	VCCIO7	7		
D4	PL2A	7	LUM0_PLLT_FB_A	T
F5	PL2B	7	LUM0_PLLC_FB_A	C
B3	PL3A	7		T*
C3	PL3B	7		C*
E4	PL3C	7	LUM0_PLLT_IN_A	T
G6	PL3D	7	LUM0_PLLC_IN_A	C
A1	PL4A	7		T*
B1	PL4B	7		C*
F4	PL4C	7		T
VCC	VCC	-		
E3	PL4D	7		C
D2	PL5A	7		T*
D3	PL5B	7		C*
G5	PL5C	7		T
F3	PL5D	7		C
C2	PL6A	7		T*
VCCIO7	VCCIO7	7		
GND	GNDIO7	7		
C1	PL6B	7		C*
H5	PL6C	7		T
G4	PL6D	7		C
E2	PL7A	7		T*
D1	PL7B	7	GSRN	C*
J6	PL7C	7		T
H4	PL7D	7		C
F2	PL8A	7		T*
E1	PL8B	7		C*
GND	GND	-		
J3	PL8C	7		T
J5	PL8D	7		C
G3	PL9A	7		T*
H3	PL9B	7		C*
K3	PL9C	7		T
K5	PL9D	7		C
F1	PL10A	7		T*
VCCIO7	VCCIO7	7		
GND	GNDIO7	7		
G1	PL10B	7		C*
K4	PL10C	7		T
K6	PL10D	7		C

LCMX02280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMX02280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G2	PL11A	6		T*
H2	PL11B	6		C*
L3	PL11C	6		T
L5	PL11D	6		C
H1	PL12A	6		T*
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
J2	PL12B	6		C*
L4	PL12C	6		T
L6	PL12D	6		C
K2	PL13A	6		T*
K1	PL13B	6		C*
J1	PL13C	6		T
VCC	VCC	-		
L2	PL13D	6		C
M5	PL14D	6		C
M3	PL14C	6	TSALL	T
L1	PL14B	6		C*
M2	PL14A	6		T*
M1	PL15A	6		T*
N1	PL15B	6		C*
M6	PL15C	6		T
M4	PL15D	6		C
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
P1	PL16A	6		T*
P2	PL16B	6		C*
N3	PL16C	6		T
N4	PL16D	6		C
GND	GND	-		
T1	PL17A	6	LLM0_PLLT_FB_A	T*
R1	PL17B	6	LLM0_PLLC_FB_A	C*
P3	PL17C	6		T
N5	PL17D	6		C
R3	PL18A	6	LLM0_PLLT_IN_A	T*
R2	PL18B	6	LLM0_PLLC_IN_A	C*
P4	PL19A	6		T
N6	PL19B	6		C
U1	PL20A	6		T
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		

LCMX02280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMX02280				
Ball Number	Ball Function	Bank	Dual Function	Differential
T2	PL20B	6		C
P6	TMS	5	TMS	
V1	PB2A	5		T
U2	PB2B	5		C
T3	PB2C	5		T
N7	TCK	5	TCK	
R4	PB2D	5		C
R5	PB3A	5		T
T4	PB3B	5		C
VCC	VCC	-		
R6	PB3C	5		T
P7	PB3D	5		C
U3	PB4A	5		T
T5	PB4B	5		C
V2	PB4C	5		T
N8	TDO	5	TDO	
V3	PB4D	5		C
T6	PB5A	5		T
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		
U4	PB5B	5		C
P8	PB5C	5		T
T7	PB5D	5		C
V4	TDI	5	TDI	
R8	PB6A	5		T
N9	PB6B	5		C
U5	PB6C	5		T
V5	PB6D	5		C
U6	PB7A	5		T
VCC	VCC	-		
V6	PB7B	5		C
P9	PB7C	5		T
T8	PB7D	5		C
U7	PB8A	5		T
V7	PB8B	5		C
M10	VCCAUX	-		
U8	PB8C	5		T
V8	PB8D	5		C
VCCIO5	VCCIO5	5		
GND	GNDIO5	5		
T9	PB8E	5		T
U9	PB8F	5		C
V9	PB9A	4		T

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G8	VCCIO0	0		
G7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100C	1200	1.2V	73	-3	TQFP	100	COM
LCMXO1200E-4T100C	1200	1.2V	73	-4	TQFP	100	COM
LCMXO1200E-5T100C	1200	1.2V	73	-5	TQFP	100	COM
LCMXO1200E-3T144C	1200	1.2V	113	-3	TQFP	144	COM
LCMXO1200E-4T144C	1200	1.2V	113	-4	TQFP	144	COM
LCMXO1200E-5T144C	1200	1.2V	113	-5	TQFP	144	COM
LCMXO1200E-3M132C	1200	1.2V	101	-3	csBGA	132	COM
LCMXO1200E-4M132C	1200	1.2V	101	-4	csBGA	132	COM
LCMXO1200E-5M132C	1200	1.2V	101	-5	csBGA	132	COM
LCMXO1200E-3B256C	1200	1.2V	211	-3	caBGA	256	COM
LCMXO1200E-4B256C	1200	1.2V	211	-4	caBGA	256	COM
LCMXO1200E-5B256C	1200	1.2V	211	-5	caBGA	256	COM
LCMXO1200E-3FT256C	1200	1.2V	211	-3	ftBGA	256	COM
LCMXO1200E-4FT256C	1200	1.2V	211	-4	ftBGA	256	COM
LCMXO1200E-5FT256C	1200	1.2V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100C	2280	1.2V	73	-3	TQFP	100	COM
LCMXO2280E-4T100C	2280	1.2V	73	-4	TQFP	100	COM
LCMXO2280E-5T100C	2280	1.2V	73	-5	TQFP	100	COM
LCMXO2280E-3T144C	2280	1.2V	113	-3	TQFP	144	COM
LCMXO2280E-4T144C	2280	1.2V	113	-4	TQFP	144	COM
LCMXO2280E-5T144C	2280	1.2V	113	-5	TQFP	144	COM
LCMXO2280E-3M132C	2280	1.2V	101	-3	csBGA	132	COM
LCMXO2280E-4M132C	2280	1.2V	101	-4	csBGA	132	COM
LCMXO2280E-5M132C	2280	1.2V	101	-5	csBGA	132	COM
LCMXO2280E-3B256C	2280	1.2V	211	-3	caBGA	256	COM
LCMXO2280E-4B256C	2280	1.2V	211	-4	caBGA	256	COM
LCMXO2280E-5B256C	2280	1.2V	211	-5	caBGA	256	COM
LCMXO2280E-3FT256C	2280	1.2V	211	-3	ftBGA	256	COM
LCMXO2280E-4FT256C	2280	1.2V	211	-4	ftBGA	256	COM
LCMXO2280E-5FT256C	2280	1.2V	211	-5	ftBGA	256	COM
LCMXO2280E-3FT324C	2280	1.2V	271	-3	ftBGA	324	COM
LCMXO2280E-4FT324C	2280	1.2V	271	-4	ftBGA	324	COM
LCMXO2280E-5FT324C	2280	1.2V	271	-5	ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3T100I	256	1.2V	78	-3	TQFP	100	IND
LCMXO256E-4T100I	256	1.2V	78	-4	TQFP	100	IND
LCMXO256E-3M100I	256	1.2V	78	-3	csBGA	100	IND
LCMXO256E-4M100I	256	1.2V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3T100I	640	1.2V	74	-3	TQFP	100	IND
LCMXO640E-4T100I	640	1.2V	74	-4	TQFP	100	IND
LCMXO640E-3M100I	640	1.2V	74	-3	csBGA	100	IND
LCMXO640E-4M100I	640	1.2V	74	-4	csBGA	100	IND
LCMXO640E-3T144I	640	1.2V	113	-3	TQFP	144	IND
LCMXO640E-4T144I	640	1.2V	113	-4	TQFP	144	IND
LCMXO640E-3M132I	640	1.2V	101	-3	csBGA	132	IND
LCMXO640E-4M132I	640	1.2V	101	-4	csBGA	132	IND
LCMXO640E-3B256I	640	1.2V	159	-3	caBGA	256	IND
LCMXO640E-4B256I	640	1.2V	159	-4	caBGA	256	IND
LCMXO640E-3FT256I	640	1.2V	159	-3	ftBGA	256	IND
LCMXO640E-4FT256I	640	1.2V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100I	1200	1.2V	73	-3	TQFP	100	IND
LCMXO1200E-4T100I	1200	1.2V	73	-4	TQFP	100	IND
LCMXO1200E-3T144I	1200	1.2V	113	-3	TQFP	144	IND
LCMXO1200E-4T144I	1200	1.2V	113	-4	TQFP	144	IND
LCMXO1200E-3M132I	1200	1.2V	101	-3	csBGA	132	IND
LCMXO1200E-4M132I	1200	1.2V	101	-4	csBGA	132	IND
LCMXO1200E-3B256I	1200	1.2V	211	-3	caBGA	256	IND
LCMXO1200E-4B256I	1200	1.2V	211	-4	caBGA	256	IND
LCMXO1200E-3FT256I	1200	1.2V	211	-3	ftBGA	256	IND
LCMXO1200E-4FT256I	1200	1.2V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100I	2280	1.2V	73	-3	TQFP	100	IND
LCMXO2280E-4T100I	2280	1.2V	73	-4	TQFP	100	IND
LCMXO2280E-3T144I	2280	1.2V	113	-3	TQFP	144	IND
LCMXO2280E-4T144I	2280	1.2V	113	-4	TQFP	144	IND
LCMXO2280E-3M132I	2280	1.2V	101	-3	csBGA	132	IND
LCMXO2280E-4M132I	2280	1.2V	101	-4	csBGA	132	IND
LCMXO2280E-3B256I	2280	1.2V	211	-3	caBGA	256	IND
LCMXO2280E-4B256I	2280	1.2V	211	-4	caBGA	256	IND
LCMXO2280E-3FT256I	2280	1.2V	211	-3	ftBGA	256	IND
LCMXO2280E-4FT256I	2280	1.2V	211	-4	ftBGA	256	IND
LCMXO2280E-3FT324I	2280	1.2V	271	-3	ftBGA	324	IND
LCMXO2280E-4FT324I	2280	1.2V	271	-4	ftBGA	324	IND

Lead-Free Packaging
Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	COM
LCMXO256C-4TN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	COM
LCMXO256C-5TN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free TQFP	100	COM
LCMXO256C-3MN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	COM
LCMXO256C-4MN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	COM
LCMXO256C-5MN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3TN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	COM
LCMXO640C-4TN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	COM
LCMXO640C-5TN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free TQFP	100	COM
LCMXO640C-3MN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	COM
LCMXO640C-4MN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	COM
LCMXO640C-5MN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free csBGA	100	COM
LCMXO640C-3TN144C	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO640C-4TN144C	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO640C-5TN144C	640	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO640C-3MN132C	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO640C-4MN132C	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO640C-5MN132C	640	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO640C-3BN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	COM
LCMXO640C-4BN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	COM
LCMXO640C-5BN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free caBGA	256	COM
LCMXO640C-3FTN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640C-4FTN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640C-5FTN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3TN100C	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200C-4TN100C	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200C-5TN100C	1200	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200C-3TN144C	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200C-4TN144C	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200C-5TN144C	1200	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200C-3MN132C	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200C-4MN132C	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200C-5MN132C	1200	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200C-3BN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200C-4BN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200C-5BN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200C-3FTN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200C-4FTN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200C-5FTN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-3TN100C	2280	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280C-4TN100C	2280	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280C-5TN100C	2280	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280C-3TN144C	2280	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO2280C-4TN144C	2280	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO2280C-5TN144C	2280	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO2280C-3MN132C	2280	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280C-4MN132C	2280	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280C-5MN132C	2280	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280C-3BN256C	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280C-4BN256C	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280C-5BN256C	2280	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280C-3FTN256C	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280C-4FTN256C	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280C-5FTN256C	2280	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280C-3FTN324C	2280	1.8V/2.5V/3.3V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280C-4FTN324C	2280	1.8V/2.5V/3.3V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280C-5FTN324C	2280	1.8V/2.5V/3.3V	271	-5	Lead-Free ftBGA	324	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3TN100C	256	1.2V	78	-3	Lead-Free TQFP	100	COM
LCMXO256E-4TN100C	256	1.2V	78	-4	Lead-Free TQFP	100	COM
LCMXO256E-5TN100C	256	1.2V	78	-5	Lead-Free TQFP	100	COM
LCMXO256E-3MN100C	256	1.2V	78	-3	Lead-Free csBGA	100	COM
LCMXO256E-4MN100C	256	1.2V	78	-4	Lead-Free csBGA	100	COM
LCMXO256E-5MN100C	256	1.2V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN100C	640	1.2V	74	-3	Lead-Free TQFP	100	COM
LCMXO640E-4TN100C	640	1.2V	74	-4	Lead-Free TQFP	100	COM
LCMXO640E-5TN100C	640	1.2V	74	-5	Lead-Free TQFP	100	COM
LCMXO640E-3MN100C	640	1.2V	74	-3	Lead-Free csBGA	100	COM
LCMXO640E-4MN100C	640	1.2V	74	-4	Lead-Free csBGA	100	COM
LCMXO640E-5MN100C	640	1.2V	74	-5	Lead-Free csBGA	100	COM
LCMXO640E-3TN144C	640	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO640E-4TN144C	640	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO640E-5TN144C	640	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO640E-3MN132C	640	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO640E-4MN132C	640	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO640E-5MN132C	640	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO640E-3BN256C	640	1.2V	159	-3	Lead-Free caBGA	256	COM
LCMXO640E-4BN256C	640	1.2V	159	-4	Lead-Free caBGA	256	COM
LCMXO640E-5BN256C	640	1.2V	159	-5	Lead-Free caBGA	256	COM
LCMXO640E-3FTN256C	640	1.2V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640E-4FTN256C	640	1.2V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640E-5FTN256C	640	1.2V	159	-5	Lead-Free ftBGA	256	COM

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
October 2005	01.1	Introduction	Distributed RAM information in family table updated. Added footnote 1 - fpBGA packaging to the family selection guide.
		Architecture	sysIO Buffer section updated.
			Hot Socketing section updated.
			Sleep Mode section updated.
			SLEEP Pin Characteristics section updated.
			Oscillator section updated.
			Security section updated.
		DC and Switching Characteristics	Recommended Operating Conditions table updated.
			DC Electrical Characteristics table updated.
			Supply Current (Sleep Mode) table added with LCMXO256/640 data.
			Supply Current (Standby) table updated with LCMXO256/640 data.
			Initialization Supply Current table updated with LCMXO256/640 data.
			Programming and Erase Flash Supply Current table updated with LCMXO256/640 data.
			Register-to-Register Performance table updated (rev. A 0.16).
			External Switching Characteristics table updated (rev. A 0.16).
			Internal Timing Parameter table updated (rev. A 0.16).
			Family Timing Adders updated (rev. A 0.16).
			sysCLOCK Timing updated (rev. A 0.16).
			MachXO "C" Sleep Mode Timing updated (A 0.16).
			JTAG Port Timing Specification updated (rev. A 0.16).
		Pinout Information	SLEEPIN description updated.
			Pin Information Summary updated.
			Power Supply and NC Connection table has been updated.
			Logic Signal Connection section has been updated to include all devices/packages.
		Ordering Information	Part Number Description section has been updated.
			Ordering Part Number section has been updated (added LCMXO256C/LCMXO640C "4W").
		Supplemental Information	MachXO Density Migration Technical Note (TN1097) added.
November 2005	01.2	Pinout Information	Added "Power Supply and NC Connections" summary information for LCMXO1200 and LCMXO2280 in 100 TQFP package.
December 2005	01.3	DC and Switching Characteristics	Supply Current (Standby) table updated with LCMXO1200/2280 data.
		Ordering Information	Ordering Part Number section updated (added LCMXO2280C "4W").
April 2006	02.0	Introduction	Introduction paragraphs updated.
		Architecture	Architecture Overview paragraphs updated.