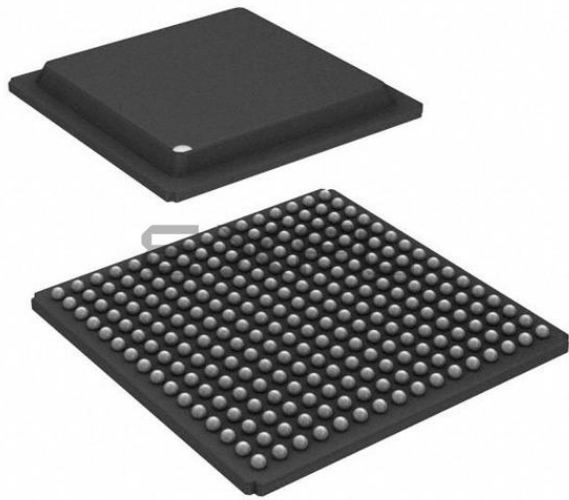




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

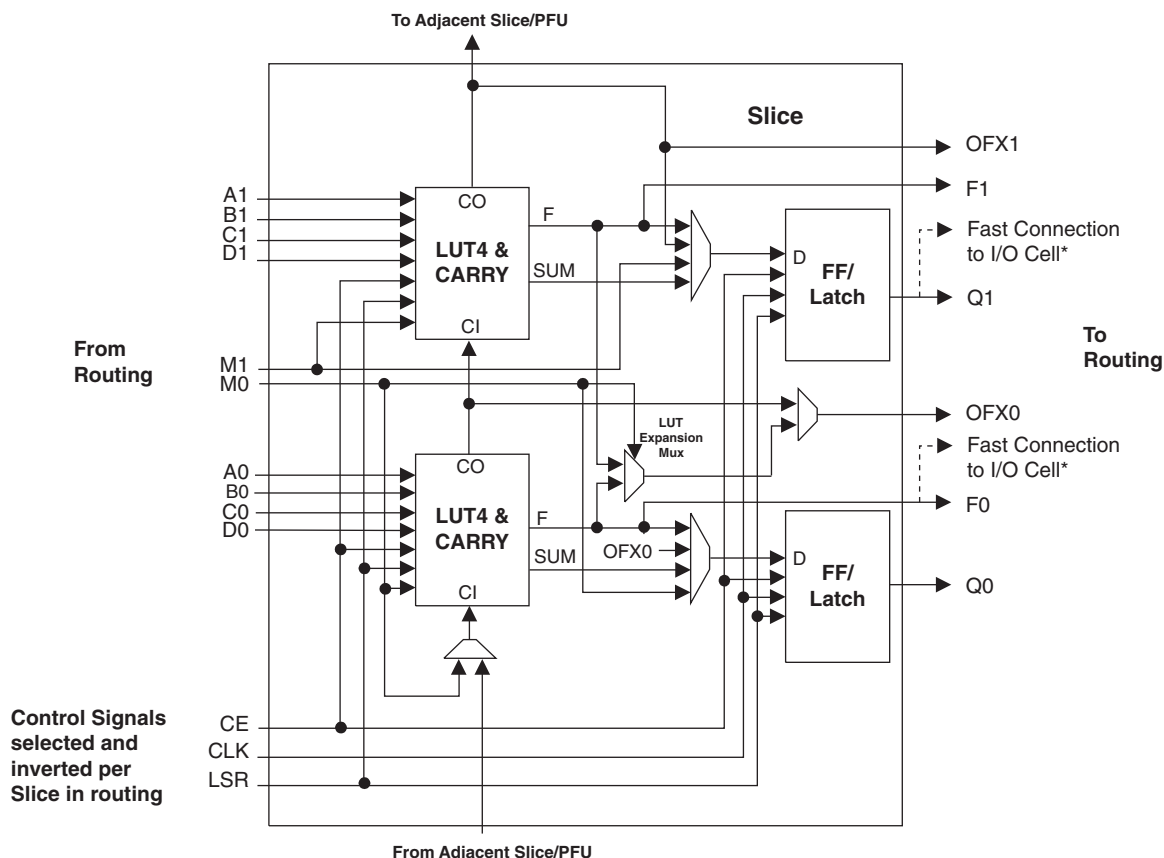
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	-
Number of I/O	159
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo640c-3ftn256c

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip, high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Popular logic synthesis tools provide synthesis library support for MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2-1 lists the signals associated with each Slice.

Figure 2-5. Slice Diagram



Notes:

Some inter-Slice signals are not shown.

* Only PFUs at the edges have fast connections to the I/O cell.

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the Slice
Output	Inter-PFU signal	FCO	Fast Carry Out ¹

1. See Figure 2-4 for connection details.

2. Requires two PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices

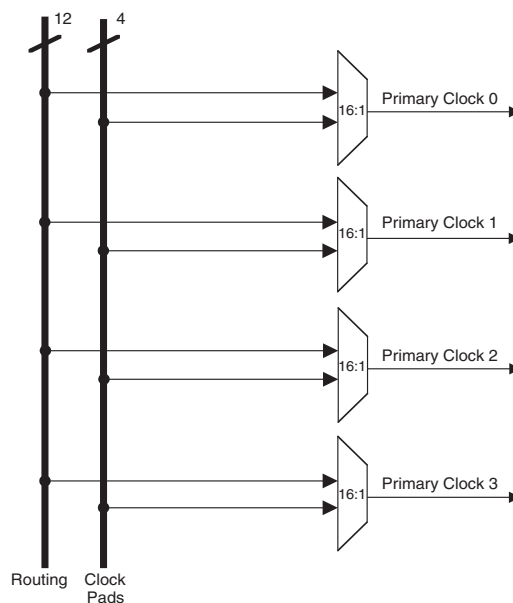
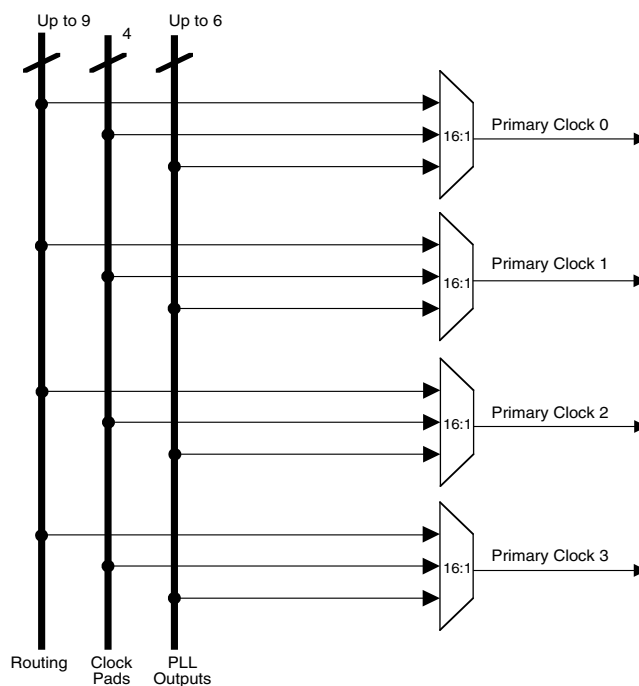


Figure 2-8. Primary Clocks for MachXO1200 and MachXO2280 Devices



Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 2-9. Secondary Clocks for MachXO Devices

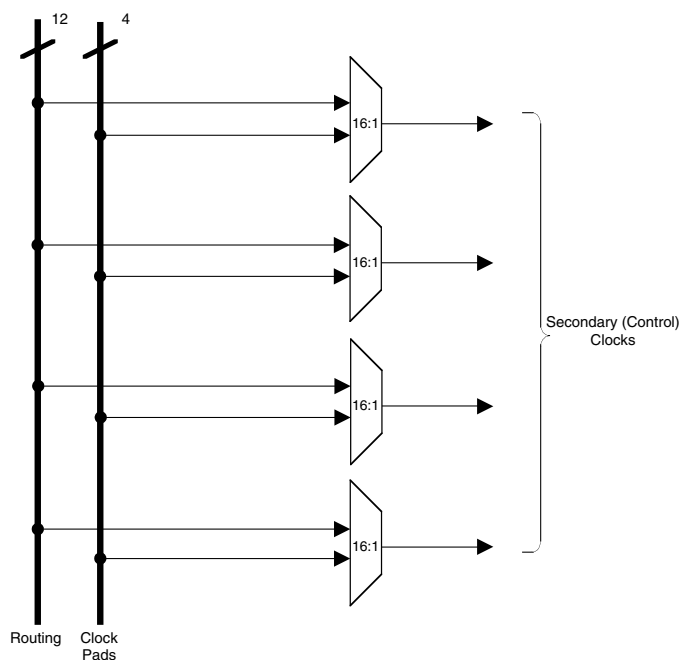


Table 2-8. I/O Support Device by Device

	MachXO256	MachXO640	MachXO1200	MachXO2280
Number of I/O Banks	2	4	8	8
Type of Input Buffers	Single-ended (all I/O Banks)	Single-ended (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)
Differential Output Emulation Capability	All I/O Banks	All I/O Banks	All I/O Banks	All I/O Banks
PCI Support	No	No	Top side only	Top side only

Table 2-9. Supported Input Standards

Input Standard	VCCIO (Typ.)				
	3.3V	2.5V	1.8V	1.5V	1.2V
Single Ended Interfaces					
LVTTL	Yes	Yes	Yes	Yes	Yes
LVC MOS33	Yes	Yes	Yes	Yes	Yes
LVC MOS25	Yes	Yes	Yes	Yes	Yes
LVC MOS18			Yes		
LVC MOS15				Yes	
LVC MOS12	Yes	Yes	Yes	Yes	Yes
PCI ¹	Yes				
Differential Interfaces					
BLVDS ² , LVDS ² , LVPECL ² , RSDS ²	Yes	Yes	Yes	Yes	Yes

1. Top Banks of MachXO1200 and MachXO2280 devices only.

2. MachXO1200 and MachXO2280 devices only.

Table 2-10. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Typ.)
Single-ended Interfaces		
LVTTTL	4mA, 8mA, 12mA, 16mA	3.3
LVC MOS33	4mA, 8mA, 12mA, 14mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 14mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 14mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33 ³	N/A	3.3
Differential Interfaces		
LVDS ^{1, 2}	N/A	2.5
BLVDS, RSDS ²	N/A	2.5
LVPECL ²	N/A	3.3

1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

3. Top Banks of MachXO1200 and MachXO2280 devices only.

sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the MachXO1200 and MachXO2280 (two Banks per side). The MachXO640 has four Banks (one Bank per side). The smallest member of this family, the MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V_{CCIO}) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The MachXO “C” devices ($V_{CC} = 1.8/2.5/3.3V$) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

Table 2-11. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <10mA	0	Typical <100uA
I/O Leakage	<10μA	<1mA	<10μA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

Configuration and Testing

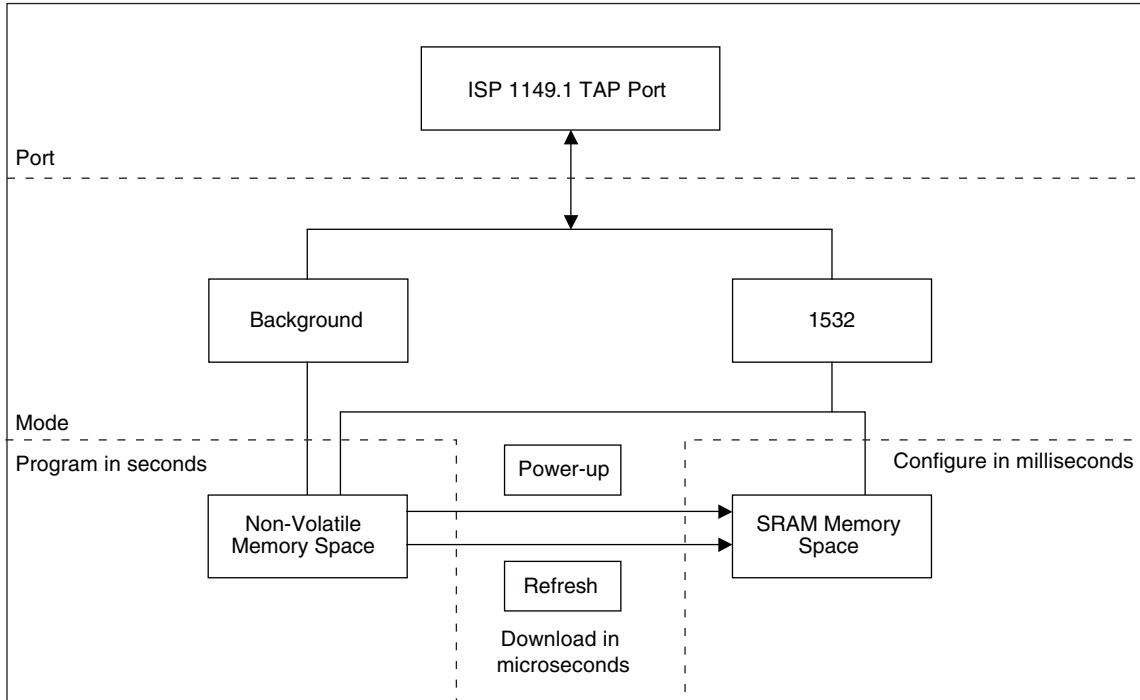
The following section describes the configuration and testing features of the MachXO family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1} ; MachXO640: V_{CCIO2} ; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

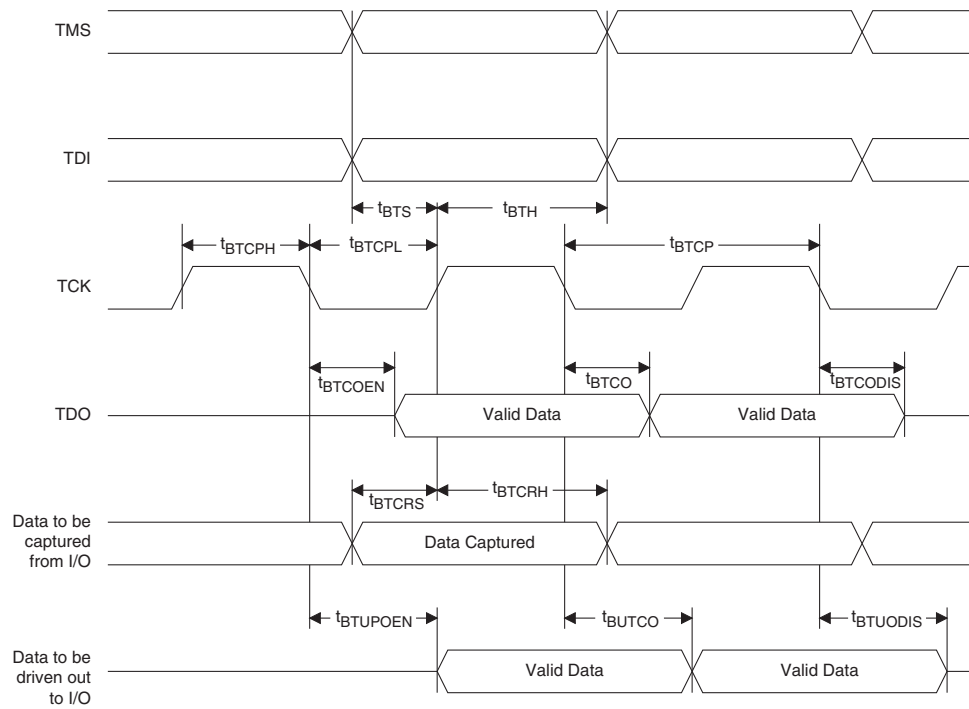
Figure 2-22. MachXO Configuration and Programming



Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Figure 3-5. JTAG Port Timing Waveforms



Switching Test Conditions

Figure 3-6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-6. Output Test Load, LVTTTL and LVCMOS Standards

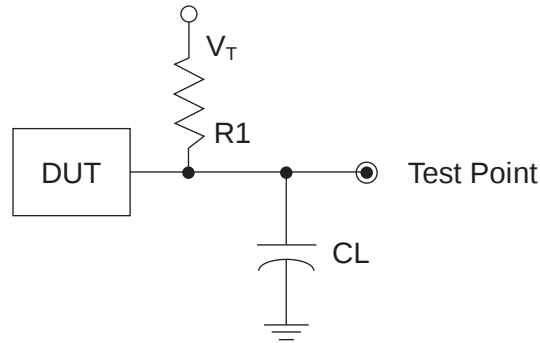


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTTL, LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V_{OL}
LVTTTL and LVCMOS 3.3 (Z -> L)				V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTTL + LVCMOS (H -> Z)			$V_{OH} - 0.15$	V_{OL}
LVTTTL + LVCMOS (L -> Z)			$V_{OL} - 0.15$	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LCMX0256 and LCMX0640 Logic Signal Connections: 100 TQFP

Pin Number	LCMX0256				LCMX0640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	1		T	PL2A	3		T
2	PL2B	1		C	PL2C	3		T
3	PL3A	1		T	PL2B	3		C
4	PL3B	1		C	PL2D	3		C
5	PL3C	1		T	PL3A	3		T
6	PL3D	1		C	PL3B	3		C
7	PL4A	1		T	PL3C	3		T
8	PL4B	1		C	PL3D	3		C
9	PL5A	1		T	PL4A	3		
10	VCCIO1	1			VCCIO3	3		
11	PL5B	1		C	PL4C	3		T
12	GNDIO1	1			GNDIO3	3		
13	PL5C	1		T	PL4D	3		C
14	PL5D	1	GSRN	C	PL5B	3	GSRN	
15	PL6A	1		T	PL7B	3		
16	PL6B	1	TSALL	C	PL8C	3	TSALL	T
17	PL7A	1		T	PL8D	3		C
18	PL7B	1		C	PL9A	3		
19	PL7C	1		T	PL9C	3		
20	PL7D	1		C	PL10A	3		
21	PL8A	1		T	PL10C	3		
22	PL8B	1		C	PL11A	3		
23	PL9A	1		T	PL11C	3		
24	VCCIO1	1			VCCIO3	3		
25	GNDIO1	1			GNDIO3	3		
26	TMS	1	TMS		TMS	2	TMS	
27	PL9B	1		C	PB2C	2		
28	TCK	1	TCK		TCK	2	TCK	
29	PB2A	1		T	VCCIO2	2		
30	PB2B	1		C	GNDIO2	2		
31	TDO	1	TDO		TDO	2	TDO	
32	PB2C	1		T	PB4C	2		
33	TDI	1	TDI		TDI	2	TDI	
34	PB2D	1		C	PB4E	2		
35	VCC	-			VCC	-		
36	PB3A	1	PCLK1_1**	T	PB5B	2	PCLK2_1**	
37	PB3B	1		C	PB5D	2		
38	PB3C	1	PCLK1_0**	T	PB6B	2	PCLK2_0**	
39	PB3D	1		C	PB6C	2		
40	GND	-			GND	-		
41	VCCIO1	1			VCCIO2	2		
42	GNDIO1	1			GNDIO2	2		

LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for "E" devices.

** Primary clock inputs are single-ended.

LCMX0256 and LCMX0640 Logic Signal Connections: 100 csBGA (Cont.)

LCMX0256					LCMX0640				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
A4	GNDIO0	0			A4	GNDIO0	0		
B4	PT3A	0		T	B4	PT3B	0		C
A3	PT2F	0		C	A3	PT3A	0		T
B3	PT2E	0		T	B3	PT2F	0		C
A2	PT2D	0		C	A2	PT2E	0		T
C3	PT2C	0		T	C3	PT2B	0		C
A1	PT2B	0		C	A1	PT2C	0		
B2	PT2A	0		T	B2	PT2A	0		T
N9	GND	-			N9	GND	-		
B9	GND	-			B9	GND	-		
B5	VCCIO0	0			B5	VCCIO0	0		
A14	VCCIO0	0			A14	VCCIO1	1		
H14	VCCIO0	0			H14	VCCIO1	1		
P10	VCCIO1	1			P10	VCCIO2	2		
G1	VCCIO1	1			G1	VCCIO3	3		
P1	VCCIO1	1			P1	VCCIO3	3		

*NC for "E" devices.

**Primary clock inputs are single-ended.

LCMX0640, LCMX01200 and LCMX02280 Logic Signal Connections: 132 csBGA (Cont.)

LCMX0640					LCMX01200					LCMX02280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
M9	PB7B	2		C	M9	PB9B	4		C	M9	PB12B	4		C
N10	PB7E	2		T	N10	PB9C	4		T	N10	PB12C	4		T
P10	PB7F	2		C	P10	PB9D	4		C	P10	PB12D	4		C
N11	GNDIO2	2			N11	GNDIO4	4			N11	GNDIO4	4		
P11	PB8C	2		T	P11	PB10A	4		T	P11	PB13C	4		T
M11	PB8D	2		C	M11	PB10B	4		C	M11	PB13D	4		C
P12	PB9C	2		T	P12	PB10C	4			P12	PB15B	4		
P13	PB9D	2		C	P13	PB11C	4		T	P13	PB16C	4		T
N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB11D	4		C	P14	PB16D	4		C
N14	PR11D	1		C	N14	PR16B	3		C	N14	PR19B	3		C
M14	PR11C	1		T	M14	PR15B	3		C*	M14	PR18B	3		C*
N13	PR11B	1		C	N13	PR16A	3		T	N13	PR19A	3		T
M12	PR11A	1		T	M12	PR15A	3		T*	M12	PR18A	3		T*
M13	PR10B	1		C	M13	PR14B	3		C*	M13	PR17B	3		C*
L14	PR10A	1		T	L14	PR14A	3		T*	L14	PR17A	3		T*
L13	GNDIO1	1			L13	GNDIO3	3			L13	GNDIO3	3		
K14	PR8D	1		C	K14	PR12B	3		C*	K14	PR15B	3		C*
K13	PR8C	1		T	K13	PR12A	3		T*	K13	PR15A	3		T*
K12	PR8B	1		C	K12	PR11B	3		C*	K12	PR14B	3		C*
J13	PR8A	1		T	J13	PR11A	3		T*	J13	PR14A	3		T*
J12	PR7C	1			J12	PR10B	3		C*	J12	PR13B	3		C*
H14	PR7B	1		C	H14	PR10A	3		T*	H14	PR13A	3		T*
H13	PR7A	1		T	H13	PR9B	3		C*	H13	PR11B	3		C*
H12	PR6D	1		C	H12	PR9A	3		T*	H12	PR11A	3		T*
G13	PR6C	1		T	G13	PR8B	2		C*	G13	PR10B	2		C*
G14	PR6B	1			G14	PR8A	2		T*	G14	PR10A	2		T*
G12	VCC	-			G12	VCC	-			G12	VCC	-		
F14	PR5D	1		C	F14	PR6C	2			F14	PR8C	2		
F13	PR5C	1		T	F13	PR6B	2		C*	F13	PR8B	2		C*
F12	PR4D	1		C	F12	PR6A	2		T*	F12	PR8A	2		T*
E13	PR4C	1		T	E13	PR5B	2		C*	E13	PR7B	2		C*
E14	PR4B	1			E14	PR5A	2		T*	E14	PR7A	2		T*
D13	GNDIO1	1			D13	GNDIO2	2			D13	GNDIO2	2		
D14	PR3D	1		C	D14	PR4B	2		C*	D14	PR5B	2		C*
D12	PR3C	1		T	D12	PR4A	2		T*	D12	PR5A	2		T*
C14	PR2D	1		C	C14	PR3D	2		C	C14	PR4D	2		C
B14	PR2C	1		T	B14	PR2B	2		C	B14	PR3B	2		C*
C13	PR2B	1		C	C13	PR3C	2		T	C13	PR4C	2		T
A14	PR2A	1		T	A14	PR2A	2		T	A14	PR3A	2		T*
A13	PT9F	0		C	A13	PT11D	1		C	A13	PT16D	1		C
A12	PT9E	0		T	A12	PT11B	1		C	A12	PT16B	1		C
B13	PT9D	0		C	B13	PT11C	1		T	B13	PT16C	1		T
B12	PT9C	0		T	B12	PT10F	1			B12	PT15D	1		
C12	PT9B	0		C	C12	PT11A	1		T	C12	PT16A	1		T
A11	PT9A	0		T	A11	PT10D	1		C	A11	PT14B	1		C
C11	PT8C	0			C11	PT10C	1		T	C11	PT14A	1		T
A10	GNDIO0	0			A10	GNDIO1	1			A10	GNDIO1	1		
B10	PT7F	0		C	B10	PT9F	1		C	B10	PT12F	1		C
C10	PT7E	0		T	C10	PT9E	1		T	C10	PT12E	1		T

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1***	C	A8	PT7D	1	PCLK1_1***		A8	PT10B	1	PCLK1_1***	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0***	C	C8	PT6F	0	PCLK1_0***		C8	PT9B	1	PCLK1_0***	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	-			A7	VCCAUX	-			A7	VCCAUX	-		
C7	VCC	-			C7	VCC	-			C7	VCC	-		
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	-			F1	GND	-			F1	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
C9	GND	-			C9	GND	-			C9	GND	-		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T
A3	PT2B	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2A	0		T	A2	PT3A	0		T	A2	PT3A	0		T
B3	NC				B3	PT2B	0		C	B3	PT2D	0		C
B2	NC				B2	PT2A	0		T	B2	PT2C	0		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A16	GND	-			A16	GND	-			A16	GND	-		
F11	GND	-			F11	GND	-			F11	GND	-		
G8	GND	-			G8	GND	-			G8	GND	-		
G9	GND	-			G9	GND	-			G9	GND	-		
H7	GND	-			H7	GND	-			H7	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
H9	GND	-			H9	GND	-			H9	GND	-		
H10	GND	-			H10	GND	-			H10	GND	-		
J7	GND	-			J7	GND	-			J7	GND	-		
J8	GND	-			J8	GND	-			J8	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
K8	GND	-			K8	GND	-			K8	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L6	GND	-			L6	GND	-			L6	GND	-		
T1	GND	-			T1	GND	-			T1	GND	-		
T16	GND	-			T16	GND	-			T16	GND	-		
G7	VCC	-			G7	VCC	-			G7	VCC	-		
G10	VCC	-			G10	VCC	-			G10	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
K10	VCC	-			K10	VCC	-			K10	VCC	-		
H6	VCCIO3	3			H6	VCCIO7	7			H6	VCCIO7	7		
G6	VCCIO3	3			G6	VCCIO7	7			G6	VCCIO7	7		
K6	VCCIO3	3			K6	VCCIO6	6			K6	VCCIO6	6		
J6	VCCIO3	3			J6	VCCIO6	6			J6	VCCIO6	6		
L8	VCCIO2	2			L8	VCCIO5	5			L8	VCCIO5	5		
L7	VCCIO2	2			L7	VCCIO5	5			L7	VCCIO5	5		
L9	VCCIO2	2			L9	VCCIO4	4			L9	VCCIO4	4		
L10	VCCIO2	2			L10	VCCIO4	4			L10	VCCIO4	4		
K11	VCCIO1	1			K11	VCCIO3	3			K11	VCCIO3	3		
J11	VCCIO1	1			J11	VCCIO3	3			J11	VCCIO3	3		
H11	VCCIO1	1			H11	VCCIO2	2			H11	VCCIO2	2		
G11	VCCIO1	1			G11	VCCIO2	2			G11	VCCIO2	2		
F9	VCCIO0	0			F9	VCCIO1	1			F9	VCCIO1	1		
F10	VCCIO0	0			F10	VCCIO1	1			F10	VCCIO1	1		
F8	VCCIO0	0			F8	VCCIO0	0			F8	VCCIO0	0		
F7	VCCIO0	0			F7	VCCIO0	0			F7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR10C	2		T
M18	PR10B	2		C*
L18	PR10A	2		T*
GND	GNDIO2	2		
VCCIO2	VCCIO2	2		
H16	PR9D	2		C
H14	PR9C	2		T
K18	PR9B	2		C*
J18	PR9A	2		T*
J17	PR8D	2		C
VCC	VCC	-		
H18	PR8C	2		T
H17	PR8B	2		C*
G17	PR8A	2		T*
H13	PR7D	2		C
H15	PR7C	2		T
G18	PR7B	2		C*
F18	PR7A	2		T*
G14	PR6D	2		C
G16	PR6C	2		T
VCCIO2	VCCIO2	2		
GND	GNDIO2	2		
E18	PR6B	2		C*
F17	PR6A	2		T*
G13	PR5D	2		C
G15	PR5C	2		T
E17	PR5B	2		C*
E16	PR5A	2		T*
GND	GND	-		
F15	PR4D	2		C
E15	PR4C	2		T
D17	PR4B	2		C*
D18	PR4A	2		T*
B18	PR3D	2		C
C18	PR3C	2		T
C16	PR3B	2		C*
D16	PR3A	2		T*
C17	PR2B	2		C
D15	PR2A	2		T
VCCIO2	VCCIO2	2		
GND	GNDIO2	2		
GND	GNDIO1	1		
VCCIO1	VCCIO1	1		

LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G8	VCCIO0	0		
G7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100C	1200	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200E-4TN100C	1200	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200E-5TN100C	1200	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200E-3TN144C	1200	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200E-4TN144C	1200	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200E-5TN144C	1200	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200E-3MN132C	1200	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200E-4MN132C	1200	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200E-5MN132C	1200	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200E-3BN256C	1200	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200E-4BN256C	1200	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200E-5BN256C	1200	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200E-3FTN256C	1200	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200E-4FTN256C	1200	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200E-5FTN256C	1200	1.2V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100C	2280	1.2V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280E-4TN100C	2280	1.2V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280E-5TN100C	2280	1.2V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280E-3TN144C	2280	1.2V	113	-3	Lead-Free TQFP	144	COM
LCMXO2280E-4TN144C	2280	1.2V	113	-4	Lead-Free TQFP	144	COM
LCMXO2280E-5TN144C	2280	1.2V	113	-5	Lead-Free TQFP	144	COM
LCMXO2280E-3MN132C	2280	1.2V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280E-4MN132C	2280	1.2V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280E-5MN132C	2280	1.2V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280E-3BN256C	2280	1.2V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280E-4BN256C	2280	1.2V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280E-5BN256C	2280	1.2V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280E-3FTN256C	2280	1.2V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280E-4FTN256C	2280	1.2V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280E-5FTN256C	2280	1.2V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280E-3FTN324C	2280	1.2V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280E-4FTN324C	2280	1.2V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280E-5FTN324C	2280	1.2V	271	-5	Lead-Free ftBGA	324	COM

Lead-Free Packaging
Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100I	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	IND
LCMXO256C-4TN100I	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	IND
LCMXO256C-3MN100I	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	IND
LCMXO256C-4MN100I	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3TN100I	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	IND
LCMXO640C-4TN100I	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	IND
LCMXO640C-3MN100I	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	IND
LCMXO640C-4MN100I	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	IND
LCMXO640C-3TN144I	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	IND
LCMXO640C-4TN144I	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	IND
LCMXO640C-3MN132I	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	IND
LCMXO640C-4MN132I	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	IND
LCMXO640C-3BN256I	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	IND
LCMXO640C-4BN256I	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	IND
LCMXO640C-3FTN256I	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640C-4FTN256I	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3TN100I	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200C-4TN100I	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200C-3TN144I	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200C-4TN144I	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200C-3MN132I	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200C-4MN132I	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200C-3BN256I	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200C-4BN256I	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200C-3FTN256I	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200C-4FTN256I	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-3TN100I	2280	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280C-4TN100I	2280	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280C-3TN144I	2280	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280C-4TN144I	2280	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280C-3MN132I	2280	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280C-4MN132I	2280	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280C-3BN256I	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280C-4BN256I	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280C-3FTN256I	2280	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280C-4FTN256I	2280	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280C-3FTN324I	2280	1.8V/2.5V/3.3V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280C-4FTN324I	2280	1.8V/2.5V/3.3V	271	-4	Lead-Free ftBGA	324	IND