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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	-
Number of I/O	159
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo640c-3ftn256i

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.
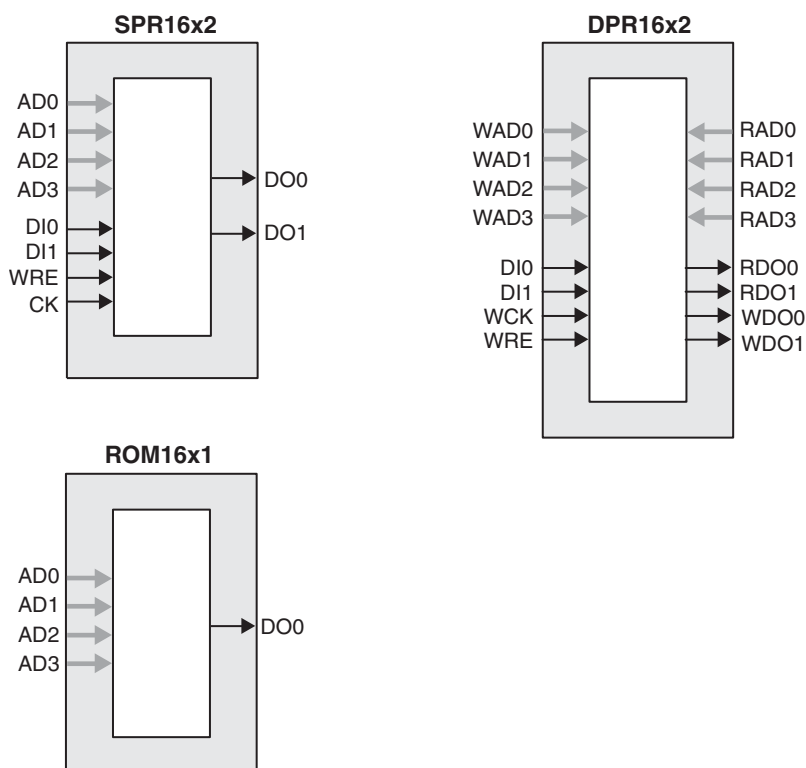
The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-6. Distributed Memory Primitives

SPR16x2

AD0
AD1
AD2
AD3
DI0
DI1
WRE
CK

DO0
DO1

DPR16x2

WAD0
WAD1
WAD2
WAD3
DI0
DI1
WCK
WRE

RAD0
RAD1
RAD2
RAD3
RDO0
RDO1
WDO0
WDO1

ROM16x1

AD0
AD1
AD2
AD3

DO0

ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation
Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

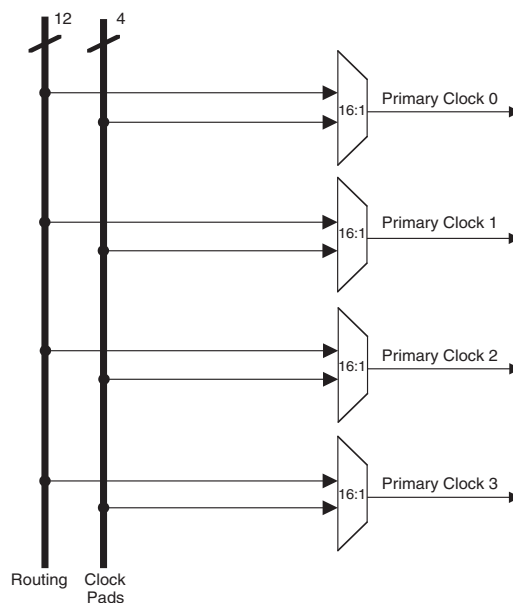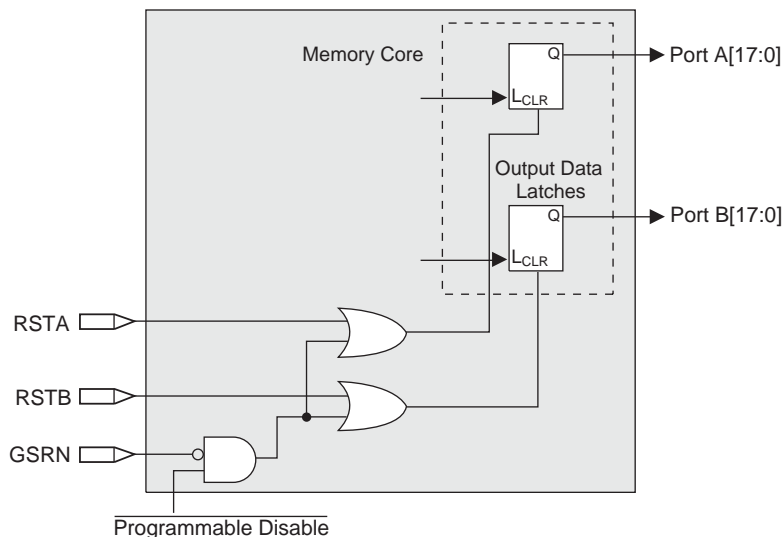*Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices*

Figure 2-13. Memory Core Reset

For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram
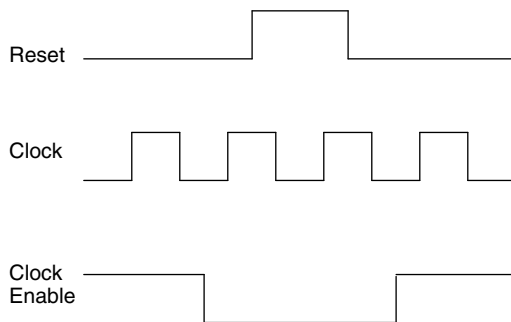
If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPReset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs.
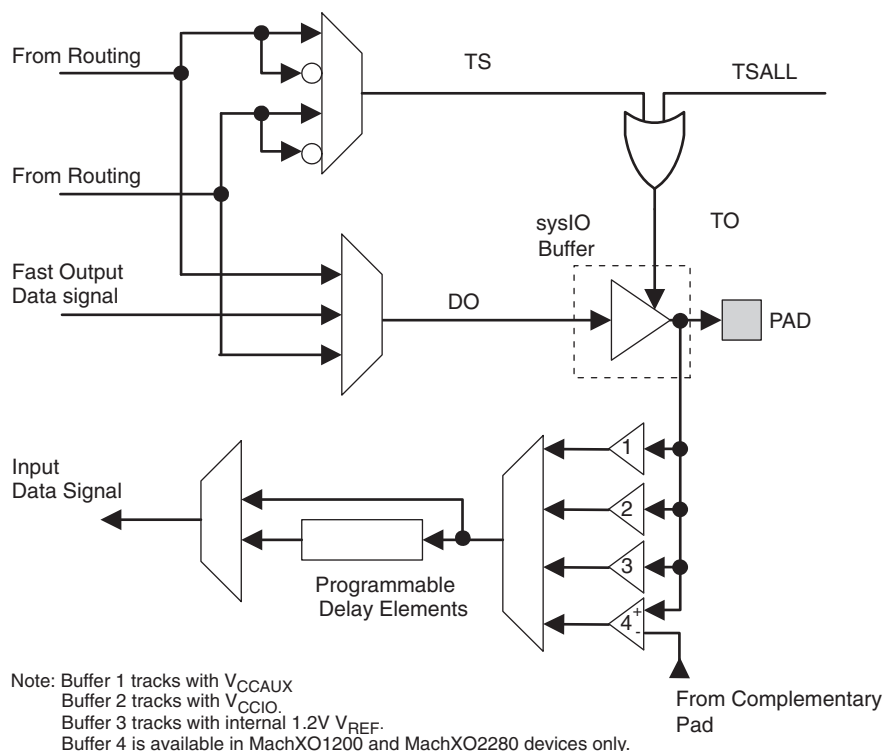
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled

output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 2-17 shows the MachXO PIO logic.

The tristate control signal is multiplexed from the output data signals and their complements. In addition a global signal (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the device. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

Figure 2-17. MachXO PIO Block Diagram

Note: Buffer 1 tracks with V_{CCAUX}
Buffer 2 tracks with V_{CCIO}.
Buffer 3 tracks with internal 1.2V V_{REF}.
Buffer 4 is available in MachXO1200 and MachXO2280 devices only.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the MachXO devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. In addition to the Bank V_{CCIO} supplies, the MachXO devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

MachXO256 and MachXO640 devices contain single-ended input buffers and single-ended output buffers with complementary outputs on all the I/O Banks.

MachXO1200 and MachXO2280 devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the top and bottom Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom

of the devices also support differential input buffers. PCI clamps are available on the top Bank I/O buffers. The PCI clamp is enabled after V_{CC}, V_{CCAUX}, and V_{CCIO} are at valid operating levels and the device has been configured.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these Banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Typical I/O Behavior During Power-up
The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} Banks are active with valid input logic levels to properly control the output logic states of all the I/O Banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to VCCIO. The I/O pins will maintain the blank configuration until VCC, VCCAUX and VCCIO have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore, V_{CCIO} supplies should be powered up before or together with the V_{CC} and V_{CCAUX} supplies

Supported Standards
The MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The MachXO1200 and MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right Banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all Banks of MachXO1200 and MachXO2280 devices. PCI support is provided in the top Banks of the MachXO1200 and MachXO2280 devices. Table 2-8 summarizes the I/O characteristics of the devices in the MachXO family.

Tables 2-9 and 2-10 show the I/O standards (together with their supply and reference voltages) supported by the MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

Figure 2-22. MachXO Configuration and Programming

```
                    ┌─────────────────────────┐
                    │   ISP 1149.1 TAP Port   │
                    └─────────────────────────┘
                                 ↕
Port
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

         ┌──────────────────┐        ┌──────────────────┐
         │   Background     │        │      1532        │
         └──────────────────┘        └──────────────────┘

Mode
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
Program in seconds                              Configure in milliseconds
                       ┌──────────────┐
                       │  Power-up    │
         ┌──────────────┐ └──────────────┘  ┌──────────────┐
         │ Non-Volatile │──────────────────→│ SRAM Memory  │
         │ Memory Space │──────────────────→│    Space     │
         └──────────────┘                    └──────────────┘
                       ┌──────────────┐
                       │   Refresh    │
                       └──────────────┘
                       Download in
                       microseconds
```
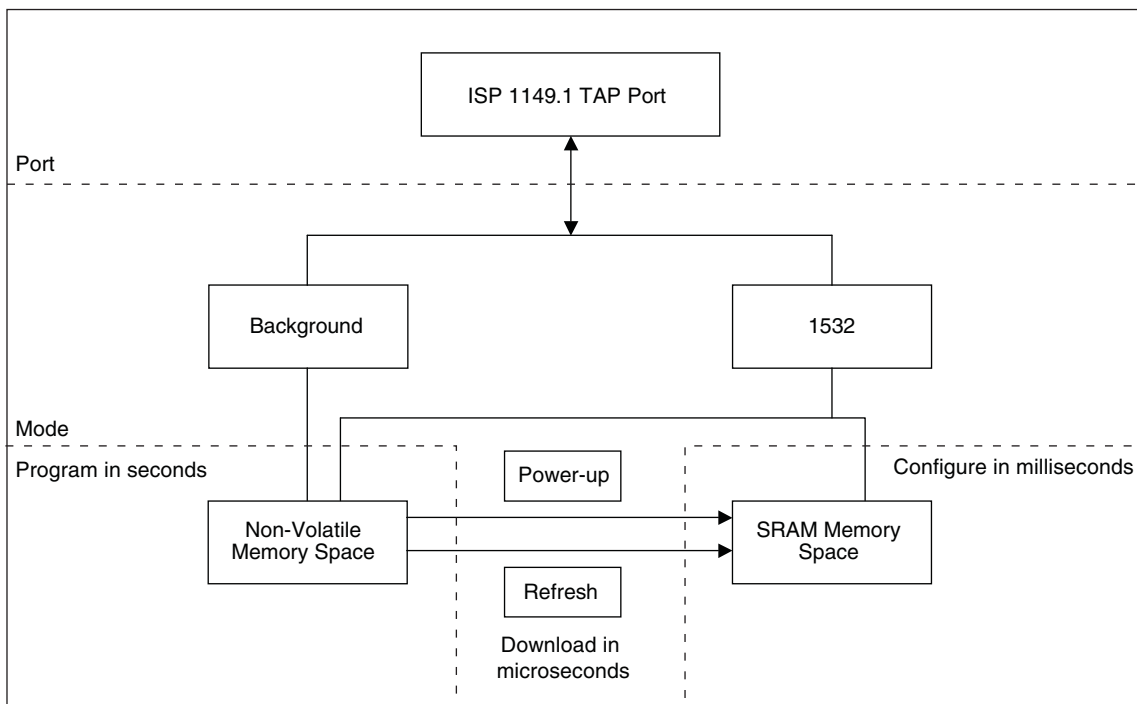
Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

sysIO Recommended Operating Conditions

| Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465
LVCMOS 2.5	2.375	2.5	2.625
LVCMOS 1.8	1.71	1.8	1.89
LVCMOS 1.5	1.425	1.5	1.575
LVCMOS 1.2	1.14	1.2	1.26
LVTTL	3.135	3.3	3.465
PCI[3]	3.135	3.3	3.465
LVDS[1, 2]	2.375	2.5	2.625
LVPECL[1]	3.135	3.3	3.465
BLVDS[1]	2.375	2.5	2.625
RSDS[1]	2.375	2.5	2.625

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers
3. Input on the top bank of the MachXO1200 and MachXO2280 only.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	2.4	16	-16
					0.4	V_{CCIO} - 0.4	12, 8, 4	-12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 ("C" Version)	-0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 ("E" Version)	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

Figure 3-5. JTAG Port Timing Waveforms
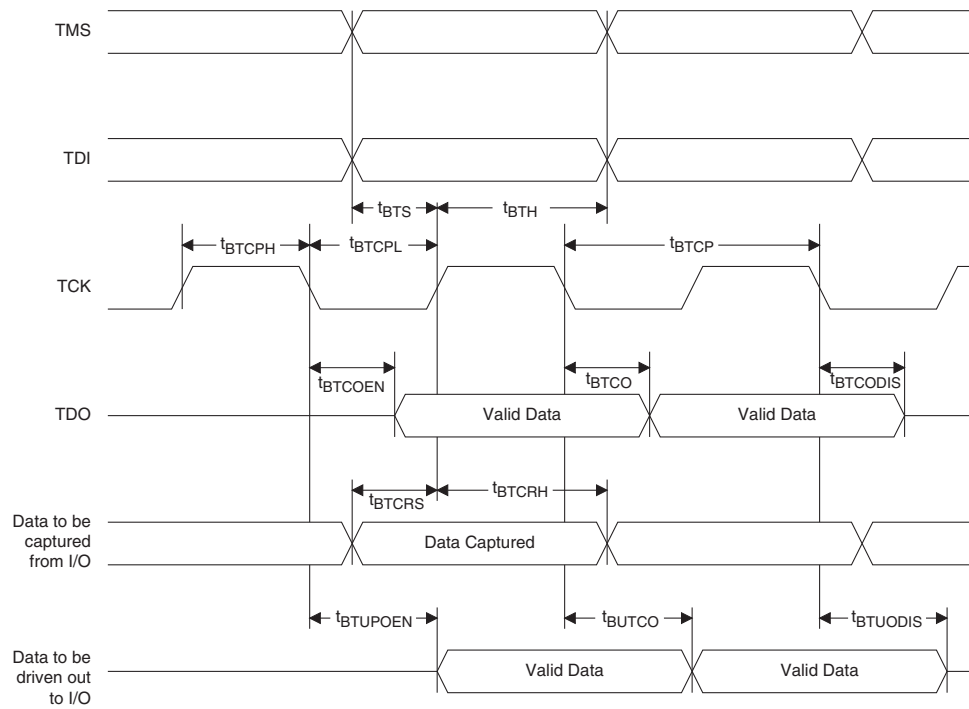
Switching Test Conditions

Figure 3-6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-6. Output Test Load, LVTTL and LVCMOS Standards
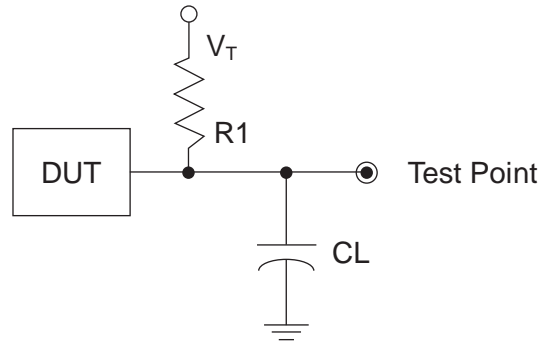
Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)				V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D/E/F]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D/E/F] indicates the PIO within the group to which the pad is connected. Some of these user programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-up resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-up resistor enabled.
GSRN	I	Global RESET signal (active low). Dedicated pad, when not in use it can be used as an I/O pin.
TSALL	I	TSALL is a dedicated pad for the global output enable signal. When TSALL is high all the outputs are tristated. It is a dual function pin. When not in use, it can be used as an I/O pin.
NC	—	No connect.
GND	—	GND - Ground. Dedicated pins.
V_{CC}	—	VCC - The power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	VCCAUX - the Auxiliary power supply pin. This pin powers up a variety of internal circuits including all the differential and referenced input buffers. Dedicated pins.
V_{CCIOx}	—	V_{CCIO} - The power supply pins for I/O Bank x. Dedicated pins.
SLEEPN[1]	I	Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ This pin has a weak internal pull-up, but when unused, an external pull-up to V_{CC} is recommended. When driven low, the device moves into Sleep mode after a specified time.
PLL and Clock Functions (Used as user programmable I/O pins when not used for PLL or clock pins)		
[LOC][0]_PLL[T, C]_IN	—	Reference clock (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
[LOC][0]_PLL[T, C]_FB	—	Optional feedback (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
PCLK [n]_[1:0]	—	Primary Clock Pads, n per side.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin -Test Data output pin used to shift data out of the device using 1149.1.

1. Applies to MachXO "C" devices only. NC for "E" devices.

Power Supply and NC

Signal	100 TQFP[1]	144 TQFP[1]	100 csBGA[2]
VCC	**LCMXO256/640**: 35, 90 **LCMXO1200/2280**: 17, 35, 66, 91	21, 52, 93, 129	P7, B6
VCCIO0	**LCMXO256**: 60, 74, 92 **LCMXO640**: 80, 92 **LCMXO1200/2280**: 94	**LCMXO640**: 117, 135 **LCMXO1200/2280**: 135	**LCMXO256**: H14, A14, B5 **LCMXO640**: B12, B5
VCCIO1	**LCMXO256**: 10, 24, 41 **LCMXO640**: 60, 74 **LCMXO1200/2280**: 80	**LCMXO640**: 82, 98 **LCMXO1200/2280**: 117	**LCMXO256**: G1, P1, P10 **LCMXO640**: H14, A14
VCCIO2	**LCMXO256**: None **LCMXO640**: 29, 41 **LCMXO1200/2280**: 70	**LCMXO640**: 38, 63 **LCMXO1200/2280**: 98	**LCMXO256**: None **LCMXO640**: P4, P10
VCCIO3	**LCMXO256**: None **LCMXO640**: 10, 24 **LCMXO1200/2280**: 56	**LCMXO640**: 10, 26 **LCMXO1200/2280**: 82	**LCMXO256**: None **LCMXO640**: G1, P1
VCCIO4	**LCMXO256/640**: None **LCMXO1200/2280**: 44	**LCMXO640**: None **LCMXO1200/2280**: 63	—
VCCIO5	**LCMXO256/640**: None **LCMXO1200/2280**: 27	**LCMXO640**: None **LCMXO1200/2280**: 38	—
VCCIO6	**LCMXO256/640**: None **LCMXO1200/2280**: 20	**LCMXO640**: None **LCMXO1200/2280**: 26	—
VCCIO7	**LCMXO256/640**: None **LCMXO1200/2280**: 6	**LCMXO640**: None **LCMXO1200/2280**: 10	—
VCCAUX	**LCMXO256/640**: 88 **LCMXO1200/2280**: 36, 90	53, 128	B7
GND[3]	**LCMXO256**: 40, 84, 62, 75, 93, 12, 25, 42 **LCMXO640**: 40, 84, 81, 93, 62, 75, 30, 42, 12, 25 **LCMXO1200/2280**: 9, 41, 59, 83, 100, 76, 50, 26	16, 59, 88, 123, 118, 136, 83, 99, 37, 64, 11, 27	**LCMXO256**: N9, B9, G14, B13, A4, H1, N2, N10 **LCMXO640**: N9, B9, A10, A4, G14, B13, N3, N10, H1, N2
NC[4]			—

1. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
2. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
3. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
4. NC pins should not be connected to any active signals, VCC or GND.

LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for "E" devices.

** Primary clock inputs are single-ended.

LCMXO1200 and LCMXO2280 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
82	PT9A	1			PT12C	1		T
83	GND	-			GND	-		
84	PT8B	1		C	PT11B	1		C
85	PT8A	1		T	PT11A	1		T
86	PT7D	1	PCLK1_1****		PT10B	1	PCLK1_1****	
87	PT6F	0	PCLK0_0****		PT9B	1	PCLK1_0****	
88	PT6D	0		C	PT8F	0		C
89	PT6C	0		T	PT8E	0		T
90	VCCAUX	-			VCCAUX	-		
91	VCC	-			VCC	-		
92	PT5B	0			PT6D	0		
93	PT4B	0			PT6F	0		
94	VCCIO0	0			VCCIO0	0		
95	PT3D	0		C	PT4B	0		C
96	PT3C	0		T	PT4A	0		T
97	PT3B	0			PT3B	0		
98	PT2B	0		C	PT2B	0		C
99	PT2A	0		T	PT2A	0		T
100**	GNDIO0 GNDIO7	-			GNDIO0 GNDIO7	-		

*Supports true LVDS outputs.
**Double bonded to the pin.
***NC for "E" devices.
****Primary clock inputs are single-ended.

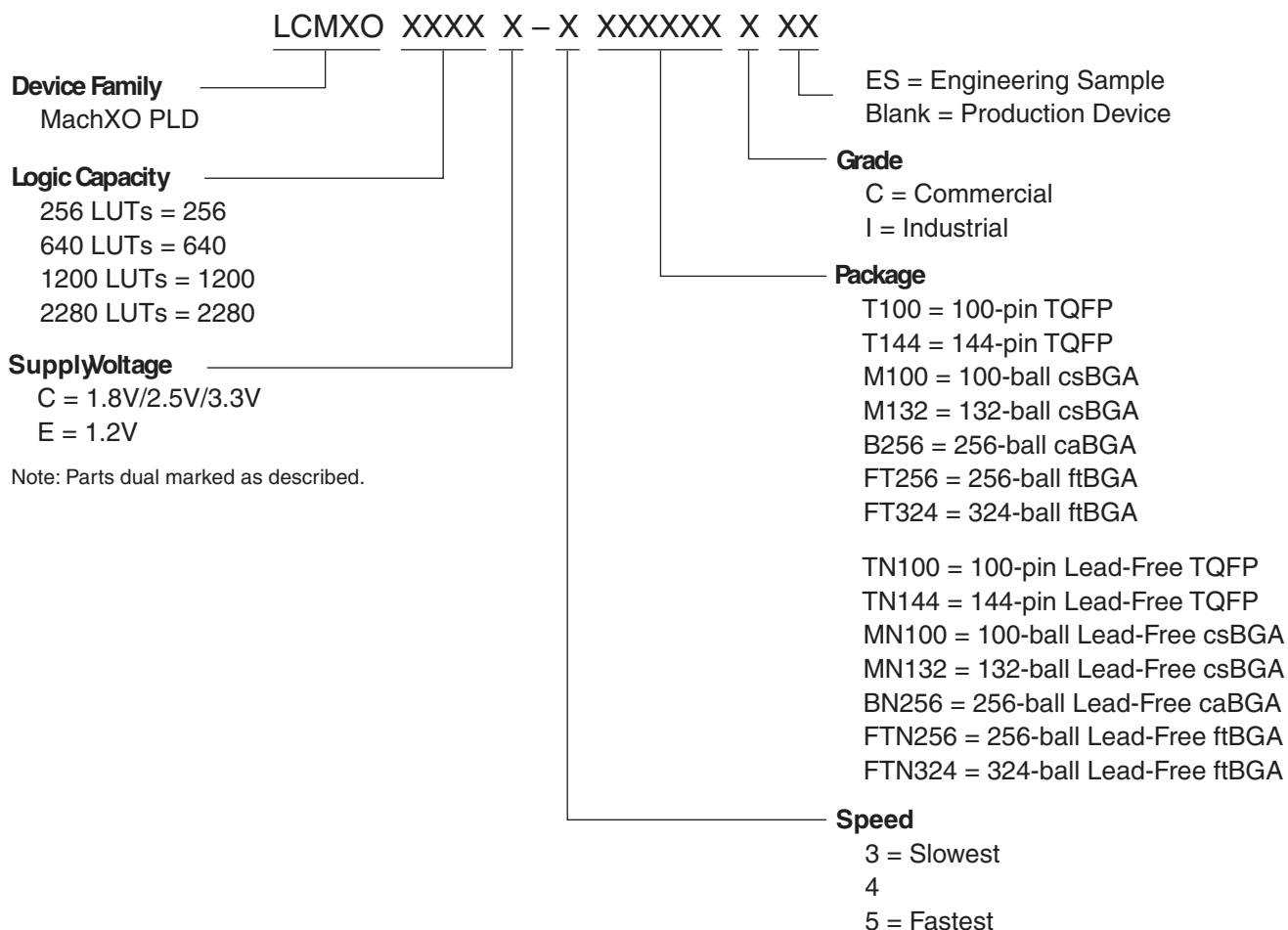## LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
101	PR3D	1		C	PR4B	2		C*	PR5B	2		C*
102	PR3C	1		T	PR4A	2		T*	PR5A	2		T*
103	PR3B	1		C	PR3D	2		C	PR4D	2		C
104	PR2D	1		C	PR3C	2		T	PR4C	2		T
105	PR3A	1		T	PR3B	2		C*	PR4B	2		C*
106	PR2B	1		C	PR3A	2		T*	PR4A	2		T*
107	PR2C	1		T	PR2B	2		C	PR3B	2		C*
108	PR2A	1		T	PR2A	2		T	PR3A	2		T*
109	PT9F	0		C	PT11D	1		C	PT16D	1		C
110	PT9D	0		C	PT11C	1		T	PT16C	1		T
111	PT9E	0		T	PT11B	1		C	PT16B	1		C
112	PT9B	0		C	PT11A	1		T	PT16A	1		T
113	PT9C	0		T	PT10F	1		C	PT15D	1		C
114	PT9A	0		T	PT10E	1		T	PT15C	1		T
115	PT8C	0			PT10D	1		C	PT14B	1		C
116	PT8B	0		C	PT10C	1		T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1			VCCIO1	1		
118	GNDIO0	0			GNDIO1	1			GNDIO1	1		
119	PT8A	0		T	PT9F	1		C	PT12F	1		C
120	PT7E	0			PT9E	1		T	PT12E	1		T
121	PT7C	0			PT9B	1		C	PT12D	1		C
122	PT7A	0			PT9A	1		T	PT12C	1		T
123	GND	-			GND	-			GND	-		
124	PT6B	0	PCLK0_1***	C	PT7D	1	PCLK1_1***		PT10B	1	PCLK1_1***	
125	PT6A	0		T	PT7B	1		C	PT9D	1		C
126	PT5C	0			PT7A	1		T	PT9C	1		T
127	PT5B	0	PCLK0_0***		PT6F	0	PCLK1_0***		PT9B	1	PCLK1_0***	
128	VCCAUX	-			VCCAUX	-			VCCAUX	-		
129	VCC	-			VCC	-			VCC	-		
130	PT4D	0			PT5D	0		C	PT7B	0		C
131	PT4B	0		C	PT5C	0		T	PT7A	0		T
132	PT4A	0		T	PT5B	0		C	PT6D	0		
133	PT3F	0			PT5A	0		T	PT6E	0		T
134	PT3D	0			PT4B	0			PT6F	0		C
135	VCCIO0	0			VCCIO0	0			VCCIO0	0		
136	GNDIO0	0			GNDIO0	0			GNDIO0	0		
137	PT3B	0		C	PT3D	0		C	PT4B	0		T
138	PT2F	0		C	PT3C	0		T	PT4A	0		C
139	PT3A	0		T	PT3B	0		C	PT3B	0		C
140	PT2D	0		C	PT3A	0		T	PT3A	0		T
141	PT2E	0		T	PT2D	0		C	PT2D	0		C
142	PT2B	0		C	PT2C	0		T	PT2C	0		T
143	PT2C	0		T	PT2B	0		C	PT2B	0		C
144	PT2A	0		T	PT2A	0		T	PT2A	0		T

*Supports true LVDS outputs.
**NC for "E" devices.
***Primary clock inputs arer single-ended.

Part Number Description

LCMXO   XXXX   X – X   XXXXXX   X   XX

Device Family
MachXO PLD

Logic Capacity
256 LUTs = 256
640 LUTs = 640
1200 LUTs = 1200
2280 LUTs = 2280

Supply Voltage
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked as described.

ES = Engineering Sample
Blank = Production Device

Grade
C = Commercial
I = Industrial

Package
T100 = 100-pin TQFP
T144 = 144-pin TQFP
M100 = 100-ball csBGA
M132 = 132-ball csBGA
B256 = 256-ball caBGA
FT256 = 256-ball ftBGA
FT324 = 324-ball ftBGA

TN100 = 100-pin Lead-Free TQFP
TN144 = 144-pin Lead-Free TQFP
MN100 = 100-ball Lead-Free csBGA
MN132 = 132-ball Lead-Free csBGA
BN256 = 256-ball Lead-Free caBGA
FTN256 = 256-ball Lead-Free ftBGA
FTN324 = 324-ball Lead-Free ftBGA

Speed
3 = Slowest
4
5 = Fastest

Ordering Information

Note: MachXO devices are dual marked except the slowest commercial speed grade device.þFor example the commercial speed grade LCMXO640E-4F256C is also marked with industrial grade -3I grade.þThe slowest commercial speed grade does not have industrial markings.þ The markings appears as follows:

|Lattice®

LCMXO640E
4F256C-3I

Datecode

Dual Mark
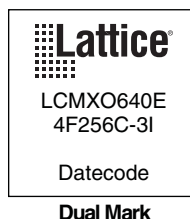
Conventional Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM
LCMXO256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM
LCMXO256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM
LCMXO256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM
LCMXO256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM
LCMXO256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMXO640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMXO640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMXO640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMXO640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMXO640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMXO640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMXO640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMXO640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMXO640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMXO640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMXO640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMXO1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMXO1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMXO1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMXO1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMXO1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMXO1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMXO1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMXO1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMXO1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMXO1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMXO1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMXO1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMXO1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMXO1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3T100I	256	1.2V	78	-3	TQFP	100	IND
LCMXO256E-4T100I	256	1.2V	78	-4	TQFP	100	IND
LCMXO256E-3M100I	256	1.2V	78	-3	csBGA	100	IND
LCMXO256E-4M100I	256	1.2V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3T100I	640	1.2V	74	-3	TQFP	100	IND
LCMXO640E-4T100I	640	1.2V	74	-4	TQFP	100	IND
LCMXO640E-3M100I	640	1.2V	74	-3	csBGA	100	IND
LCMXO640E-4M100I	640	1.2V	74	-4	csBGA	100	IND
LCMXO640E-3T144I	640	1.2V	113	-3	TQFP	144	IND
LCMXO640E-4T144I	640	1.2V	113	-4	TQFP	144	IND
LCMXO640E-3M132I	640	1.2V	101	-3	csBGA	132	IND
LCMXO640E-4M132I	640	1.2V	101	-4	csBGA	132	IND
LCMXO640E-3B256I	640	1.2V	159	-3	caBGA	256	IND
LCMXO640E-4B256I	640	1.2V	159	-4	caBGA	256	IND
LCMXO640E-3FT256I	640	1.2V	159	-3	ftBGA	256	IND
LCMXO640E-4FT256I	640	1.2V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100I	1200	1.2V	73	-3	TQFP	100	IND
LCMXO1200E-4T100I	1200	1.2V	73	-4	TQFP	100	IND
LCMXO1200E-3T144I	1200	1.2V	113	-3	TQFP	144	IND
LCMXO1200E-4T144I	1200	1.2V	113	-4	TQFP	144	IND
LCMXO1200E-3M132I	1200	1.2V	101	-3	csBGA	132	IND
LCMXO1200E-4M132I	1200	1.2V	101	-4	csBGA	132	IND
LCMXO1200E-3B256I	1200	1.2V	211	-3	caBGA	256	IND
LCMXO1200E-4B256I	1200	1.2V	211	-4	caBGA	256	IND
LCMXO1200E-3FT256I	1200	1.2V	211	-3	ftBGA	256	IND
LCMXO1200E-4FT256I	1200	1.2V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100I	2280	1.2V	73	-3	TQFP	100	IND
LCMXO2280E-4T100I	2280	1.2V	73	-4	TQFP	100	IND
LCMXO2280E-3T144I	2280	1.2V	113	-3	TQFP	144	IND
LCMXO2280E-4T144I	2280	1.2V	113	-4	TQFP	144	IND
LCMXO2280E-3M132I	2280	1.2V	101	-3	csBGA	132	IND
LCMXO2280E-4M132I	2280	1.2V	101	-4	csBGA	132	IND
LCMXO2280E-3B256I	2280	1.2V	211	-3	caBGA	256	IND
LCMXO2280E-4B256I	2280	1.2V	211	-4	caBGA	256	IND
LCMXO2280E-3FT256I	2280	1.2V	211	-3	ftBGA	256	IND
LCMXO2280E-4FT256I	2280	1.2V	211	-4	ftBGA	256	IND
LCMXO2280E-3FT324I	2280	1.2V	271	-3	ftBGA	324	IND
LCMXO2280E-4FT324I	2280	1.2V	271	-4	ftBGA	324	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3TN100I	256	1.2V	78	-3	Lead-Free TQFP	100	IND
LCMXO256E-4TN100I	256	1.2V	78	-4	Lead-Free TQFP	100	IND
LCMXO256E-3MN100I	256	1.2V	78	-3	Lead-Free csBGA	100	IND
LCMXO256E-4MN100I	256	1.2V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN100I	640	1.2V	74	-3	Lead-Free TQFP	100	IND
LCMXO640E-4TN100I	640	1.2V	74	-4	Lead-Free TQFP	100	IND
LCMXO640E-3MN100I	640	1.2V	74	-3	Lead-Free csBGA	100	IND
LCMXO640E-4MN100I	640	1.2V	74	-4	Lead-Free csBGA	100	IND
LCMXO640E-3TN144I	640	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO640E-4TN144I	640	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO640E-3MN132I	640	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO640E-4MN132I	640	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO640E-3BN256I	640	1.2V	159	-3	Lead-Free caBGA	256	IND
LCMXO640E-4BN256I	640	1.2V	159	-4	Lead-Free caBGA	256	IND
LCMXO640E-3FTN256I	640	1.2V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640E-4FTN256I	640	1.2V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100I	1200	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200E-4TN100I	1200	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200E-3TN144I	1200	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200E-4TN144I	1200	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200E-3MN132I	1200	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200E-4MN132I	1200	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200E-3BN256I	1200	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200E-4BN256I	1200	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200E-3FTN256I	1200	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200E-4FTN256I	1200	1.2V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100I	2280	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280E-4TN100I	2280	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280E-3TN144I	2280	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280E-4TN144I	2280	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280E-3MN132I	2280	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280E-4MN132I	2280	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280E-3BN256I	2280	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280E-4BN256I	2280	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280E-3FTN256I	2280	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280E-4FTN256I	2280	1.2V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280E-3FTN324I	2280	1.2V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280E-4FTN324I	2280	1.2V	271	-4	Lead-Free ftBGA	324	IND

Date	Version	Section	Change Summary
April 2006 (cont.)	02.0 (cont.)	Architecture (cont.)	"Top View of the MachXO1200 Device" figure updated.
			"Top View of the MachXO640 Device" figure updated.
			"Top View of the MachXO256 Device" figure updated.
			"Slice Diagram" figure updated.
			Slice Signal Descriptions table updated.
			Routing section updated.
			sysCLOCK Phase Lockecd Loops (PLLs) section updated.
			PLL Diagram updated.
			PLL Signal Descriptions table updated.
			sysMEM Memory section has been updated.
			PIO Groups section has been updated.
			PIO section has been updated.
			MachXO PIO Block Diagram updated.
			Supported Input Standards table updated.
			MachXO Configuration and Programming diagram updated.
		DC and Switching Characteristics	Recommended Operating Conditions table - footnotes updated.
			MachXO256 and MachXO640 Hot Socketing Specifications - footnotes updated.
			Added MachXO1200 and MachXO2280 Hot Socketing Specifications table.
			DC Electrical Characteristics, footnotes have been updated.
			Supply Current (Sleep Mode) table has been updated, removed "4W" references. Footnotes have been updated.
			Supply Current (Standby) table and associated footnotes updated.
			Intialization Supply Current table and footnotes updated.
			Programming and Erase Flash Supply Current table and associated footnotes have been updatd.
			Register-to-Register Performance table updated (rev. A 0.19).
			MachXO External Switching Characteristics updated (rev. A 0.19).
			MachXO Internal Timing Parameters updated (rev. A 0.19).
			MachXO Family Timing Adders updated (rev. A 0.19).
			sysCLOCK Timing updated (rev. A 0.19).
			MachXO "C" Sleep Mode Timing updated (A 0.19).
			JTAG Port Timing Specification updated (rev. A 0.19).
			Test Fixture Required Components table updated.
		Pinout Information	Signal Descriptions have been updated.
			Pin Information Summary has been updated. Footnote has been added.
			Power Supply and NC Connection table has been updated.
			Logic Signal Connections have been updated (PCLKTx_x --> PCLKx_x)
		Ordering Information	Removed "4W" references.
			Added 256-ftBGA Ordering Part Numbers for MachXO640.
May 2006	02.1	Pinout Information	Removed [LOC][0]_PLL_RST from Signal Description table.
			PCLK footnote has been added to all appropriate pins.
August 2006	02.2	Multiple	Removed 256 fpBGA information for MachXO640.