

Welcome to [E-XFL.COM](#)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	-
Number of I/O	113
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo640c-3tn144c

Figure 2-20. MachXO640 Banks

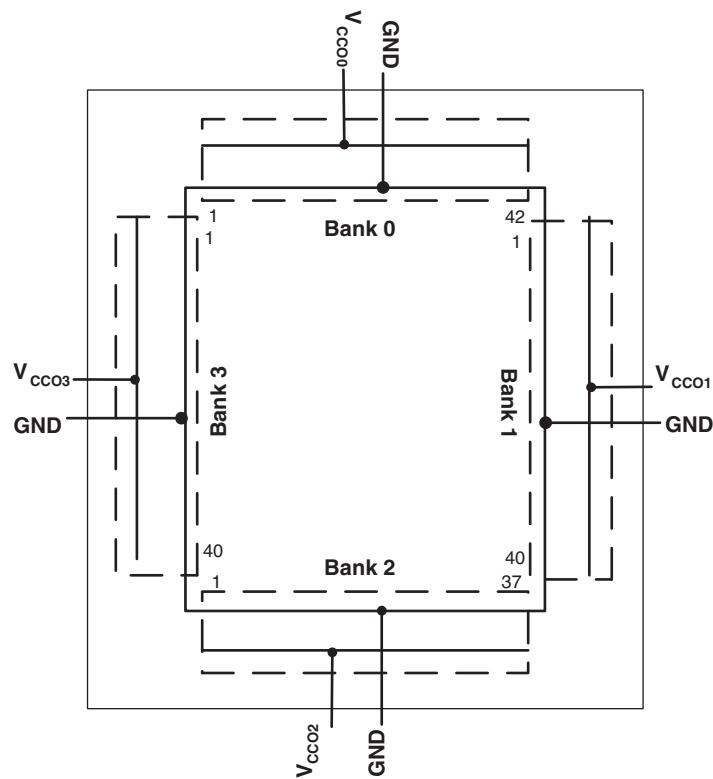
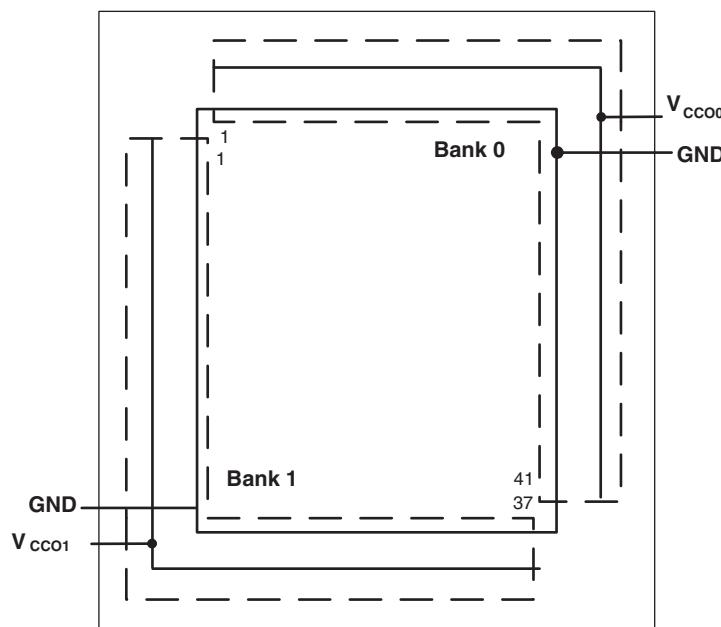


Figure 2-21. MachXO256 Banks



Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of

the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The MachXO "C" devices ($V_{CC} = 1.8/2.5/3.3V$) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

Table 2-11. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static I_{CC}	Typical <10mA	0	Typical <100uA
I/O Leakage	<10 μ A	<1mA	<10 μ A
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1} ; MachXO640: V_{CCIO2} ; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Supply Current (Sleep Mode)^{1,2}

Symbol	Parameter	Device	Typ. ³	Max.	Units
I_{CC}	Core Power Supply	LCMxo256C	12	25	μA
		LCMxo640C	12	25	μA
		LCMxo1200C	12	25	μA
		LCMxo2280C	12	25	μA
I_{CCAUX}	Auxiliary Power Supply	LCMxo256C	1	15	μA
		LCMxo640C	1	25	μA
		LCMxo1200C	1	45	μA
		LCMxo2280C	1	85	μA
I_{CCIO}	Bank Power Supply ⁴	All LCMxo 'C' Devices	2	30	μA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.

2. Frequency = 0MHz.

3. $T_A = 25^\circ C$, power supplies at nominal voltage.

4. Per Bank.

Supply Current (Standby)^{1, 2, 3, 4}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMxo256C	7	mA
		LCMxo640C	9	mA
		LCMxo1200C	14	mA
		LCMxo2280C	20	mA
		LCMxo256E	4	mA
		LCMxo640E	6	mA
		LCMxo1200E	10	mA
		LCMxo2280E	12	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LCMxo256E/C	5	mA
		LCMxo640E/C	7	mA
		LCMxo1200E/C	12	mA
		LCMxo2280E/C	13	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND.

3. Frequency = 0MHz.

4. User pattern = blank.

5. $T_J = 25^\circ C$, power supplies at nominal voltage.

6. Per Bank. $V_{CCIO} = 2.5V$. Does not include pull-up/pull-down.

Initialization Supply Current^{1, 2, 3, 4}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I _{CC}	Core Power Supply	LCMxo256C	13	mA
		LCMxo640C	17	mA
		LCMxo1200C	21	mA
		LCMxo2280C	23	mA
		LCMxo256E	10	mA
		LCMxo640E	14	mA
		LCMxo1200E	18	mA
		LCMxo2280E	20	mA
I _{CCAUX}	Auxiliary Power Supply V _{CCAUX} = 3.3V	LCMxo256C/E	10	mA
		LCMxo640E/C	13	mA
		LCMxo1200E/C	24	mA
		LCMxo2280E/C	25	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Frequency = 0MHz.
4. Typical user pattern.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank, V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁵	Units
I _{CC}	Core Power Supply	LCMxo256C	9	mA
		LCMxo640C	11	mA
		LCMxo1200C	16	mA
		LCMxo2280C	22	mA
		LCMxo256E	6	mA
		LCMxo640E	8	mA
		LCMxo1200E	12	mA
		LCMxo2280E	14	mA
I _{CCAUX}	Auxiliary Power Supply V _{CCAUX} = 3.3V	LCMxo256C/E	8	mA
		LCMxo640C/E	10	mA
		LCMxo1200/E	15	mA
		LCMxo2280C/E	16	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Typical user pattern.
4. JTAG programming is at 25MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

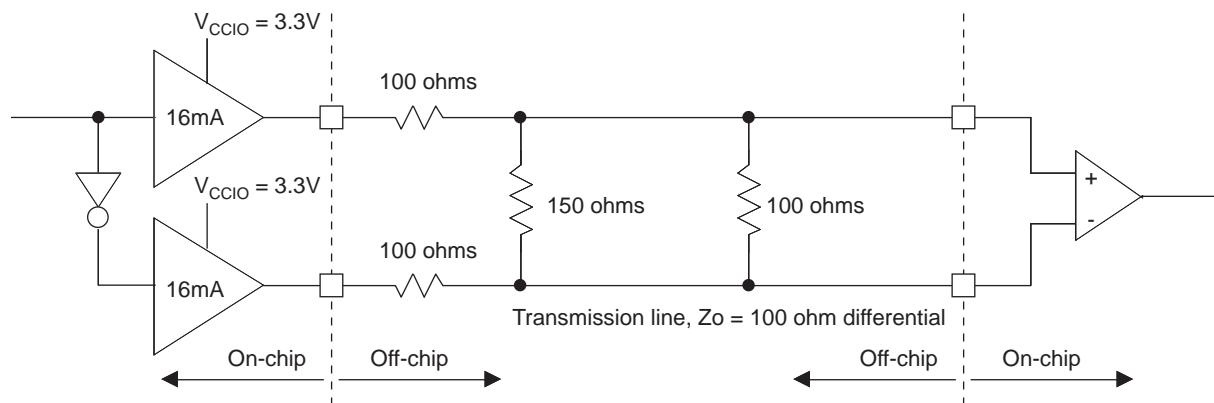
Table 3-2. BLVDS DC Conditions¹
Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	100	100	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

Table 3-3. LVPECL DC Conditions¹
Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	100	Ohms
R _P	Driver parallel resistor	150	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	2.03	V
V _{OL}	Output low voltage	1.27	V
V _{OD}	Output differential voltage	0.76	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	85.7	Ohms
I _{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4 ^{5, 6}	18	25	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f_{VCO}	PLL VCO Frequency		420	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4 ^{5, 6}	18	25	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	55	%
t_{PH}^4	Output Phase Accuracy		—	0.05	UI
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	+/-120	ps
		$f_{OUT} < 100$ MHz	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	1	—	ns
t_{LOCK}^2	PLL Lock-in Time		—	150	μs
t_{PA}	Programmable Delay Unit		100	450	ps
t_{IPJIT}	Input Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	+/-200	ps
		$f_{OUT} < 100$ MHz	—	0.02	UI
t_{FBKDLY}	External Feedback Delay		—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST Pulse Width		10	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output.

5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.

6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.

Rev. A 0.19

Power Supply and NC

Signal	100 TQFP ¹	144 TQFP ¹	100 csBGA ²
VCC	LCMxo256/640: 35, 90 LCMxo1200/2280: 17, 35, 66, 91	21, 52, 93, 129	P7, B6
VCCIO0	LCMxo256: 60, 74, 92 LCMxo640: 80, 92 LCMxo1200/2280: 94	LCMxo640: 117, 135 LCMxo1200/2280: 135	LCMxo256: H14, A14, B5 LCMxo640: B12, B5
VCCIO1	LCMxo256: 10, 24, 41 LCMxo640: 60, 74 LCMxo1200/2280: 80	LCMxo640: 82, 98 LCMxo1200/2280: 117	LCMxo256: G1, P1, P10 LCMxo640: H14, A14
VCCIO2	LCMxo256: None LCMxo640: 29, 41 LCMxo1200/2280: 70	LCMxo640: 38, 63 LCMxo1200/2280: 98	LCMxo256: None LCMxo640: P4, P10
VCCIO3	LCMxo256: None LCMxo640: 10, 24 LCMxo1200/2280: 56	LCMxo640: 10, 26 LCMxo1200/2280: 82	LCMxo256: None LCMxo640: G1, P1
VCCIO4	LCMxo256/640: None LCMxo1200/2280: 44	LCMxo640: None LCMxo1200/2280: 63	—
VCCIO5	LCMxo256/640: None LCMxo1200/2280: 27	LCMxo640: None LCMxo1200/2280: 38	—
VCCIO6	LCMxo256/640: None LCMxo1200/2280: 20	LCMxo640: None LCMxo1200/2280: 26	—
VCCIO7	LCMxo256/640: None LCMxo1200/2280: 6	LCMxo640: None LCMxo1200/2280: 10	—
VCCAUX	LCMxo256/640: 88 LCMxo1200/2280: 36, 90	53, 128	B7
GND ³	LCMxo256: 40, 84, 62, 75, 93, 12, 25, 42 LCMxo640: 40, 84, 81, 93, 62, 75, 30, 42, 12, 25 LCMxo1200/2280: 9, 41, 59, 83, 100, 76, 50, 26	16, 59, 88, 123, 118, 136, 83, 99, 37, 64, 11, 27	LCMxo256: N9, B9, G14, B13, A4, H1, N2, N10 LCMxo640: N9, B9, A10, A4, G14, B13, N3, N10, H1, N2
NC ⁴			—

1. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
2. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
3. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
4. NC pins should not be connected to any active signals, VCC or GND.

Power Supply and NC (Cont.)

Signal	132 csBGA ¹	256 caBGA / 256 ftBGA ¹	324 ftBGA ¹
VCC	H3, P6, G12, C7	G7, G10, K7, K10	F14, G11, G9, H7, L7, M9
VCCIO0	LCMxo640: B11, C5 LCMxo1200/2280: C5	LCMxo640: F8, F7, F9, F10 LCMxo1200/2280: F8, F7	G8, G7
VCCIO1	LCMxo640: L12, E12 LCMxo1200/2280: B11	LCMxo640: H11, G11, K11, J11 LCMxo1200/2280: F9, F10	G12, G10
VCCIO2	LCMxo640: N2, M10 LCMxo1200/2280: E12	LCMxo640: L9, L10, L8, L7 LCMxo1200/2280: H11, G11	J12, H12
VCCIO3	LCMxo640: D2, K3 LCMxo1200/2280: L12	LCMxo640: K6, J6, H6, G6 LCMxo1200/2280: K11, J11	L12, K12
VCCIO4	LCMxo640: None LCMxo1200/2280: M10	LCMxo640: None LCMxo1200/2280: L9, L10	M12, M11
VCCIO5	LCMxo640: None LCMxo1200/2280: N2	LCMxo640: None LCMxo1200/2280: L8, L7	M8, R9
VCCIO6	LCMxo640: None LCMxo1200/2280: K3	LCMxo640: None LCMxo1200/2280: K6, J6	M7, K7
VCCIO7	LCMxo640: None LCMxo1200/2280: D2	LCMxo640: None LCMxo1200/2280: H6, G6	H6, J7
VCCAUX	P7, A7	T9, A8	M10, F9
GND ²	F1, P9, J14, C9, A10, B4, L13, D13, P2, N11, E1, L2	A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16	E14, F16, H10, H11, H8, H9, J10, J11, J4, J8, J9, K10, K11, K17, K8, K9, L10, L11, L8, L9, N2, P14, P5, R7
NC ³	—	LCMxo640: E4, E5, F5, F6, C3, C2, G4, G5, H4, H5, K5, K4, M5, M4, P2, P3, N5, N6, M7, M8, N10, N11, R15, R16, P15, P16, M11, L11, N12, N13, M13, M12, K12, J12, F12, F13, E12, E13, D13, D14, B15, A15, C14, B14, E11, E10, E7, E6, D4, D3, B3, B2 LCMxo1200: None LCMxo2280: None	—

1. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
3. NC pins should not be connected to any active signals, VCC or GND.

LCMxo1200 and LCMxo2280 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
82	PT9A	1			PT12C	1		T
83	GND	-			GND	-		
84	PT8B	1		C	PT11B	1		C
85	PT8A	1		T	PT11A	1		T
86	PT7D	1	PCLK1_1****		PT10B	1	PCLK1_1****	
87	PT6F	0	PCLK0_0****		PT9B	1	PCLK1_0****	
88	PT6D	0		C	PT8F	0		C
89	PT6C	0		T	PT8E	0		T
90	VCCAUX	-			VCCAUX	-		
91	VCC	-			VCC	-		
92	PT5B	0			PT6D	0		
93	PT4B	0			PT6F	0		
94	VCCIO0	0			VCCIO0	0		
95	PT3D	0		C	PT4B	0		C
96	PT3C	0		T	PT4A	0		T
97	PT3B	0			PT3B	0		
98	PT2B	0		C	PT2B	0		C
99	PT2A	0		T	PT2A	0		T
100**	GNDIO0 GNDIO7	-			GNDIO0 GNDIO7	-		

*Supports true LVDS outputs.

**Double bonded to the pin.

***NC for "E" devices.

****Primary clock inputs are single-ended.

**LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections:
 132 csBGA (Cont.)**

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
M9	PB7B	2		C	M9	PB9B	4		C	M9	PB12B	4		C
N10	PB7E	2		T	N10	PB9C	4		T	N10	PB12C	4		T
P10	PB7F	2		C	P10	PB9D	4		C	P10	PB12D	4		C
N11	GNDIO2	2			N11	GNDIO4	4			N11	GNDIO4	4		
P11	PB8C	2		T	P11	PB10A	4		T	P11	PB13C	4		T
M11	PB8D	2		C	M11	PB10B	4		C	M11	PB13D	4		C
P12	PB9C	2		T	P12	PB10C	4			P12	PB15B	4		
P13	PB9D	2		C	P13	PB11C	4		T	P13	PB16C	4		T
N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN		N12**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB11D	4		C	P14	PB16D	4		C
N14	PR11D	1		C	N14	PR16B	3		C	N14	PR19B	3		C
M14	PR11C	1		T	M14	PR15B	3		C*	M14	PR18B	3		C*
N13	PR11B	1		C	N13	PR16A	3		T	N13	PR19A	3		T
M12	PR11A	1		T	M12	PR15A	3		T*	M12	PR18A	3		T*
M13	PR10B	1		C	M13	PR14B	3		C*	M13	PR17B	3		C*
L14	PR10A	1		T	L14	PR14A	3		T*	L14	PR17A	3		T*
L13	GNDIO1	1			L13	GNDIO3	3			L13	GNDIO3	3		
K14	PR8D	1		C	K14	PR12B	3		C*	K14	PR15B	3		C*
K13	PR8C	1		T	K13	PR12A	3		T*	K13	PR15A	3		T*
K12	PR8B	1		C	K12	PR11B	3		C*	K12	PR14B	3		C*
J13	PR8A	1		T	J13	PR11A	3		T*	J13	PR14A	3		T*
J12	PR7C	1			J12	PR10B	3		C*	J12	PR13B	3		C*
H14	PR7B	1		C	H14	PR10A	3		T*	H14	PR13A	3		T*
H13	PR7A	1		T	H13	PR9B	3		C*	H13	PR11B	3		C*
H12	PR6D	1		C	H12	PR9A	3		T*	H12	PR11A	3		T*
G13	PR6C	1		T	G13	PR8B	2		C*	G13	PR10B	2		C*
G14	PR6B	1			G14	PR8A	2		T*	G14	PR10A	2		T*
G12	VCC	-			G12	VCC	-			G12	VCC	-		
F14	PR5D	1		C	F14	PR6C	2			F14	PR8C	2		
F13	PR5C	1		T	F13	PR6B	2		C*	F13	PR8B	2		C*
F12	PR4D	1		C	F12	PR6A	2		T*	F12	PR8A	2		T*
E13	PR4C	1		T	E13	PR5B	2		C*	E13	PR7B	2		C*
E14	PR4B	1			E14	PR5A	2		T*	E14	PR7A	2		T*
D13	GNDIO1	1			D13	GNDIO2	2			D13	GNDIO2	2		
D14	PR3D	1		C	D14	PR4B	2		C*	D14	PR5B	2		C*
D12	PR3C	1		T	D12	PR4A	2		T*	D12	PR5A	2		T*
C14	PR2D	1		C	C14	PR3D	2		C	C14	PR4D	2		C
B14	PR2C	1		T	B14	PR2B	2		C	B14	PR3B	2		C*
C13	PR2B	1		C	C13	PR3C	2		T	C13	PR4C	2		T
A14	PR2A	1		T	A14	PR2A	2		T	A14	PR3A	2		T*
A13	PT9F	0		C	A13	PT11D	1		C	A13	PT16D	1		C
A12	PT9E	0		T	A12	PT11B	1		C	A12	PT16B	1		C
B13	PT9D	0		C	B13	PT11C	1		T	B13	PT16C	1		T
B12	PT9C	0		T	B12	PT10F	1			B12	PT15D	1		
C12	PT9B	0		C	C12	PT11A	1		T	C12	PT16A	1		T
A11	PT9A	0		T	A11	PT10D	1		C	A11	PT14B	1		C
C11	PT8C	0			C11	PT10C	1		T	C11	PT14A	1		T
A10	GNDIO0	0			A10	GNDIO1	1			A10	GNDIO1	1		
B10	PT7F	0		C	B10	PT9F	1		C	B10	PT12F	1		C
C10	PT7E	0		T	C10	PT9E	1		T	C10	PT12E	1		T

**LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections:
 132 csBGA (Cont.)**

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1***	C	A8	PT7D	1	PCLK1_1***		A8	PT10B	1	PCLK1_1***	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0***	C	C8	PT6F	0	PCLK1_0***		C8	PT9B	1	PCLK1_0***	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	-			A7	VCCAUX	-			A7	VCCAUX	-		
C7	VCC	-			C7	VCC	-			C7	VCC	-		
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	-			F1	GND	-			F1	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
C9	GND	-			C9	GND	-			C9	GND	-		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 144 TQFP (Cont.)**

Pin Number	LCMxo640				LCMxo1200				LCMxo2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
51	TDI	2	TDI		TDI	5	TDI		TDI	5	TDI	
52	VCC	-			VCC	-			VCC	-		
53	VCCAUX	-			VCCAUX	-			VCCAUX	-		
54	PB5A	2		T	PB6F	5			PB8F	5		
55	PB5B	2	PCLKT2_1***	C	PB7B	4	PCLK4_1***		PB10F	4	PCLK4_1***	
56	PB5D	2			PB7C	4			PB10C	4		T
57	PB6A	2		T	PB7D	4			PB10D	4		C
58	PB6B	2	PCLKT2_0***	C	PB7F	4	PCLK4_0***		PB10B	4	PCLK4_0***	
59	GND	-			GND	-			GND	-		
60	PB7C	2			PB9A	4			PB12A	4		T
61	PB7E	2			PB9B	4			PB12B	4		C
62	PB8A	2			PB9E	4			PB12E	4		
63	VCCIO2	2			VCCIO4	4			VCCIO4	4		
64	GNDIO2	2			GNDIO4	4			GNDIO4	4		
65	PB8C	2		T	PB10A	4			PB13A	4		T
66	PB8D	2		C	PB10B	4			PB13B	4		C
67	PB9A	2		T	PB10C	4			PB13C	4		T
68	PB9C	2		T	PB10D	4			PB13D	4		C
69	PB9B	2		C	PB10F	4			PB14D	4		
70**	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN	
71	PB9D	2		C	PB11C	4			PB16C	4		T
72	PB9F	2			PB11D	4			PB16D	4		C
73	PR11D	1		C	PR16B	3			PR20B	3		C
74	PR11B	1		C	PR16A	3			PR20A	3		T
75	PR11C	1		T	PR15B	3			PR19B	3		C
76	PR10D	1		C	PR15A	3			PR19A	3		T
77	PR11A	1		T	PR14D	3			PR17D	3		C
78	PR10B	1		C	PR14C	3			PR17C	3		T
79	PR10C	1		T	PR14B	3			PR17B	3		C*
80	PR10A	1		T	PR14A	3			PR17A	3		T*
81	PR9D	1			PR13D	3			PR16D	3		
82	VCCIO1	1			VCCIO3	3			VCCIO3	3		
83	GNDIO1	1			GNDIO3	3			GNDIO3	3		
84	PR9A	1			PR12B	3			PR15B	3		C*
85	PR8C	1			PR12A	3			PR15A	3		T*
86	PR8A	1			PR11B	3			PR14B	3		C*
87	PR7D	1			PR11A	3			PR14A	3		T*
88	GND	-			GND	-			GND	-		
89	PR7B	1		C	PR10B	3			PR13B	3		C*
90	PR7A	1		T	PR10A	3			PR13A	3		T*
91	PR6D	1		C	PR8B	2			PR10B	2		C*
92	PR6C	1		T	PR8A	2			PR10A	2		T*
93	VCC	-			VCC	-			VCC	-		
94	PR5D	1			PR6B	2			PR8B	2		C*
95	PR5B	1			PR6A	2			PR8A	2		T*
96	PR4D	1			PR5B	2			PR7B	2		C*
97	PR4B	1		C	PR5A	2			PR7A	2		T*
98	VCCIO1	1			VCCIO2	2			VCCIO2	2		
99	GNDIO1	1			GNDIO2	2			GNDIO2	2		
100	PR4A	1		T	PR4C	2			PR5C	2		

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 144 TQFP (Cont.)**

Pin Number	LCMxo640				LCMxo1200				LCMxo2280				
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	
101	PR3D	1		C	PR4B	2			C*	PR5B	2		C*
102	PR3C	1		T	PR4A	2			T*	PR5A	2		T*
103	PR3B	1		C	PR3D	2			C	PR4D	2		C
104	PR2D	1		C	PR3C	2			T	PR4C	2		T
105	PR3A	1		T	PR3B	2			C*	PR4B	2		C*
106	PR2B	1		C	PR3A	2			T*	PR4A	2		T*
107	PR2C	1		T	PR2B	2			C	PR3B	2		C*
108	PR2A	1		T	PR2A	2			T	PR3A	2		T*
109	PT9F	0		C	PT11D	1			C	PT16D	1		C
110	PT9D	0		C	PT11C	1			T	PT16C	1		T
111	PT9E	0		T	PT11B	1			C	PT16B	1		C
112	PT9B	0		C	PT11A	1			T	PT16A	1		T
113	PT9C	0		T	PT10F	1			C	PT15D	1		C
114	PT9A	0		T	PT10E	1			T	PT15C	1		T
115	PT8C	0			PT10D	1			C	PT14B	1		C
116	PT8B	0		C	PT10C	1			T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1				VCCIO1	1		
118	GNDIO0	0			GNDIO1	1				GNDIO1	1		
119	PT8A	0		T	PT9F	1			C	PT12F	1		C
120	PT7E	0			PT9E	1			T	PT12E	1		T
121	PT7C	0			PT9B	1			C	PT12D	1		C
122	PT7A	0			PT9A	1			T	PT12C	1		T
123	GND	-			GND	-				GND	-		
124	PT6B	0	PCLK0_1***	C	PT7D	1	PCLK1_1***			PT10B	1	PCLK1_1***	
125	PT6A	0		T	PT7B	1			C	PT9D	1		C
126	PT5C	0			PT7A	1			T	PT9C	1		T
127	PT5B	0	PCLK0_0***		PT6F	0	PCLK1_0***			PT9B	1	PCLK1_0***	
128	VCCAUX	-			VCCAUX	-				VCCAUX	-		
129	VCC	-			VCC	-				VCC	-		
130	PT4D	0			PT5D	0			C	PT7B	0		C
131	PT4B	0		C	PT5C	0			T	PT7A	0		T
132	PT4A	0		T	PT5B	0			C	PT6D	0		
133	PT3F	0			PT5A	0			T	PT6E	0		T
134	PT3D	0			PT4B	0				PT6F	0		C
135	VCCIO0	0			VCCIO0	0				VCCIO0	0		
136	GNDIO0	0			GNDIO0	0				GNDIO0	0		
137	PT3B	0		C	PT3D	0			C	PT4B	0		T
138	PT2F	0		C	PT3C	0			T	PT4A	0		C
139	PT3A	0		T	PT3B	0			C	PT3B	0		C
140	PT2D	0		C	PT3A	0			T	PT3A	0		T
141	PT2E	0		T	PT2D	0			C	PT2D	0		C
142	PT2B	0		C	PT2C	0			T	PT2C	0		T
143	PT2C	0		T	PT2B	0			C	PT2B	0		C
144	PT2A	0		T	PT2A	0			T	PT2A	0		T

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640				LCMxo1200				LCMxo2280					
Ball Number	Ball Function	Bank	Dual Function	Ball Number	Ball Function	Bank	Dual Function	Ball Number	Ball Function	Bank	Dual Function		
J4	PL8A	3	T	J4	PL13A	6	T*	J4	PL16A	6	T*		
J5	PL8B	3	C	J5	PL13B	6	C*	J5	PL16B	6	C*		
R1	PL11A	3	T	R1	PL13C	6	T	R1	PL16C	6	T		
R2	PL11B	3	C	R2	PL13D	6	C	R2	PL16D	6	C		
-	-	-	-	-	-	-	-	GND	GND	-	-		
K5	NC			K5	PL14A	6	LLM0_PLLT_FB_A	T*	K5	PL17A	6	LLM0_PLLT_FB_A	
K4	NC			K4	PL14B	6	LLM0_PLLC_FB_A	C*	K4	PL17B	6	LLM0_PLLC_FB_A	
L5	PL10C	3	T	L5	PL14C	6	T	L5	PL17C	6	T		
L4	PL10D	3	C	L4	PL14D	6	C	L4	PL17D	6	C		
M5	NC			M5	PL15A	6	LLM0_PLLT_IN_A	T*	M5	PL18A	6	LLM0_PLLT_IN_A	
M4	NC			M4	PL15B	6	LLM0_PLLC_IN_A	C*	M4	PL18B	6	LLM0_PLLC_IN_A	
N4	PL11C	3	T	N4	PL16A	6	T	N4	PL19A	6	T		
N3	PL11D	3	C	N3	PL16B	6	C	N3	PL19B	6	C		
VCCIO3	VCCIO3	3		VCCIO6	VCCIO6	6		VCCIO6	VCCIO6	6			
GND	GNDIO3	3		GND	GNDIO6	6		GND	GNDIO6	6			
GND	GNDIO2	2		GND	GNDIO5	5		GND	GNDIO5	5			
VCCIO2	VCCIO2	2		VCCIO5	VCCIO5	5		VCCIO5	VCCIO5	5			
P4	TMS	2	TMS	P4	TMS	5	TMS	P4	TMS	5	TMS		
P2	NC			P2	PB2A	5	T	P2	PB2A	5	T		
P3	NC			P3	PB2B	5	C	P3	PB2B	5	C		
N5	NC			N5	PB2C	5	T	N5	PB2C	5	T		
R3	TCK	2	TCK	R3	TCK	5	TCK	R3	TCK	5	TCK		
N6	NC			N6	PB2D	5	C	N6	PB2D	5	C		
T2	PB2A	2	T	T2	PB3A	5	T	T2	PB3A	5	T		
T3	PB2B	2	C	T3	PB3B	5	C	T3	PB3B	5	C		
R4	PB2C	2	T	R4	PB3C	5	T	R4	PB3C	5	T		
R5	PB2D	2	C	R5	PB3D	5	C	R5	PB3D	5	C		
P5	PB3A	2	T	P5	PB4A	5	T	P5	PB4A	5	T		
P6	PB3B	2	C	P6	PB4B	5	C	P6	PB4B	5	C		
T5	PB3C	2	T	T5	PB4C	5	T	T5	PB4C	5	T		
M6	TDO	2	TDO	M6	TDO	5	TDO	M6	TDO	5	TDO		
T4	PB3D	2	C	T4	PB4D	5	C	T4	PB4D	5	C		
R6	PB4A	2	T	R6	PB5A	5	T	R6	PB5A	5	T		
GND	GNDIO2	2		GND	GNDIO5	5		GND	GNDIO5	5			
VCCIO2	VCCIO2	2		VCCIO5	VCCIO5	5		VCCIO5	VCCIO5	5			
T6	PB4B	2	C	T6	PB5B	5	C	T6	PB5B	5	C		
N7	TDI	2	TDI	N7	TDI	5	TDI	N7	TDI	5	TDI		
T8	PB4C	2	T	T8	PB5C	5	T	T8	PB6A	5	T		
T7	PB4D	2	C	T7	PB5D	5	C	T7	PB6B	5	C		
M7	NC			M7	PB6A	5	T	M7	PB7C	5	T		
M8	NC			M8	PB6B	5	C	M8	PB7D	5	C		
T9	VCCAUX	-		T9	VCCAUX	-		T9	VCCAUX	-			
R7	PB4E	2	T	R7	PB6C	5	T	R7	PB8C	5	T		
R8	PB4F	2	C	R8	PB6D	5	C	R8	PB8D	5	C		
-	-			VCCIO5	VCCIO5	5		VCCIO5	VCCIO5	5			
-	-			GND	GNDIO5	5		GND	GNDIO5	5			
P7	PB5C	2	T	P7	PB6E	5	T	P7	PB9A	4	T		
P8	PB5D	2	C	P8	PB6F	5	C	P8	PB9B	4	C		
N8	PB5A	2	T	N8	PB7A	4	T	N8	PB10E	4	T		
N9	PB5B	2	PCLK2_1***	C	N9	PB7B	4	PCLK4_1***	C	N9	PB10F	4	PCLK4_1***
P10	PB7B	2	C	P10	PB7D	4	C	P10	PB10D	4	C		
P9	PB7A	2	T	P9	PB7C	4	T	P9	PB10C	4	T		
M9	PB6B	2	PCLK2_0***	C	M9	PB7F	4	PCLK4_0***	C	M9	PB10B	4	PCLK4_0***

**LCMxo640, LCMxo1200 and LCMxo2280 Logic Signal Connections:
 256 caBGA / 256 ftBGA (Cont.)**

LCMxo640					LCMxo1200					LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
-	-				VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
-	-				GND	GNDIO4	4			GND	GNDIO4	4		
M10	PB6A	2		T	M10	PB7E	4			M10	PB10A	4		T
R9	PB6C	2		T	R9	PB8A	4			R9	PB11C	4		T
R10	PB6D	2		C	R10	PB8B	4			R10	PB11D	4		C
T10	PB7C	2		T	T10	PB8C	4			T10	PB12A	4		T
T11	PB7D	2		C	T11	PB8D	4			T11	PB12B	4		C
N10	NC				N10	PB8E	4			N10	PB12C	4		T
N11	NC				N11	PB8F	4			N11	PB12D	4		C
VCCIO2	VCCIO2	2			VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
GND	GNDIO2	2			GND	GNDIO4	4			GND	GNDIO4	4		
R11	PB7E	2		T	R11	PB9A	4			R11	PB13A	4		T
R12	PB7F	2		C	R12	PB9B	4			R12	PB13B	4		C
P11	PB8A	2		T	P11	PB9C	4			P11	PB13C	4		T
P12	PB8B	2		C	P12	PB9D	4			P12	PB13D	4		C
T13	PB8C	2		T	T13	PB9E	4			T13	PB14A	4		T
T12	PB8D	2		C	T12	PB9F	4			T12	PB14B	4		C
R13	PB9A	2		T	R13	PB10A	4			R13	PB14C	4		T
R14	PB9B	2		C	R14	PB10B	4			R14	PB14D	4		C
GND	GND	-			GND	GND	-			GND	GND	-		
T14	PB9C	2		T	T14	PB10C	4			T14	PB15A	4		T
T15	PB9D	2		C	T15	PB10D	4			T15	PB15B	4		C
P13**	SLEEPN	-	SLEEPN		P13**	SLEEPN	-	SLEEPN		P13**	SLEEPN	-	SLEEPN	
P14	PB9F	2			P14	PB10F	4			P14	PB15D	4		
R15	NC				R15	PB11A	4			R15	PB16A	4		T
R16	NC				R16	PB11B	4			R16	PB16B	4		C
P15	NC				P15	PB11C	4			P15	PB16C	4		T
P16	NC				P16	PB11D	4			P16	PB16D	4		C
VCCIO2	VCCIO2	2			VCCIO4	VCCIO4	4			VCCIO4	VCCIO4	4		
GND	GNDIO2	2			GND	GNDIO4	4			GND	GNDIO4	4		
GND	GNDIO1	1			GND	GNDIO3	3			GND	GNDIO3	3		
VCCIO1	VCCIO1	1			VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
M11	NC				M11	PR16B	3			M11	PR20B	3		C
L11	NC				L11	PR16A	3			L11	PR20A	3		T
N12	NC				N12	PR15B	3			N12	PR18B	3		C*
N13	NC				N13	PR15A	3			N13	PR18A	3		T*
M13	NC				M13	PR14D	3			M13	PR17D	3		C
M12	NC				M12	PR14C	3			M12	PR17C	3		T
N14	PR11D	1		C	N14	PR14B	3			N14	PR17B	3		C*
N15	PR11C	1		T	N15	PR14A	3			N15	PR17A	3		T*
L13	PR11B	1		C	L13	PR13D	3			L13	PR16D	3		C
L12	PR11A	1		T	L12	PR13C	3			L12	PR16C	3		T
M14	PR10B	1		C	M14	PR13B	3			M14	PR16B	3		C*
VCCIO1	VCCIO1	1			VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
GND	GNDIO1	1			GND	GNDIO3	3			GND	GNDIO3	3		
L14	PR10A	1		T	L14	PR13A	3			L14	PR16A	3		T*
N16	PR10D	1		C	N16	PR12D	3			N16	PR15D	3		C
M16	PR10C	1		T	M16	PR12C	3			M16	PR15C	3		T
M15	PR9D	1		C	M15	PR12B	3			M15	PR15B	3		C*
L15	PR9C	1		T	L15	PR12A	3			L15	PR15A	3		T*
L16	PR9B	1		C	L16	PR11D	3			L16	PR14D	3		C
K16	PR9A	1		T	K16	PR11C	3			K16	PR14C	3		T
K13	PR8D	1		C	K13	PR11B	3			K13	PR14B	3		C*

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G2	PL11A	6		T*
H2	PL11B	6		C*
L3	PL11C	6		T
L5	PL11D	6		C
H1	PL12A	6		T*
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
J2	PL12B	6		C*
L4	PL12C	6		T
L6	PL12D	6		C
K2	PL13A	6		T*
K1	PL13B	6		C*
J1	PL13C	6		T
VCC	VCC	-		
L2	PL13D	6		C
M5	PL14D	6		C
M3	PL14C	6	TSALL	T
L1	PL14B	6		C*
M2	PL14A	6		T*
M1	PL15A	6		T*
N1	PL15B	6		C*
M6	PL15C	6		T
M4	PL15D	6		C
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
P1	PL16A	6		T*
P2	PL16B	6		C*
N3	PL16C	6		T
N4	PL16D	6		C
GND	GND	-		
T1	PL17A	6	LLM0_PLLT_FB_A	T*
R1	PL17B	6	LLM0_PLLC_FB_A	C*
P3	PL17C	6		T
N5	PL17D	6		C
R3	PL18A	6	LLM0_PLLT_IN_A	T*
R2	PL18B	6	LLM0_PLLC_IN_A	C*
P4	PL19A	6		T
N6	PL19B	6		C
U1	PL20A	6		T
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		

LCMxo2280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMxo2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G8	VCCIO0	0		
G7	VCCIO0	0		

* Supports true LVDS outputs.

** NC for "E" devices.

*** Primary clock inputs are single-ended.

Conventional Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3T100C	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	COM
LCMxo256C-4T100C	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	COM
LCMxo256C-5T100C	256	1.8V/2.5V/3.3V	78	-5	TQFP	100	COM
LCMxo256C-3M100C	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	COM
LCMxo256C-4M100C	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	COM
LCMxo256C-5M100C	256	1.8V/2.5V/3.3V	78	-5	csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3T100C	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	COM
LCMxo640C-4T100C	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	COM
LCMxo640C-5T100C	640	1.8V/2.5V/3.3V	74	-5	TQFP	100	COM
LCMxo640C-3M100C	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	COM
LCMxo640C-4M100C	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	COM
LCMxo640C-5M100C	640	1.8V/2.5V/3.3V	74	-5	csBGA	100	COM
LCMxo640C-3T144C	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMxo640C-4T144C	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMxo640C-5T144C	640	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMxo640C-3M132C	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMxo640C-4M132C	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMxo640C-5M132C	640	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMxo640C-3B256C	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	COM
LCMxo640C-4B256C	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	COM
LCMxo640C-5B256C	640	1.8V/2.5V/3.3V	159	-5	caBGA	256	COM
LCMxo640C-3FT256C	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	COM
LCMxo640C-4FT256C	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	COM
LCMxo640C-5FT256C	640	1.8V/2.5V/3.3V	159	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3T100C	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	COM
LCMxo1200C-4T100C	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	COM
LCMxo1200C-5T100C	1200	1.8V/2.5V/3.3V	73	-5	TQFP	100	COM
LCMxo1200C-3T144C	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	COM
LCMxo1200C-4T144C	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	COM
LCMxo1200C-5T144C	1200	1.8V/2.5V/3.3V	113	-5	TQFP	144	COM
LCMxo1200C-3M132C	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	COM
LCMxo1200C-4M132C	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	COM
LCMxo1200C-5M132C	1200	1.8V/2.5V/3.3V	101	-5	csBGA	132	COM
LCMxo1200C-3B256C	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	COM
LCMxo1200C-4B256C	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	COM
LCMxo1200C-5B256C	1200	1.8V/2.5V/3.3V	211	-5	caBGA	256	COM
LCMxo1200C-3FT256C	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	COM
LCMxo1200C-4FT256C	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	COM
LCMxo1200C-5FT256C	1200	1.8V/2.5V/3.3V	211	-5	ftBGA	256	COM

Conventional Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3T100I	256	1.8V/2.5V/3.3V	78	-3	TQFP	100	IND
LCMxo256C-4T100I	256	1.8V/2.5V/3.3V	78	-4	TQFP	100	IND
LCMxo256C-3M100I	256	1.8V/2.5V/3.3V	78	-3	csBGA	100	IND
LCMxo256C-4M100I	256	1.8V/2.5V/3.3V	78	-4	csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3T100I	640	1.8V/2.5V/3.3V	74	-3	TQFP	100	IND
LCMxo640C-4T100I	640	1.8V/2.5V/3.3V	74	-4	TQFP	100	IND
LCMxo640C-3M100I	640	1.8V/2.5V/3.3V	74	-3	csBGA	100	IND
LCMxo640C-4M100I	640	1.8V/2.5V/3.3V	74	-4	csBGA	100	IND
LCMxo640C-3T144I	640	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo640C-4T144I	640	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo640C-3M132I	640	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo640C-4M132I	640	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo640C-3B256I	640	1.8V/2.5V/3.3V	159	-3	caBGA	256	IND
LCMxo640C-4B256I	640	1.8V/2.5V/3.3V	159	-4	caBGA	256	IND
LCMxo640C-3FT256I	640	1.8V/2.5V/3.3V	159	-3	ftBGA	256	IND
LCMxo640C-4FT256I	640	1.8V/2.5V/3.3V	159	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3T100I	1200	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo1200C-4T100I	1200	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo1200C-3T144I	1200	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo1200C-4T144I	1200	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo1200C-3M132I	1200	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo1200C-4M132I	1200	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo1200C-3B256I	1200	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo1200C-4B256I	1200	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo1200C-3FT256I	1200	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo1200C-4FT256I	1200	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo2280C-3T100I	2280	1.8V/2.5V/3.3V	73	-3	TQFP	100	IND
LCMxo2280C-4T100I	2280	1.8V/2.5V/3.3V	73	-4	TQFP	100	IND
LCMxo2280C-3T144I	2280	1.8V/2.5V/3.3V	113	-3	TQFP	144	IND
LCMxo2280C-4T144I	2280	1.8V/2.5V/3.3V	113	-4	TQFP	144	IND
LCMxo2280C-3M132I	2280	1.8V/2.5V/3.3V	101	-3	csBGA	132	IND
LCMxo2280C-4M132I	2280	1.8V/2.5V/3.3V	101	-4	csBGA	132	IND
LCMxo2280C-3B256I	2280	1.8V/2.5V/3.3V	211	-3	caBGA	256	IND
LCMxo2280C-4B256I	2280	1.8V/2.5V/3.3V	211	-4	caBGA	256	IND
LCMxo2280C-3FT256I	2280	1.8V/2.5V/3.3V	211	-3	ftBGA	256	IND
LCMxo2280C-4FT256I	2280	1.8V/2.5V/3.3V	211	-4	ftBGA	256	IND
LCMxo2280C-3FT324I	2280	1.8V/2.5V/3.3V	271	-3	ftBGA	324	IND
LCMxo2280C-4FT324I	2280	1.8V/2.5V/3.3V	271	-4	ftBGA	324	IND

Lead-Free Packaging
Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo256C-3TN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	COM
LCMxo256C-4TN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	COM
LCMxo256C-5TN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free TQFP	100	COM
LCMxo256C-3MN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	COM
LCMxo256C-4MN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	COM
LCMxo256C-5MN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo640C-3TN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	COM
LCMxo640C-4TN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	COM
LCMxo640C-5TN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free TQFP	100	COM
LCMxo640C-3MN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	COM
LCMxo640C-4MN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	COM
LCMxo640C-5MN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free csBGA	100	COM
LCMxo640C-3TN144C	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMxo640C-4TN144C	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMxo640C-5TN144C	640	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMxo640C-3MN132C	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMxo640C-4MN132C	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMxo640C-5MN132C	640	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMxo640C-3BN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	COM
LCMxo640C-4BN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	COM
LCMxo640C-5BN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free caBGA	256	COM
LCMxo640C-3FTN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	COM
LCMxo640C-4FTN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	COM
LCMxo640C-5FTN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMxo1200C-3TN100C	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMxo1200C-4TN100C	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMxo1200C-5TN100C	1200	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMxo1200C-3TN144C	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMxo1200C-4TN144C	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMxo1200C-5TN144C	1200	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMxo1200C-3MN132C	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMxo1200C-4MN132C	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMxo1200C-5MN132C	1200	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMxo1200C-3BN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMxo1200C-4BN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMxo1200C-5BN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMxo1200C-3FTN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMxo1200C-4FTN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMxo1200C-5FTN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM