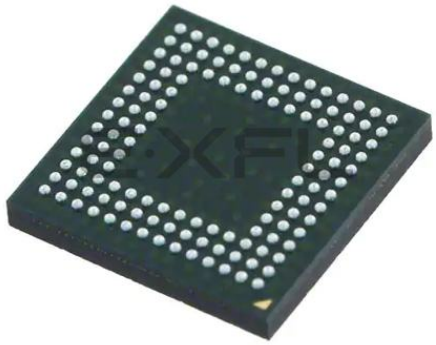

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

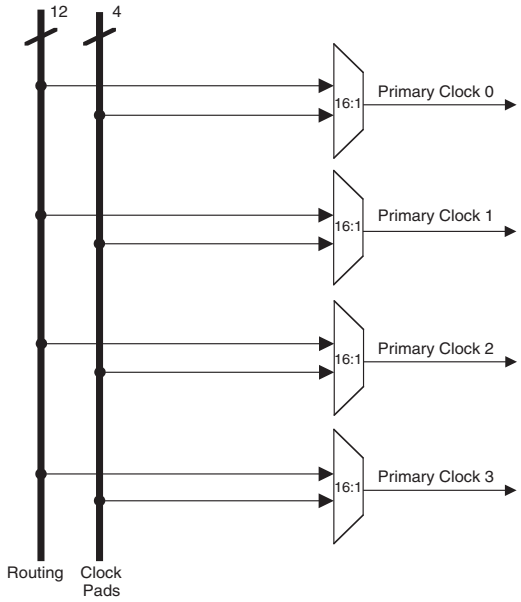
| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 80 |
| Number of Logic Elements/Cells | 640 |
| Total RAM Bits | - |
| Number of I/O | 101 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 132-LFBGA, CSPBGA |
| Supplier Device Package | 132-CSPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo640e-3m132i |

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

***Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices***



## sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

***Figure 2-10. PLL Diagram***

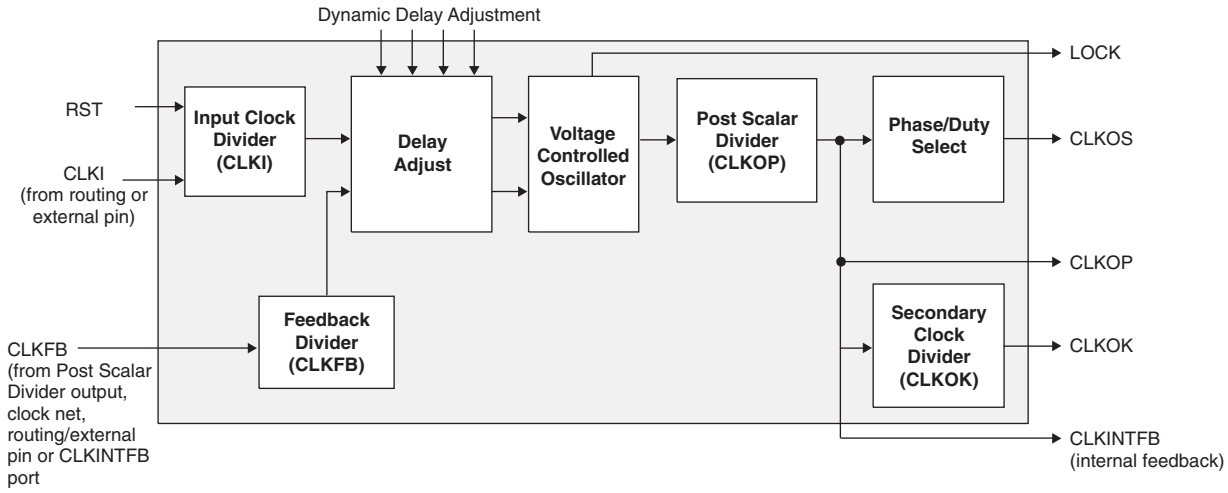
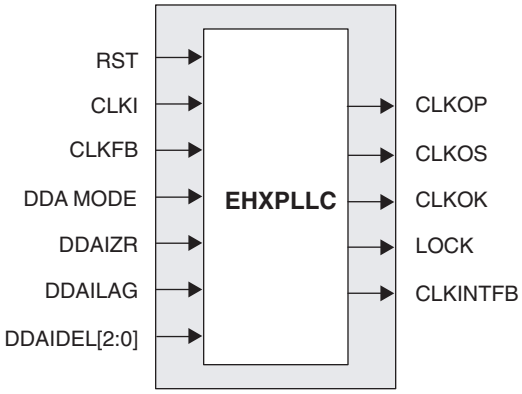



Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

***Figure 2-11. PLL Primitive***



### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

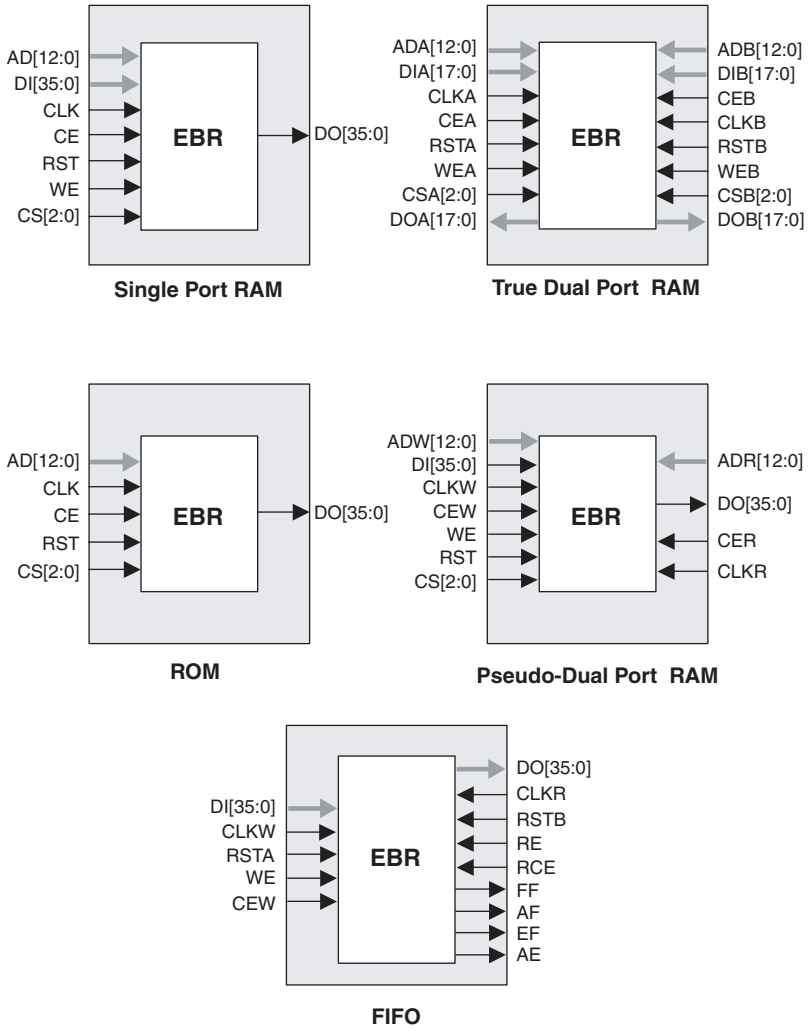
### Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

### Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-12 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

***Figure 2-12. sysMEM Memory Primitives***

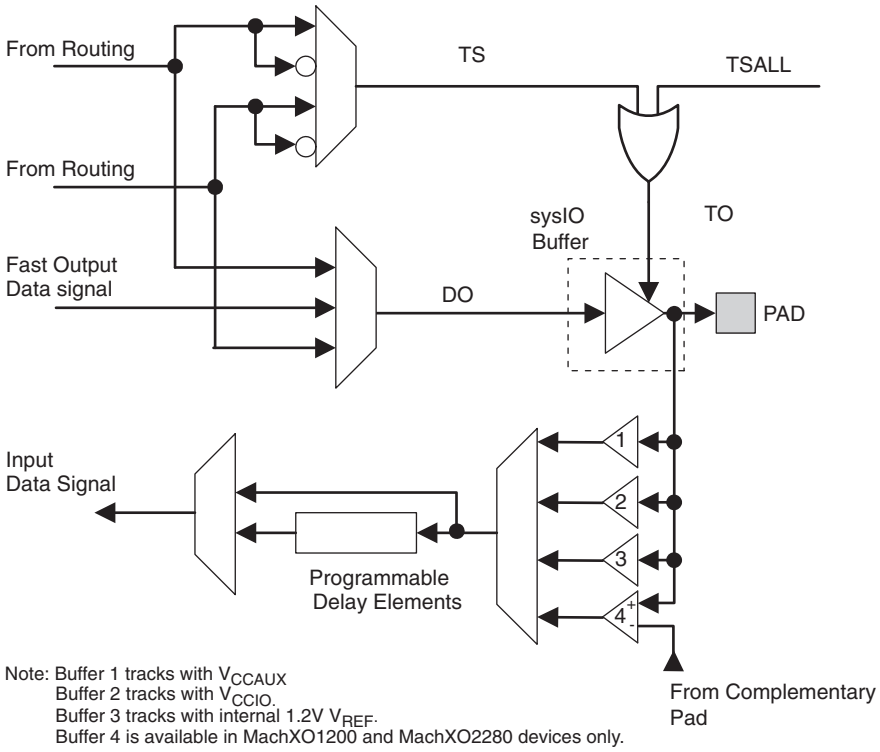


output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 2-17 shows the MachXO PIO logic.

The tristate control signal is multiplexed from the output data signals and their complements. In addition a global signal (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the device. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

***Figure 2-17. MachXO PIO Block Diagram***




## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the MachXO devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using $V_{CCIO}$. In addition to the Bank $V_{CCIO}$ supplies, the MachXO devices have a $V_{CC}$ core logic power supply, and a $V_{CCAUX}$ supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

MachXO256 and MachXO640 devices contain single-ended input buffers and single-ended output buffers with complementary outputs on all the I/O Banks.

MachXO1200 and MachXO2280 devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the top and bottom Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom

the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

## Sleep Mode

The MachXO "C" devices ($V_{CC}$ = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

***Table 2-11. Characteristics of Normal, Off and Sleep Modes***

| Characteristic | Normal | Off | Sleep |
|---|---|---|---|
| SLEEPN Pin | High | — | Low |
| Static Icc | Typical <10mA | 0 | Typical <100uA |
| I/O Leakage | <10µA | <1mA | <10µA |
| Power Supplies VCC/VCCIO/VCCAUX | Normal Range | 0 | Normal Range |
| Logic Operation | User Defined | Non Operational | Non operational |
| I/O Operation | User Defined | Tri-state | Tri-state |
| JTAG and Programming circuitry | Operational | Non-operational | Non-operational |
| EBR Contents and Registers | Maintained | Non-maintained | Non-maintained |

### SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

## Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

## Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: $V_{CCIO1}$; MachXO640: $V_{CCIO2}$; MachXO1200 and MachXO2280: $V_{CCIO5}$) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ (V) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.465 |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 |
| LVTTL | 3.135 | 3.3 | 3.465 |
| PCI[3] | 3.135 | 3.3 | 3.465 |
| LVDS[1, 2] | 2.375 | 2.5 | 2.625 |
| LVPECL[1] | 3.135 | 3.3 | 3.465 |
| BLVDS[1] | 2.375 | 2.5 | 2.625 |
| RSDS[1] | 2.375 | 2.5 | 2.625 |

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers
3. Input on the top bank of the MachXO1200 and MachXO2280 only.

## sysIO Single-Ended DC Electrical Characteristics

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -14, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 16 | -16 |
| | | | | | 0.4 | $V_{CCIO}$ - 0.4 | 12, 8, 4 | -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -14, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -14, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.5 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8, 4 | -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 (“C” Version) | -0.3 | 0.42 | 0.78 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 (“E” Version) | -0.3 | $0.35V_{CC}$ | $0.65V_{CC}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| PCI | -0.3 | $0.3V_{CCIO}$ | $0.5V_{CCIO}$ | 3.6 | $0.1V_{CCIO}$ | $0.9V_{CCIO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

*Table 3-2. BLVDS DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | Ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ohms |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

## LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

*Figure 3-3. Differential LVPECL*

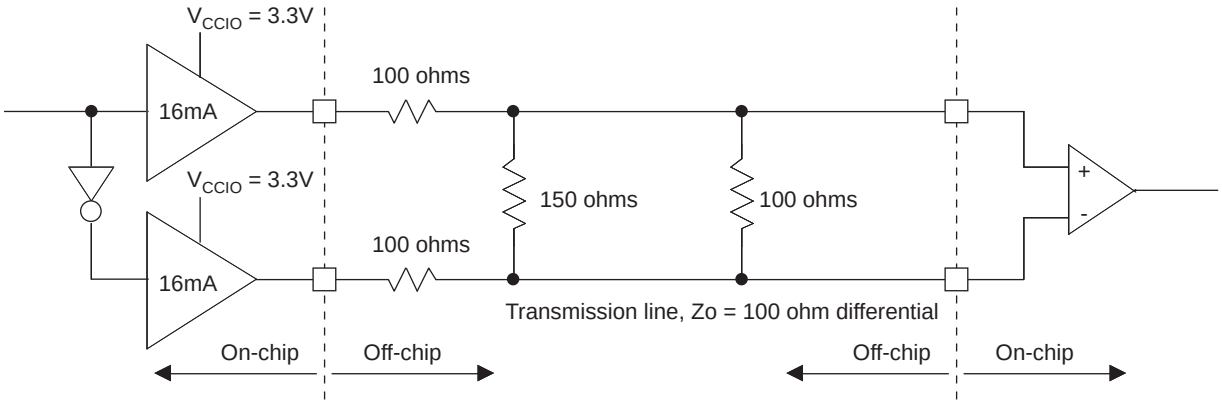



*Table 3-3. LVPECL DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | Ohms |
| $R_P$ | Driver parallel resistor | 150 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | Ohms |
| $I_{DC}$ | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

# MachXO External Switching Characteristics[1]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (Using Global Clock without PLL)[1]** | | | | | | | | | |
| $t_{PD}$ | Best Case $t_{PD}$ Through 1 LUT | LCMXO256 | — | 3.5 | — | 4.2 | — | 4.9 | ns |
| | | LCMXO640 | — | 3.5 | — | 4.2 | — | 4.9 | ns |
| | | LCMXO1200 | — | 3.6 | — | 4.4 | — | 5.1 | ns |
| | | LCMXO2280 | — | 3.6 | — | 4.4 | — | 5.1 | ns |
| $t_{CO}$ | Best Case Clock to Output - From PFU | LCMXO256 | — | 4.0 | — | 4.8 | — | 5.6 | ns |
| | | LCMXO640 | — | 4.0 | — | 4.8 | — | 5.7 | ns |
| | | LCMXO1200 | — | 4.3 | — | 5.2 | — | 6.1 | ns |
| | | LCMXO2280 | — | 4.3 | — | 5.2 | — | 6.1 | ns |
| $t_{SU}$ | Clock to Data Setup - To PFU | LCMXO256 | 1.3 | — | 1.6 | — | 1.8 | — | ns |
| | | LCMXO640 | 1.1 | — | 1.3 | — | 1.5 | — | ns |
| | | LCMXO1200 | 1.1 | — | 1.3 | — | 1.6 | — | ns |
| | | LCMXO2280 | 1.1 | — | 1.3 | — | 1.5 | — | ns |
| $t_{H}$ | Clock to Data Hold - To PFU | LCMXO256 | -0.3 | — | -0.3 | — | -0.3 | — | ns |
| | | LCMXO640 | -0.1 | — | -0.1 | — | -0.1 | — | ns |
| | | LCMXO1200 | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| | | LCMXO2280 | -0.4 | — | -0.4 | — | -0.4 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | LCMXO256 | — | 600 | — | 550 | — | 500 | MHz |
| | | LCMXO640 | — | 600 | — | 550 | — | 500 | MHz |
| | | LCMXO1200 | — | 600 | — | 550 | — | 500 | MHz |
| | | LCMXO2280 | — | 600 | — | 550 | — | 500 | MHz |
| $t_{SKEW\_PRI}$ | Global Clock Skew Across Device | LCMXO256 | — | 200 | — | 220 | — | 240 | ps |
| | | LCMXO640 | — | 200 | — | 220 | — | 240 | ps |
| | | LCMXO1200 | — | 220 | — | 240 | — | 260 | ps |
| | | LCMXO2280 | — | 220 | — | 240 | — | 260 | ps |

1. General timing numbers based on LVCMOS2.5V, 12 mA.

# sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 25 | 420 | MHz |
| | | Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6] | 18 | 25 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | | 25 | 420 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency (CLKOK) | | 0.195 | 210 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 420 | 840 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 25 | — | MHz |
| | | Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6] | 18 | 25 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default duty cycle selected[3] | 45 | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | — | 0.05 | UI |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | $f_{OUT}$ >= 100 MHz | — | +/-120 | ps |
| | | $f_{OUT}$ < 100 MHz | — | 0.02 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | Divider ratio = integer | — | +/-200 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%[3] | 1 | — | ns |
| $t_{LOCK}$[2] | PLL Lock-in Time | | — | 150 | µs |
| $t_{PA}$ | Programmable Delay Unit | | 100 | 450 | ps |
| $t_{IPJIT}$ | Input Clock Period Jitter | $f_{OUT} \geq$ 100 MHz | — | +/-200 | ps |
| | | $f_{OUT}$ < 100 MHz | — | 0.02 | UI |
| $t_{FBKDLY}$ | External Feedback Delay | | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | ns |
| $t_{RST}$ | RST Pulse Width | | 10 | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output.
5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.
6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.

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## Switching Test Conditions

Figure 3-6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

***Figure 3-6. Output Test Load, LVTTL and LVCMOS Standards***

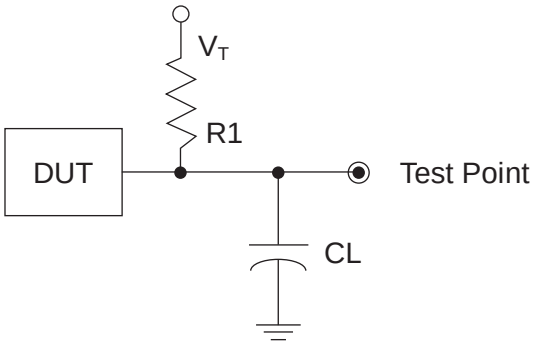


***Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|
| LVTTL and LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVTTL, LVCMOS 3.3 = 1.5V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVTTL and LVCMOS 3.3 (Z -> H) | 188 | 0pF | 1.5 | $V_{OL}$ |
| LVTTL and LVCMOS 3.3 (Z -> L) | | | | $V_{OH}$ |
| Other LVCMOS (Z -> H) | | | $V_{CCIO}/2$ | $V_{OL}$ |
| Other LVCMOS (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVTTL + LVCMOS (H -> Z) | | | $V_{OH}$ - 0.15 | $V_{OL}$ |
| LVTTL + LVCMOS (L -> Z) | | | $V_{OL}$ - 0.15 | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

# Pin Information Summary

| Pin Type | | LCMXO256C/E | | LCMXO640C/E | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 100 csBGA | 100 TQFP | 144 TQFP | 100 csBGA | 132 csBGA | 256 caBGA / 256 ftBGA |
| Single Ended User I/O | | 78 | 78 | 74 | 113 | 74 | 101 | 159 |
| Differential Pair User I/O[1] | | 38 | 38 | 17 | 43 | 17 | 42 | 79 |
| Muxed | | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| TAP | | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Dedicated (Total Without Supplies) | | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| VCC | | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| VCCAUX | | 1 | 1 | 1 | 2 | 1 | 2 | 2 |
| VCCIO | Bank0 | 3 | 3 | 2 | 2 | 2 | 2 | 4 |
| | Bank1 | 3 | 3 | 2 | 2 | 2 | 2 | 4 |
| | Bank2 | — | — | 2 | 2 | 2 | 2 | 4 |
| | Bank3 | — | — | 2 | 2 | 2 | 2 | 4 |
| GND | | 8 | 8 | 10 | 12 | 10 | 12 | 18 |
| NC | | 0 | 0 | 0 | 0 | 0 | 0 | 52 |
| Single Ended/Differential I/O per Bank | Bank0 | 41/20 | 41/20 | 18/5 | 29/10 | 18/5 | 26/11 | 42/21 |
| | Bank1 | 37/18 | 37/18 | 21/4 | 30/11 | 21/4 | 27/12 | 40/20 |
| | Bank2 | — | — | 14/2 | 24/9 | 14/2 | 21/9 | 36/18 |
| | Bank3 | — | — | 21/6 | 30/13 | 21/6 | 27/10 | 40/20 |

1. These devices support emulated LVDS outputs.þLVDS inputs are not supported.

| Pin Type | | LCMXO1200C/E | | | | LCMXO2280C/E | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 144 TQFP | 132 csBGA | 256 caBGA / 256 ftBGA | 100 TQFP | 144 TQFP | 132 csBGA | 256 caBGA / 256 ftBGA | 324 ftBGA |
| Single Ended User I/O | | 73 | 113 | 101 | 211 | 73 | 113 | 101 | 211 | 271 |
| Differential Pair User I/O[1] | | 27 | 48 | 42 | 105 | 30 | 47 | 41 | 105 | 134 |
| Muxed | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| TAP | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Dedicated (Total Without Supplies) | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| VCC | | 4 | 4 | 4 | 4 | 2 | 4 | 4 | 4 | 6 |
| VCCAUX | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| VCCIO | Bank0 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank2 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank3 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank4 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank5 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank6 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| | Bank7 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| GND | | 8 | 12 | 12 | 18 | 8 | 12 | 12 | 18 | 24 |
| NC | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Single Ended/Differential I/O per Bank | Bank0 | 10/3 | 14/6 | 13/5 | 26/13 | 9/3 | 13/6 | 12/5 | 24/12 | 34/17 |
| | Bank1 | 8/2 | 15/7 | 13/5 | 28/14 | 9/3 | 16/7 | 14/5 | 30/15 | 36/18 |
| | Bank2 | 10/4 | 15/7 | 13/6 | 26/13 | 10/4 | 15/7 | 13/6 | 26/13 | 34/17 |
| | Bank3 | 11/5 | 15/7 | 14/7 | 28/14 | 11/5 | 15/7 | 14/7 | 28/14 | 34/17 |
| | Bank4 | 8/3 | 14/5 | 13/5 | 27/13 | 8/3 | 14/4 | 13/4 | 29/14 | 35/17 |
| | Bank5 | 5/2 | 10/4 | 8/2 | 22/11 | 5/2 | 10/4 | 8/2 | 20/10 | 30/15 |
| | Bank6 | 10/3 | 15/6 | 13/6 | 28/14 | 10/4 | 15/6 | 13/6 | 28/14 | 34/17 |
| | Bank7 | 11/5 | 15/6 | 14/6 | 26/13 | 11/5 | 15/6 | 14/6 | 26/13 | 34/17 |

1. These devices support on-chip LVDS buffers for left and right I/O Banks.

## LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP

| Pin Number | LCMXO256 | | | | LCMXO640 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 1 | PL2A | 1 | | T | PL2A | 3 | | T |
| 2 | PL2B | 1 | | C | PL2C | 3 | | T |
| 3 | PL3A | 1 | | T | PL2B | 3 | | C |
| 4 | PL3B | 1 | | C | PL2D | 3 | | C |
| 5 | PL3C | 1 | | T | PL3A | 3 | | T |
| 6 | PL3D | 1 | | C | PL3B | 3 | | C |
| 7 | PL4A | 1 | | T | PL3C | 3 | | T |
| 8 | PL4B | 1 | | C | PL3D | 3 | | C |
| 9 | PL5A | 1 | | T | PL4A | 3 | | |
| 10 | VCCIO1 | 1 | | | VCCIO3 | 3 | | |
| 11 | PL5B | 1 | | C | PL4C | 3 | | T |
| 12 | GNDIO1 | 1 | | | GNDIO3 | 3 | | |
| 13 | PL5C | 1 | | T | PL4D | 3 | | C |
| 14 | PL5D | 1 | GSRN | C | PL5B | 3 | GSRN | |
| 15 | PL6A | 1 | | T | PL7B | 3 | | |
| 16 | PL6B | 1 | TSALL | C | PL8C | 3 | TSALL | T |
| 17 | PL7A | 1 | | T | PL8D | 3 | | C |
| 18 | PL7B | 1 | | C | PL9A | 3 | | |
| 19 | PL7C | 1 | | T | PL9C | 3 | | |
| 20 | PL7D | 1 | | C | PL10A | 3 | | |
| 21 | PL8A | 1 | | T | PL10C | 3 | | |
| 22 | PL8B | 1 | | C | PL11A | 3 | | |
| 23 | PL9A | 1 | | T | PL11C | 3 | | |
| 24 | VCCIO1 | 1 | | | VCCIO3 | 3 | | |
| 25 | GNDIO1 | 1 | | | GNDIO3 | 3 | | |
| 26 | TMS | 1 | TMS | | TMS | 2 | TMS | |
| 27 | PL9B | 1 | | C | PB2C | 2 | | |
| 28 | TCK | 1 | TCK | | TCK | 2 | TCK | |
| 29 | PB2A | 1 | | T | VCCIO2 | 2 | | |
| 30 | PB2B | 1 | | C | GNDIO2 | 2 | | |
| 31 | TDO | 1 | TDO | | TDO | 2 | TDO | |
| 32 | PB2C | 1 | | T | PB4C | 2 | | |
| 33 | TDI | 1 | TDI | | TDI | 2 | TDI | |
| 34 | PB2D | 1 | | C | PB4E | 2 | | |
| 35 | VCC | - | | | VCC | - | | |
| 36 | PB3A | 1 | PCLK1_1** | T | PB5B | 2 | PCLK2_1** | |
| 37 | PB3B | 1 | | C | PB5D | 2 | | |
| 38 | PB3C | 1 | PCLK1_0** | T | PB6B | 2 | PCLK2_0** | |
| 39 | PB3D | 1 | | C | PB6C | 2 | | |
| 40 | GND | - | | | GND | - | | |
| 41 | VCCIO1 | 1 | | | VCCIO2 | 2 | | |
| 42 | GNDIO1 | 1 | | | GNDIO2 | 2 | | |

# LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

| LCMXO640 | | | | | LCMXO1200 | | | | | LCMXO2280 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball # | Ball Function | Bank | Dual Function | Differential | Ball # | Ball Function | Bank | Dual Function | Differential | Ball # | Ball Function | Bank | Dual Function | Differential |
| B9 | PT7B | 0 | | C | B9 | PT9B | 1 | | C | B9 | PT12D | 1 | | C |
| A9 | PT7A | 0 | | T | A9 | PT9A | 1 | | T | A9 | PT12C | 1 | | T |
| A8 | PT6B | 0 | PCLK0_1*** | C | A8 | PT7D | 1 | PCLK1_1*** | | A8 | PT10B | 1 | PCLK1_1*** | |
| B8 | PT6A | 0 | | T | B8 | PT7B | 1 | | | B8 | PT9D | 1 | | |
| C8 | PT5B | 0 | PCLK0_0*** | C | C8 | PT6F | 0 | PCLK1_0*** | | C8 | PT9B | 1 | PCLK1_0*** | |
| B7 | PT5A | 0 | | T | B7 | PT6D | 0 | | | B7 | PT8D | 0 | | |
| A7 | VCCAUX | - | | | A7 | VCCAUX | - | | | A7 | VCCAUX | - | | |
| C7 | VCC | - | | | C7 | VCC | - | | | C7 | VCC | - | | |
| A6 | PT4D | 0 | | C | A6 | PT5D | 0 | | C | A6 | PT7B | 0 | | C |
| B6 | PT4C | 0 | | T | B6 | PT5C | 0 | | T | B6 | PT7A | 0 | | T |
| C6 | PT3F | 0 | | C | C6 | PT5B | 0 | | C | C6 | PT6D | 0 | | |
| B5 | PT3E | 0 | | T | B5 | PT5A | 0 | | T | B5 | PT6E | 0 | | T |
| A5 | PT3D | 0 | | | A5 | PT4B | 0 | | | A5 | PT6F | 0 | | C |
| B4 | GNDIO0 | 0 | | | B4 | GNDIO0 | 0 | | | B4 | GNDIO0 | 0 | | |
| A4 | PT3B | 0 | | | A4 | PT3D | 0 | | C | A4 | PT4B | 0 | | C |
| C4 | PT2F | 0 | | | C4 | PT3C | 0 | | T | C4 | PT4A | 0 | | T |
| A3 | PT2D | 0 | | C | A3 | PT3B | 0 | | C | A3 | PT3B | 0 | | C |
| A2 | PT2C | 0 | | T | A2 | PT2B | 0 | | C | A2 | PT2B | 0 | | C |
| B3 | PT2B | 0 | | C | B3 | PT3A | 0 | | T | B3 | PT3A | 0 | | T |
| A1 | PT2A | 0 | | T | A1 | PT2A | 0 | | T | A1 | PT2A | 0 | | T |
| F1 | GND | - | | | F1 | GND | - | | | F1 | GND | - | | |
| P9 | GND | - | | | P9 | GND | - | | | P9 | GND | - | | |
| J14 | GND | - | | | J14 | GND | - | | | J14 | GND | - | | |
| C9 | GND | - | | | C9 | GND | - | | | C9 | GND | - | | |
| C5 | VCCIO0 | 0 | | | C5 | VCCIO0 | 0 | | | C5 | VCCIO0 | 0 | | |
| B11 | VCCIO0 | 0 | | | B11 | VCCIO1 | 1 | | | B11 | VCCIO1 | 1 | | |
| E12 | VCCIO1 | 1 | | | E12 | VCCIO2 | 2 | | | E12 | VCCIO2 | 2 | | |
| L12 | VCCIO1 | 1 | | | L12 | VCCIO3 | 3 | | | L12 | VCCIO3 | 3 | | |
| M10 | VCCIO2 | 2 | | | M10 | VCCIO4 | 4 | | | M10 | VCCIO4 | 4 | | |
| N2 | VCCIO2 | 2 | | | N2 | VCCIO5 | 5 | | | N2 | VCCIO5 | 5 | | |
| D2 | VCCIO3 | 3 | | | D2 | VCCIO7 | 7 | | | D2 | VCCIO7 | 7 | | |
| K3 | VCCIO3 | 3 | | | K3 | VCCIO6 | 6 | | | K3 | VCCIO6 | 6 | | |

*Supports true LVDS outputs.
**NC for “E” devices.
***Primary clock inputs arer single-ended.

## LCMXO2280 Logic Signal Connections: 324 ftBGA

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| GND | GNDIO7 | 7 | | |
| VCCIO7 | VCCIO7 | 7 | | |
| D4 | PL2A | 7 | LUM0_PLLT_FB_A | T |
| F5 | PL2B | 7 | LUM0_PLLC_FB_A | C |
| B3 | PL3A | 7 | | T* |
| C3 | PL3B | 7 | | C* |
| E4 | PL3C | 7 | LUM0_PLLT_IN_A | T |
| G6 | PL3D | 7 | LUM0_PLLC_IN_A | C |
| A1 | PL4A | 7 | | T* |
| B1 | PL4B | 7 | | C* |
| F4 | PL4C | 7 | | T |
| VCC | VCC | - | | |
| E3 | PL4D | 7 | | C |
| D2 | PL5A | 7 | | T* |
| D3 | PL5B | 7 | | C* |
| G5 | PL5C | 7 | | T |
| F3 | PL5D | 7 | | C |
| C2 | PL6A | 7 | | T* |
| VCCIO7 | VCCIO7 | 7 | | |
| GND | GNDIO7 | 7 | | |
| C1 | PL6B | 7 | | C* |
| H5 | PL6C | 7 | | T |
| G4 | PL6D | 7 | | C |
| E2 | PL7A | 7 | | T* |
| D1 | PL7B | 7 | GSRN | C* |
| J6 | PL7C | 7 | | T |
| H4 | PL7D | 7 | | C |
| F2 | PL8A | 7 | | T* |
| E1 | PL8B | 7 | | C* |
| GND | GND | - | | |
| J3 | PL8C | 7 | | T |
| J5 | PL8D | 7 | | C |
| G3 | PL9A | 7 | | T* |
| H3 | PL9B | 7 | | C* |
| K3 | PL9C | 7 | | T |
| K5 | PL9D | 7 | | C |
| F1 | PL10A | 7 | | T* |
| VCCIO7 | VCCIO7 | 7 | | |
| GND | GNDIO7 | 7 | | |
| G1 | PL10B | 7 | | C* |
| K4 | PL10C | 7 | | T |
| K6 | PL10D | 7 | | C |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| T2 | PL20B | 6 | | C |
| P6 | TMS | 5 | TMS | |
| V1 | PB2A | 5 | | T |
| U2 | PB2B | 5 | | C |
| T3 | PB2C | 5 | | T |
| N7 | TCK | 5 | TCK | |
| R4 | PB2D | 5 | | C |
| R5 | PB3A | 5 | | T |
| T4 | PB3B | 5 | | C |
| VCC | VCC | - | | |
| R6 | PB3C | 5 | | T |
| P7 | PB3D | 5 | | C |
| U3 | PB4A | 5 | | T |
| T5 | PB4B | 5 | | C |
| V2 | PB4C | 5 | | T |
| N8 | TDO | 5 | TDO | |
| V3 | PB4D | 5 | | C |
| T6 | PB5A | 5 | | T |
| GND | GNDIO5 | 5 | | |
| VCCIO5 | VCCIO5 | 5 | | |
| U4 | PB5B | 5 | | C |
| P8 | PB5C | 5 | | T |
| T7 | PB5D | 5 | | C |
| V4 | TDI | 5 | TDI | |
| R8 | PB6A | 5 | | T |
| N9 | PB6B | 5 | | C |
| U5 | PB6C | 5 | | T |
| V5 | PB6D | 5 | | C |
| U6 | PB7A | 5 | | T |
| VCC | VCC | - | | |
| V6 | PB7B | 5 | | C |
| P9 | PB7C | 5 | | T |
| T8 | PB7D | 5 | | C |
| U7 | PB8A | 5 | | T |
| V7 | PB8B | 5 | | C |
| M10 | VCCAUX | - | | |
| U8 | PB8C | 5 | | T |
| V8 | PB8D | 5 | | C |
| VCCIO5 | VCCIO5 | 5 | | |
| GND | GNDIO5 | 5 | | |
| T9 | PB8E | 5 | | T |
| U9 | PB8F | 5 | | C |
| V9 | PB9A | 4 | | T |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| A10 | PT8E | 0 | | T |
| VCCIO0 | VCCIO0 | 0 | | |
| GND | GNDIO0 | 0 | | |
| A9 | PT8D | 0 | | C |
| C9 | PT8C | 0 | | T |
| B9 | PT8B | 0 | | C |
| F9 | VCCAUX | - | | |
| A8 | PT8A | 0 | | T |
| B8 | PT7D | 0 | | C |
| C8 | PT7C | 0 | | T |
| VCC | VCC | - | | |
| A7 | PT7B | 0 | | C |
| B7 | PT7A | 0 | | T |
| A6 | PT6A | 0 | | T |
| B6 | PT6B | 0 | | C |
| D8 | PT6C | 0 | | T |
| F8 | PT6D | 0 | | C |
| C7 | PT6E | 0 | | T |
| E8 | PT6F | 0 | | C |
| D7 | PT5D | 0 | | C |
| VCCIO0 | VCCIO0 | 0 | | |
| GND | GNDIO0 | 0 | | |
| E7 | PT5C | 0 | | T |
| A5 | PT5B | 0 | | C |
| C6 | PT5A | 0 | | T |
| B5 | PT4A | 0 | | T |
| A4 | PT4B | 0 | | C |
| D6 | PT4C | 0 | | T |
| F7 | PT4D | 0 | | C |
| B4 | PT4E | 0 | | T |
| GND | GND | - | | |
| C5 | PT4F | 0 | | C |
| F6 | PT3D | 0 | | C |
| E5 | PT3C | 0 | | T |
| E6 | PT3B | 0 | | C |
| D5 | PT3A | 0 | | T |
| A3 | PT2D | 0 | | C |
| C4 | PT2C | 0 | | T |
| A2 | PT2B | 0 | | C |
| B2 | PT2A | 0 | | T |
| VCCIO0 | VCCIO0 | 0 | | |
| GND | GNDIO0 | 0 | | |
| E14 | GND | - | | |

## LCMXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LCMXO2280 | | | | |
|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Dual Function | Differential |
| F16 | GND | - | | |
| H10 | GND | - | | |
| H11 | GND | - | | |
| H8 | GND | - | | |
| H9 | GND | - | | |
| J10 | GND | - | | |
| J11 | GND | - | | |
| J4 | GND | - | | |
| J8 | GND | - | | |
| J9 | GND | - | | |
| K10 | GND | - | | |
| K11 | GND | - | | |
| K17 | GND | - | | |
| K8 | GND | - | | |
| K9 | GND | - | | |
| L10 | GND | - | | |
| L11 | GND | - | | |
| L8 | GND | - | | |
| L9 | GND | - | | |
| N2 | GND | - | | |
| P14 | GND | - | | |
| P5 | GND | - | | |
| R7 | GND | - | | |
| F14 | VCC | - | | |
| G11 | VCC | - | | |
| G9 | VCC | - | | |
| H7 | VCC | - | | |
| L7 | VCC | - | | |
| M9 | VCC | - | | |
| H6 | VCCIO7 | 7 | | |
| J7 | VCCIO7 | 7 | | |
| M7 | VCCIO6 | 6 | | |
| K7 | VCCIO6 | 6 | | |
| M8 | VCCIO5 | 5 | | |
| R9 | VCCIO5 | 5 | | |
| M12 | VCCIO4 | 4 | | |
| M11 | VCCIO4 | 4 | | |
| L12 | VCCIO3 | 3 | | |
| K12 | VCCIO3 | 3 | | |
| J12 | VCCIO2 | 2 | | |
| H12 | VCCIO2 | 2 | | |
| G12 | VCCIO1 | 1 | | |
| G10 | VCCIO1 | 1 | | |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200E-3TN100C | 1200 | 1.2V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO1200E-4TN100C | 1200 | 1.2V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO1200E-5TN100C | 1200 | 1.2V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO1200E-3TN144C | 1200 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO1200E-4TN144C | 1200 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO1200E-5TN144C | 1200 | 1.2V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO1200E-3MN132C | 1200 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO1200E-4MN132C | 1200 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO1200E-5MN132C | 1200 | 1.2V | 101 | -5 | Lead-Free csBGA | 132 | COM |
| LCMXO1200E-3BN256C | 1200 | 1.2V | 211 | -3 | Lead-Free caBGA | 256 | COM |
| LCMXO1200E-4BN256C | 1200 | 1.2V | 211 | -4 | Lead-Free caBGA | 256 | COM |
| LCMXO1200E-5BN256C | 1200 | 1.2V | 211 | -5 | Lead-Free caBGA | 256 | COM |
| LCMXO1200E-3FTN256C | 1200 | 1.2V | 211 | -3 | Lead-Free ftBGA | 256 | COM |
| LCMXO1200E-4FTN256C | 1200 | 1.2V | 211 | -4 | Lead-Free ftBGA | 256 | COM |
| LCMXO1200E-5FTN256C | 1200 | 1.2V | 211 | -5 | Lead-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280E-3TN100C | 2280 | 1.2V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO2280E-4TN100C | 2280 | 1.2V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO2280E-5TN100C | 2280 | 1.2V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO2280E-3TN144C | 2280 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO2280E-4TN144C | 2280 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO2280E-5TN144C | 2280 | 1.2V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO2280E-3MN132C | 2280 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO2280E-4MN132C | 2280 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO2280E-5MN132C | 2280 | 1.2V | 101 | -5 | Lead-Free csBGA | 132 | COM |
| LCMXO2280E-3BN256C | 2280 | 1.2V | 211 | -3 | Lead-Free caBGA | 256 | COM |
| LCMXO2280E-4BN256C | 2280 | 1.2V | 211 | -4 | Lead-Free caBGA | 256 | COM |
| LCMXO2280E-5BN256C | 2280 | 1.2V | 211 | -5 | Lead-Free caBGA | 256 | COM |
| LCMXO2280E-3FTN256C | 2280 | 1.2V | 211 | -3 | Lead-Free ftBGA | 256 | COM |
| LCMXO2280E-4FTN256C | 2280 | 1.2V | 211 | -4 | Lead-Free ftBGA | 256 | COM |
| LCMXO2280E-5FTN256C | 2280 | 1.2V | 211 | -5 | Lead-Free ftBGA | 256 | COM |
| LCMXO2280E-3FTN324C | 2280 | 1.2V | 271 | -3 | Lead-Free ftBGA | 324 | COM |
| LCMXO2280E-4FTN324C | 2280 | 1.2V | 271 | -4 | Lead-Free ftBGA | 324 | COM |
| LCMXO2280E-5FTN324C | 2280 | 1.2V | 271 | -5 | Lead-Free ftBGA | 324 | COM |

# MachXO Family Data Sheet Revision History



## Revision History

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2005 | 01.0 | — | Initial release. |
| October 2005 | 01.1 | Introduction | Distributed RAM information in family table updated. Added footnote 1 - fpBGA packaging to the family selection guide. |
| | | Architecture | sysIO Buffer section updated. |
| | | | Hot Socketing section updated. |
| | | | Sleep Mode section updated. |
| | | | SLEEP Pin Characteristics section updated. |
| | | | Oscillator section updated. |
| | | | Security section updated. |
| | | DC and Switching Characteristics | Recommended Operating Conditions table updated. |
| | | | DC Electrical Characteristics table updated. |
| | | | Supply Current (Sleep Mode) table added with LCMXO256/640 data. |
| | | | Supply Current (Standby) table updated with LCMXO256/640 data. |
| | | | Initialization Supply Current table updated with LCMXO256/640 data. |
| | | | Programming and Erase Flash Supply Current table updated with LCMXO256/640 data. |
| | | | Register-to-Register Performance table updated (rev. A 0.16). |
| | | | External Switching Characteristics table updated (rev. A 0.16). |
| | | | Internal Timing Parameter table updated (rev. A 0.16). |
| | | | Family Timing Adders updated (rev. A 0.16). |
| | | | sysCLOCK Timingupdated (rev. A 0.16). |
| | | | MachXO "C" Sleep Mode Timing updated (A 0.16). |
| | | | JTAG Port Timing Specification updated (rev. A 0.16). |
| | | Pinout Information | SLEEPIN description updated. |
| | | | Pin Information Summary updated. |
| | | | Power Supply and NC Connection table has been updated. |
| | | | Logic Signal Connection section has been updated to include all devices/packages. |
| | | Ordering Information | Part Number Description section has been updated. |
| | | | Ordering Part Number section has been updated (added LCMXO256C/ LCMXO640C "4W"). |
| | | Supplemental Information | MachXO Density Migration Technical Note (TN1097) added. |
| November 2005 | 01.2 | Pinout Information | Added “Power Supply and NC Connections” summary information for LCMXO1200 and LCMXO2280 in 100 TQFP package. |
| December 2005 | 01.3 | DC and Switching Characteristics | Supply Current (Standby) table updated with LCMXO1200/2280 data. |
| | | Ordering Information | Ordering Part Number section updated (added LCMXO2280C "4W"). |
| April 2006 | 02.0 | Introduction | Introduction paragraphs updated. |
| | | Architecture | Architecture Overview paragraphs updated. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| April 2006 (cont.) | 02.0 (cont.) | Architecture (cont.) | "Top View of the MachXO1200 Device" figure updated. |
| | | | "Top View of the MachXO640 Device" figure updated. |
| | | | "Top View of the MachXO256 Device" figure updated. |
| | | | "Slice Diagram" figure updated. |
| | | | Slice Signal Descriptions table updated. |
| | | | Routing section updated. |
| | | | sysCLOCK Phase Lockecd Loops (PLLs) section updated. |
| | | | PLL Diagram updated. |
| | | | PLL Signal Descriptions table updated. |
| | | | sysMEM Memory section has been updated. |
| | | | PIO Groups section has been updated. |
| | | | PIO section has been updated. |
| | | | MachXO PIO Block Diagram updated. |
| | | | Supported Input Standards table updated. |
| | | | MachXO Configuration and Programming diagram updated. |
| | | DC and Switching Characteristics | Recommended Operating Conditions table - footnotes updated. |
| | | | MachXO256 and MachXO640 Hot Socketing Specifications - footnotes updated. |
| | | | Added MachXO1200 and MachXO2280 Hot Socketing Specifications table. |
| | | | DC Electrical Characteristics, footnotes have been updated. |
| | | | Supply Current (Sleep Mode) table has been updated, removed "4W" references. Footnotes have been updated. |
| | | | Supply Current (Standby) table and associated footnotes updated. |
| | | | Intialization Supply Current table and footnotes updated. |
| | | | Programming and Erase Flash Supply Current table and associated footnotes have been updatd. |
| | | | Register-to-Register Performance table updated (rev. A 0.19). |
| | | | MachXO External Switching Characteristics updated (rev. A 0.19). |
| | | | MachXO Internal Timing Parameters updated (rev. A 0.19). |
| | | | MachXO Family Timing Adders updated (rev. A 0.19). |
| | | | sysCLOCK Timing updated (rev. A 0.19). |
| | | | MachXO "C" Sleep Mode Timing updated (A 0.19). |
| | | | JTAG Port Timing Specification updated (rev. A 0.19). |
| | | | Test Fixture Required Components table updated. |
| | | Pinout Information | Signal Descriptions have been updated. |
| | | | Pin Information Summary has been updated. Footnote has been added. |
| | | | Power Supply and NC Connection table has been updated. |
| | | | Logic Signal Connections have been updated (PCLKTx_x --> PCLKx_x) |
| | | Ordering Information | Removed "4W" references. |
| | | | Added 256-ftBGA Ordering Part Numbers for MachXO640. |
| May 2006 | 02.1 | Pinout Information | Removed [LOC][0]_PLL_RST from Signal Description table. |
| | | | PCLK footnote has been added to all appropriate pins. |
| August 2006 | 02.2 | Multiple | Removed 256 fpBGA information for MachXO640. |