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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

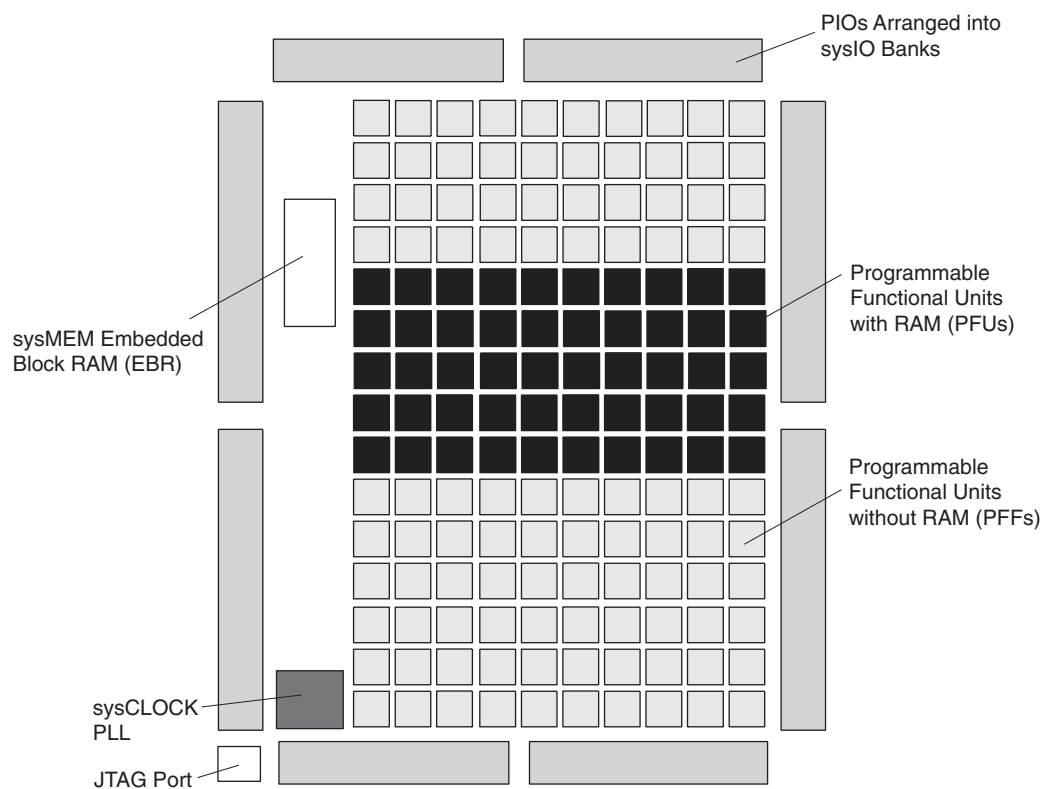
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	-
Number of I/O	74
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo640e-4tn100c

Figure 2-1. Top View of the MachXO1200 Device¹



1. Top view of the MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the MachXO640 Device

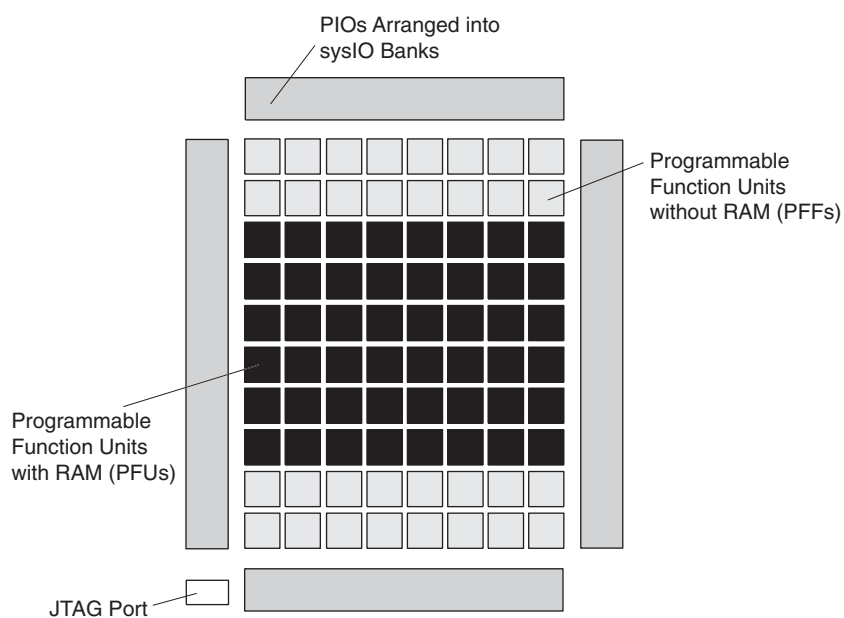
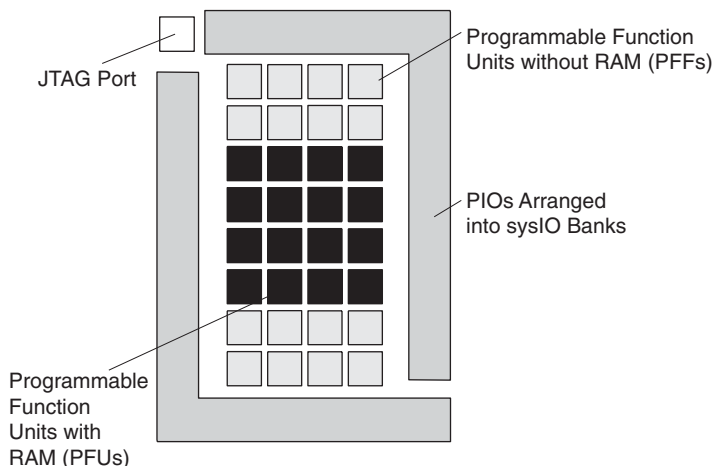


Figure 2-3. Top View of the MachXO256 Device

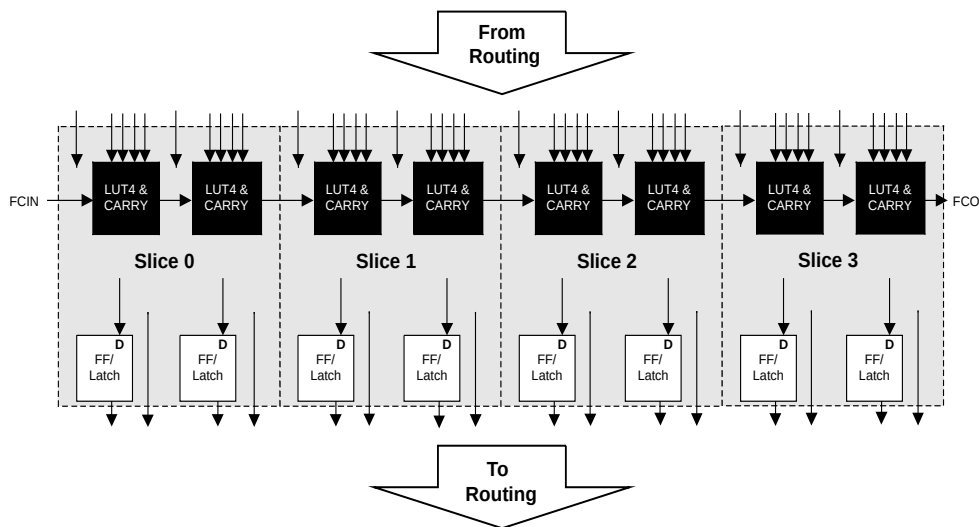


PFU Blocks

The core of the MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected Slices, numbered 0-3 as shown in Figure 2-4. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-4. PFU Diagram



Slice

Each Slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 2-5 shows an overview of the internal logic of the Slice. The registers in the Slice can be configured for positive/negative and edge/level clocks.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-10. PLL Diagram

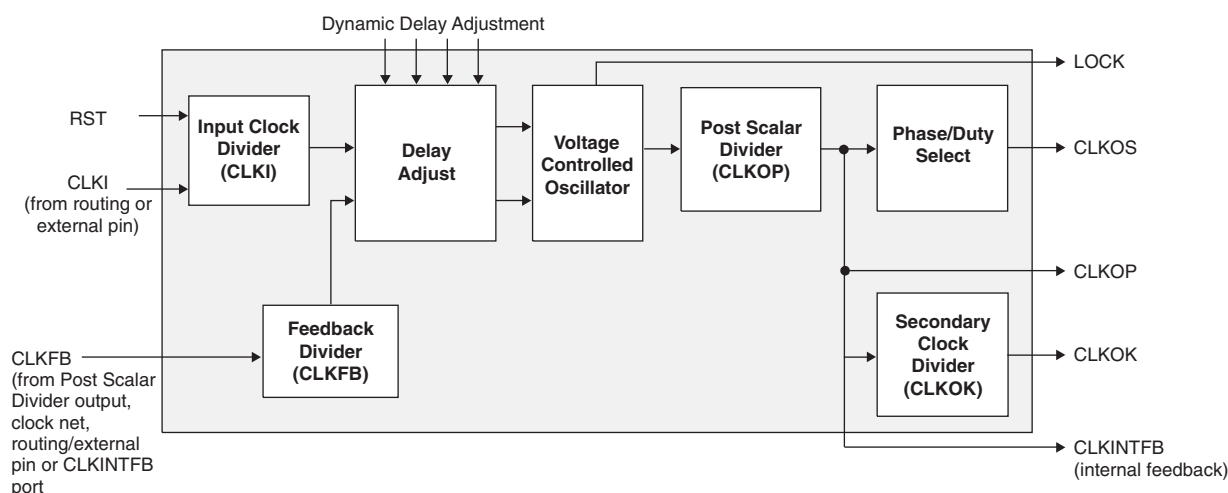
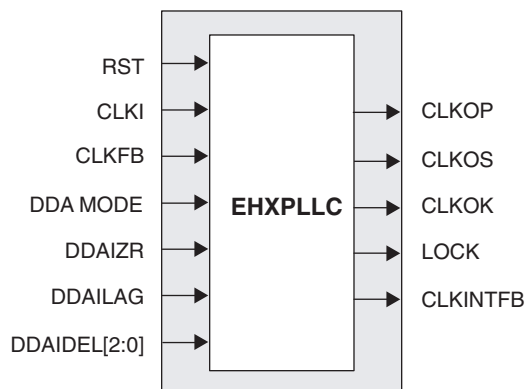


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive



The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

FIFO Configuration

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2-7.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

Figure 2-20. MachXO640 Banks

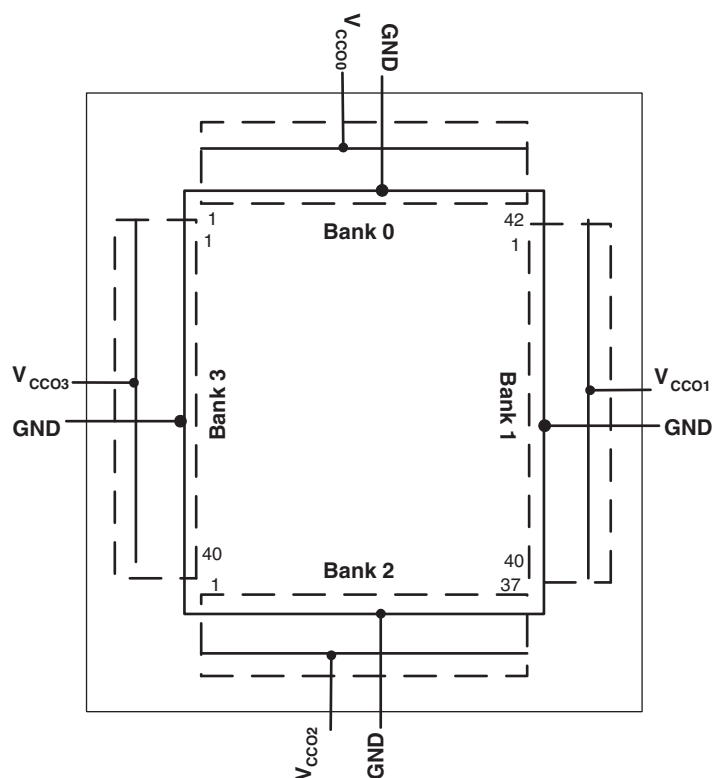
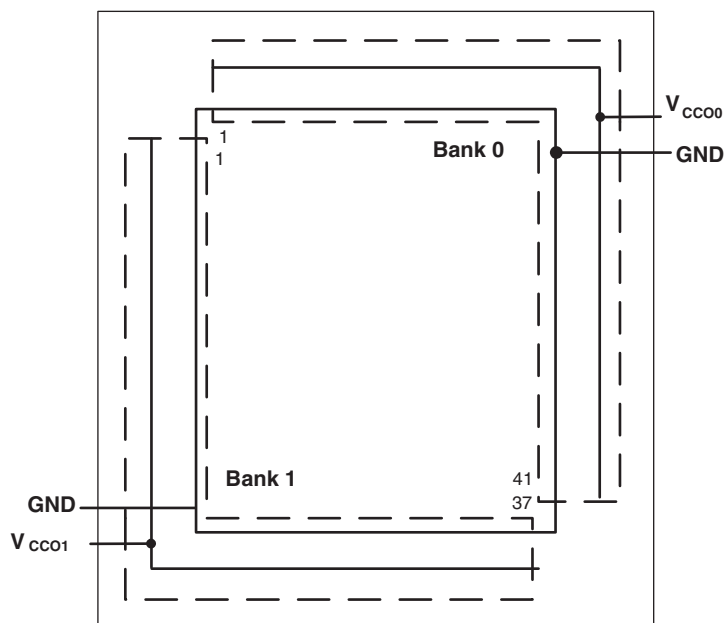


Figure 2-21. MachXO256 Banks



Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of

MachXO256 and MachXO640 Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	+/-1000	μA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} , and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} , and V_{CCIO} .
2. $0 \leq V_{CC} \leq V_{CC} (MAX)$, $0 \leq V_{CCIO} \leq V_{CCIO} (MAX)$ and $0 \leq V_{CCAUX} \leq V_{CCAUX} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

MachXO1200 and MachXO2280 Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Non-LVDS General Purpose sysIOs						
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH} (MAX.)$	—	—	+/-1000	μA
LVDS General Purpose sysIOs						
I_{DK_LVDS}	Input or I/O Leakage Current	$V_{IN} \leq V_{CCIO}$	—	—	+/-1000	μA
		$V_{IN} > V_{CCIO}$	—	35	—	mA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} , and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} , and V_{CCIO} .
2. $0 \leq V_{CC} \leq V_{CC} (MAX)$, $0 \leq V_{CCIO} \leq V_{CCIO} (MAX)$, and $0 \leq V_{CCAUX} \leq V_{CCAUX} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL} , I_{IH} ^{1, 4, 5}	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	μA
V_{BHT} ³	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = Typ.$, $V_{IO} = 0$ to $V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = Typ.$, $V_{IO} = 0$ to $V_{IH} (MAX)$	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A = 25^\circ C$, $f = 1.0MHz$
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Not applicable to SLEEPN pin.
5. When V_{IH} is higher than V_{CCIO} , a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For MachXO1200 and MachXO2280 true LVDS output pins, V_{IH} must be less than or equal to V_{CCIO} .

Table 3-2. BLVDS DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Z _o = 45	Z _o = 90	
Z _{OUT}	Output impedance	100	100	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

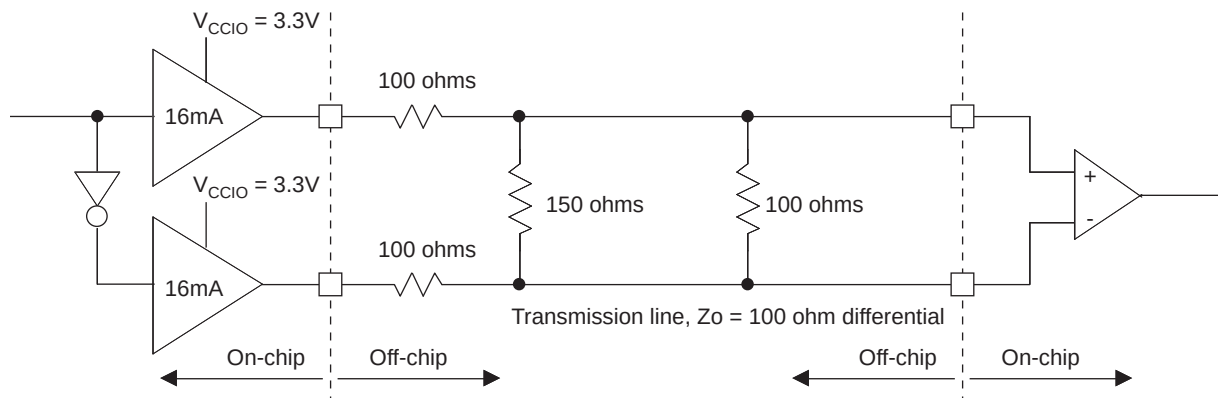


Table 3-3. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	100	Ohms
R _P	Driver parallel resistor	150	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	2.03	V
V _{OL}	Output low voltage	1.27	V
V _{OD}	Output differential voltage	0.76	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	85.7	Ohms
I _{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.7	ns
4:1 MUX	4.5	ns
16:1 MUX	5.1	ns

Register-to-Register Performance

Function	-5 Timing	Units
Basic Functions		
16:1 MUX	487	MHz
16-bit adder	292	MHz
16-bit counter	388	MHz
64-bit counter	200	MHz
Embedded Memory Functions (1200 and 2280 Devices Only)		
256x36 Single Port RAM	284	MHz
512x18 True-Dual Port RAM	284	MHz
Distributed Memory Functions		
16x2 Single Port RAM	434	MHz
64x2 Single Port RAM	320	MHz
128x4 Single Port RAM	261	MHz
32x2 Pseudo-Dual Port RAM	314	MHz
64x4 Pseudo-Dual Port RAM	271	MHz

1. The above timing numbers are generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Rev. A 0.19

Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays may be much faster. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4 ^{5, 6}	18	25	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f _{VCO}	PLL VCO Frequency		420	840	MHz
f _{PFD}	Phase Detector Input Frequency		25	—	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4 ^{5, 6}	18	25	MHz
AC Characteristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	55	%
t _{PH} ⁴	Output Phase Accuracy		—	0.05	UI
t _{OPJIT} ¹	Output Clock Period Jitter	f _{OUT} >= 100 MHz	—	+/-120	ps
		f _{OUT} < 100 MHz	—	0.02	UIPP
t _{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	1	—	ns
t _{LOCK} ²	PLL Lock-in Time		—	150	μs
t _{PA}	Programmable Delay Unit		100	450	ps
t _{IPJIT}	Input Clock Period Jitter	f _{OUT} ≥ 100 MHz	—	+/-200	ps
		f _{OUT} < 100 MHz	—	0.02	UI
t _{FBKDLY}	External Feedback Delay		—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t _{RST}	RST Pulse Width		10	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output.

5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.

6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.

Rev. A 0.19

LCMX01200 and LCMX02280 Logic Signal Connections: 100 TQFP

Pin Number	LCMX01200				LCMX02280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
4	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
5	PL4B	7			PL4B	7		
6	VCCIO7	7			VCCIO7	7		
7	PL6A	7		T*	PL7A	7		T*
8	PL6B	7	GSRN	C*	PL7B	7	GSRN	C*
9	GND	-			GND	-		
10	PL7C	7		T	PL9C	7		T
11	PL7D	7		C	PL9D	7		C
12	PL8C	7		T	PL10C	7		T
13	PL8D	7		C	PL10D	7		C
14	PL9C	6			PL11C	6		
15	PL10A	6		T*	PL13A	6		T*
16	PL10B	6		C*	PL13B	6		C*
17	VCC	-			VCC	-		
18	PL11B	6			PL14D	6		C
19	PL11C	6	TSALL		PL14C	6	TSALL	T
20	VCCIO6	6			VCCIO6	6		
21	PL13C	6			PL16C	6		
22	PL14A	6	LLM0_PLLT_FB_A	T*	PL17A	6	LLM0_PLLT_FB_A	T*
23	PL14B	6	LLM0_PLLC_FB_A	C*	PL17B	6	LLM0_PLLC_FB_A	C*
24	PL15A	6	LLM0_PLLT_IN_A	T*	PL18A	6	LLM0_PLLT_IN_A	T*
25	PL15B	6	LLM0_PLLC_IN_A	C*	PL18B	6	LLM0_PLLC_IN_A	C*
26**	GNDIO6 GNDIO5	-			GNDIO6 GNDIO5	-		
27	VCCIO5	5			VCCIO5	5		
28	TMS	5	TMS		TMS	5	TMS	
29	TCK	5	TCK		TCK	5	TCK	
30	PB3B	5			PB3B	5		
31	PB4A	5		T	PB4A	5		T
32	PB4B	5		C	PB4B	5		C
33	TDO	5	TDO		TDO	5	TDO	
34	TDI	5	TDI		TDI	5	TDI	
35	VCC	-			VCC	-		
36	VCCAUX	-			VCCAUX	-		
37	PB6E	5		T	PB8E	5		T
38	PB6F	5		C	PB8F	5		C
39	PB7B	4	PCLK4_1****		PB10F	4	PCLK4_1****	
40	PB7F	4	PCLK4_0****		PB10B	4	PCLK4_0****	
41	GND	-			GND	-		

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1***	C	A8	PT7D	1	PCLK1_1***		A8	PT10B	1	PCLK1_1***	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0***	C	C8	PT6F	0	PCLK1_0***		C8	PT9B	1	PCLK1_0***	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	-			A7	VCCAUX	-			A7	VCCAUX	-		
C7	VCC	-			C7	VCC	-			C7	VCC	-		
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	-			F1	GND	-			F1	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
C9	GND	-			C9	GND	-			C9	GND	-		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
101	PR3D	1		C	PR4B	2		C*	PR5B	2		C*
102	PR3C	1		T	PR4A	2		T*	PR5A	2		T*
103	PR3B	1		C	PR3D	2		C	PR4D	2		C
104	PR2D	1		C	PR3C	2		T	PR4C	2		T
105	PR3A	1		T	PR3B	2		C*	PR4B	2		C*
106	PR2B	1		C	PR3A	2		T*	PR4A	2		T*
107	PR2C	1		T	PR2B	2		C	PR3B	2		C*
108	PR2A	1		T	PR2A	2		T	PR3A	2		T*
109	PT9F	0		C	PT11D	1		C	PT16D	1		C
110	PT9D	0		C	PT11C	1		T	PT16C	1		T
111	PT9E	0		T	PT11B	1		C	PT16B	1		C
112	PT9B	0		C	PT11A	1		T	PT16A	1		T
113	PT9C	0		T	PT10F	1		C	PT15D	1		C
114	PT9A	0		T	PT10E	1		T	PT15C	1		T
115	PT8C	0			PT10D	1		C	PT14B	1		C
116	PT8B	0		C	PT10C	1		T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1			VCCIO1	1		
118	GNDIO0	0			GNDIO1	1			GNDIO1	1		
119	PT8A	0		T	PT9F	1		C	PT12F	1		C
120	PT7E	0			PT9E	1		T	PT12E	1		T
121	PT7C	0			PT9B	1		C	PT12D	1		C
122	PT7A	0			PT9A	1		T	PT12C	1		T
123	GND	-			GND	-			GND	-		
124	PT6B	0	PCLK0_1***	C	PT7D	1	PCLK1_1***		PT10B	1	PCLK1_1***	
125	PT6A	0		T	PT7B	1		C	PT9D	1		C
126	PT5C	0			PT7A	1		T	PT9C	1		T
127	PT5B	0	PCLK0_0***		PT6F	0	PCLK1_0***		PT9B	1	PCLK1_0***	
128	VCCAUX	-			VCCAUX	-			VCCAUX	-		
129	VCC	-			VCC	-			VCC	-		
130	PT4D	0			PT5D	0		C	PT7B	0		C
131	PT4B	0		C	PT5C	0		T	PT7A	0		T
132	PT4A	0		T	PT5B	0		C	PT6D	0		
133	PT3F	0			PT5A	0		T	PT6E	0		T
134	PT3D	0			PT4B	0			PT6F	0		C
135	VCCIO0	0			VCCIO0	0			VCCIO0	0		
136	GNDIO0	0			GNDIO0	0			GNDIO0	0		
137	PT3B	0		C	PT3D	0		C	PT4B	0		T
138	PT2F	0		C	PT3C	0		T	PT4A	0		C
139	PT3A	0		T	PT3B	0		C	PT3B	0		C
140	PT2D	0		C	PT3A	0		T	PT3A	0		T
141	PT2E	0		T	PT2D	0		C	PT2D	0		C
142	PT2B	0		C	PT2C	0		T	PT2C	0		T
143	PT2C	0		T	PT2B	0		C	PT2B	0		C
144	PT2A	0		T	PT2A	0		T	PT2A	0		T

*Supports true LVDS outputs.

**NC for "E" devices.

***Primary clock inputs are single-ended.

LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA (Cont.)

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR8C	1		T	J13	PR11A	3		T*	J13	PR14A	3		T*
GND	GND	-			GND	GND	-			GND	GND	-		
K14	PR8B	1		C	K14	PR10D	3		C	K14	PR13D	3		C
J14	PR8A	1		T	J14	PR10C	3		T	J14	PR13C	3		T
K15	PR7D	1		C	K15	PR10B	3		C*	K15	PR13B	3		C*
J15	PR7C	1		T	J15	PR10A	3		T*	J15	PR13A	3		T*
-	-				GND	GNDIO3	3			GND	GNDIO3	3		
-	-				VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
K12	NC				K12	PR9D	3		C	K12	PR11D	3		C
J12	NC				J12	PR9C	3		T	J12	PR11C	3		T
J16	PR7B	1		C	J16	PR9B	3		C*	J16	PR11B	3		C*
H16	PR7A	1		T	H16	PR9A	3		T*	H16	PR11A	3		T*
H15	PR6B	1		C	H15	PR8D	2		C	H15	PR10D	2		C
G15	PR6A	1		T	G15	PR8C	2		T	G15	PR10C	2		T
H14	PR5D	1		C	H14	PR8B	2		C*	H14	PR10B	2		C*
G14	PR5C	1		T	G14	PR8A	2		T*	G14	PR10A	2		T*
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
H13	PR6D	1		C	H13	PR7D	2		C	H13	PR9D	2		C
H12	PR6C	1		T	H12	PR7C	2		T	H12	PR9C	2		T
G13	PR4D	1		C	G13	PR7B	2		C*	G13	PR9B	2		C*
G12	PR4C	1		T	G12	PR7A	2		T*	G12	PR9A	2		T*
G16	PR5B	1		C	G16	PR6D	2		C	G16	PR7D	2		C
F16	PR5A	1		T	F16	PR6C	2		T	F16	PR7C	2		T
F15	PR4B	1		C	F15	PR6B	2		C*	F15	PR7B	2		C*
E15	PR4A	1		T	E15	PR6A	2		T*	E15	PR7A	2		T*
E16	PR3B	1		C	E16	PR5D	2		C	E16	PR6D	2		C
D16	PR3A	1		T	D16	PR5C	2		T	D16	PR6C	2		T
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
D15	PR2D	1		C	D15	PR5B	2		C*	D15	PR6B	2		C*
C15	PR2C	1		T	C15	PR5A	2		T*	C15	PR6A	2		T*
C16	PR2B	1		C	C16	PR4D	2		C	C16	PR5D	2		C
B16	PR2A	1		T	B16	PR4C	2		T	B16	PR5C	2		T
F14	PR3D	1		C	F14	PR4B	2		C*	F14	PR5B	2		C*
E14	PR3C	1		T	E14	PR4A	2		T*	E14	PR5A	2		T*
-	-	-			-	-	-			GND	GND	-		
F12	NC				F12	PR3D	2		C	F12	PR4D	2		C
F13	NC				F13	PR3C	2		T	F13	PR4C	2		T
E12	NC				E12	PR3B	2		C*	E12	PR4B	2		C*
E13	NC				E13	PR3A	2		T*	E13	PR4A	2		T*
D13	NC				D13	PR2B	2		C	D13	PR3B	2		C*
D14	NC				D14	PR2A	2		T	D14	PR3A	2		T*
VCCIO0	VCCIO0	0			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO0	0			GND	GNDIO2	2			GND	GNDIO2	2		
GND	GNDIO0	0			GND	GNDIO1	1			GND	GNDIO1	1		
VCCIO0	VCCIO0	0			VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
B15	NC				B15	PT11D	1		C	B15	PT16D	1		C
A15	NC				A15	PT11C	1		T	A15	PT16C	1		T
C14	NC				C14	PT11B	1		C	C14	PT16B	1		C
B14	NC				B14	PT11A	1		T	B14	PT16A	1		T
C13	PT9F	0		C	C13	PT10F	1		C	C13	PT15D	1		C
B13	PT9E	0		T	B13	PT10E	1		T	B13	PT15C	1		T

LCMX02280 Logic Signal Connections: 324 ftBGA (Cont.)

LCMX02280				
Ball Number	Ball Function	Bank	Dual Function	Differential
E13	PT16D	1		C
C15	PT16C	1		T
F13	PT16B	1		C
D14	PT16A	1		T
A18	PT15D	1		C
B17	PT15C	1		T
A16	PT15B	1		C
A17	PT15A	1		T
VCC	VCC	-		
D13	PT14D	1		C
F12	PT14C	1		T
C14	PT14B	1		C
E12	PT14A	1		T
C13	PT13D	1		C
B16	PT13C	1		T
B15	PT13B	1		C
A15	PT13A	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
B14	PT12F	1		C
A14	PT12E	1		T
D12	PT12D	1		C
F11	PT12C	1		T
B13	PT12B	1		C
A13	PT12A	1		T
C12	PT11D	1		C
GND	GND	-		
B12	PT11C	1		T
E11	PT11B	1		C
D11	PT11A	1		T
C11	PT10F	1		C
A12	PT10E	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
F10	PT10D	1		C
D10	PT10C	1		T
B11	PT10B	1	PCLK1_1***	C
A11	PT10A	1		T
E10	PT9D	1		C
C10	PT9C	1		T
D9	PT9B	1	PCLK1_0***	C
E9	PT9A	1		T
B10	PT8F	0		C

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3T100C	1200	1.2V	73	-3	TQFP	100	COM
LCMXO1200E-4T100C	1200	1.2V	73	-4	TQFP	100	COM
LCMXO1200E-5T100C	1200	1.2V	73	-5	TQFP	100	COM
LCMXO1200E-3T144C	1200	1.2V	113	-3	TQFP	144	COM
LCMXO1200E-4T144C	1200	1.2V	113	-4	TQFP	144	COM
LCMXO1200E-5T144C	1200	1.2V	113	-5	TQFP	144	COM
LCMXO1200E-3M132C	1200	1.2V	101	-3	csBGA	132	COM
LCMXO1200E-4M132C	1200	1.2V	101	-4	csBGA	132	COM
LCMXO1200E-5M132C	1200	1.2V	101	-5	csBGA	132	COM
LCMXO1200E-3B256C	1200	1.2V	211	-3	caBGA	256	COM
LCMXO1200E-4B256C	1200	1.2V	211	-4	caBGA	256	COM
LCMXO1200E-5B256C	1200	1.2V	211	-5	caBGA	256	COM
LCMXO1200E-3FT256C	1200	1.2V	211	-3	ftBGA	256	COM
LCMXO1200E-4FT256C	1200	1.2V	211	-4	ftBGA	256	COM
LCMXO1200E-5FT256C	1200	1.2V	211	-5	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3T100C	2280	1.2V	73	-3	TQFP	100	COM
LCMXO2280E-4T100C	2280	1.2V	73	-4	TQFP	100	COM
LCMXO2280E-5T100C	2280	1.2V	73	-5	TQFP	100	COM
LCMXO2280E-3T144C	2280	1.2V	113	-3	TQFP	144	COM
LCMXO2280E-4T144C	2280	1.2V	113	-4	TQFP	144	COM
LCMXO2280E-5T144C	2280	1.2V	113	-5	TQFP	144	COM
LCMXO2280E-3M132C	2280	1.2V	101	-3	csBGA	132	COM
LCMXO2280E-4M132C	2280	1.2V	101	-4	csBGA	132	COM
LCMXO2280E-5M132C	2280	1.2V	101	-5	csBGA	132	COM
LCMXO2280E-3B256C	2280	1.2V	211	-3	caBGA	256	COM
LCMXO2280E-4B256C	2280	1.2V	211	-4	caBGA	256	COM
LCMXO2280E-5B256C	2280	1.2V	211	-5	caBGA	256	COM
LCMXO2280E-3FT256C	2280	1.2V	211	-3	ftBGA	256	COM
LCMXO2280E-4FT256C	2280	1.2V	211	-4	ftBGA	256	COM
LCMXO2280E-5FT256C	2280	1.2V	211	-5	ftBGA	256	COM
LCMXO2280E-3FT324C	2280	1.2V	271	-3	ftBGA	324	COM
LCMXO2280E-4FT324C	2280	1.2V	271	-4	ftBGA	324	COM
LCMXO2280E-5FT324C	2280	1.2V	271	-5	ftBGA	324	COM

Lead-Free Packaging
Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	COM
LCMXO256C-4TN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free TQFP	100	COM
LCMXO256C-5TN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free TQFP	100	COM
LCMXO256C-3MN100C	256	1.8V/2.5V/3.3V	78	-3	Lead-Free csBGA	100	COM
LCMXO256C-4MN100C	256	1.8V/2.5V/3.3V	78	-4	Lead-Free csBGA	100	COM
LCMXO256C-5MN100C	256	1.8V/2.5V/3.3V	78	-5	Lead-Free csBGA	100	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640C-3TN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	COM
LCMXO640C-4TN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free TQFP	100	COM
LCMXO640C-5TN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free TQFP	100	COM
LCMXO640C-3MN100C	640	1.8V/2.5V/3.3V	74	-3	Lead-Free csBGA	100	COM
LCMXO640C-4MN100C	640	1.8V/2.5V/3.3V	74	-4	Lead-Free csBGA	100	COM
LCMXO640C-5MN100C	640	1.8V/2.5V/3.3V	74	-5	Lead-Free csBGA	100	COM
LCMXO640C-3TN144C	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO640C-4TN144C	640	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO640C-5TN144C	640	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO640C-3MN132C	640	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO640C-4MN132C	640	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO640C-5MN132C	640	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO640C-3BN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free caBGA	256	COM
LCMXO640C-4BN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free caBGA	256	COM
LCMXO640C-5BN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free caBGA	256	COM
LCMXO640C-3FTN256C	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640C-4FTN256C	640	1.8V/2.5V/3.3V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640C-5FTN256C	640	1.8V/2.5V/3.3V	159	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-3TN100C	1200	1.8V/2.5V/3.3V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200C-4TN100C	1200	1.8V/2.5V/3.3V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200C-5TN100C	1200	1.8V/2.5V/3.3V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200C-3TN144C	1200	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200C-4TN144C	1200	1.8V/2.5V/3.3V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200C-5TN144C	1200	1.8V/2.5V/3.3V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200C-3MN132C	1200	1.8V/2.5V/3.3V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200C-4MN132C	1200	1.8V/2.5V/3.3V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200C-5MN132C	1200	1.8V/2.5V/3.3V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200C-3BN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200C-4BN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200C-5BN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200C-3FTN256C	1200	1.8V/2.5V/3.3V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200C-4FTN256C	1200	1.8V/2.5V/3.3V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200C-5FTN256C	1200	1.8V/2.5V/3.3V	211	-5	Lead-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256E-3TN100I	256	1.2V	78	-3	Lead-Free TQFP	100	IND
LCMXO256E-4TN100I	256	1.2V	78	-4	Lead-Free TQFP	100	IND
LCMXO256E-3MN100I	256	1.2V	78	-3	Lead-Free csBGA	100	IND
LCMXO256E-4MN100I	256	1.2V	78	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN100I	640	1.2V	74	-3	Lead-Free TQFP	100	IND
LCMXO640E-4TN100I	640	1.2V	74	-4	Lead-Free TQFP	100	IND
LCMXO640E-3MN100I	640	1.2V	74	-3	Lead-Free csBGA	100	IND
LCMXO640E-4MN100I	640	1.2V	74	-4	Lead-Free csBGA	100	IND
LCMXO640E-3TN144I	640	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO640E-4TN144I	640	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO640E-3MN132I	640	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO640E-4MN132I	640	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO640E-3BN256I	640	1.2V	159	-3	Lead-Free caBGA	256	IND
LCMXO640E-4BN256I	640	1.2V	159	-4	Lead-Free caBGA	256	IND
LCMXO640E-3FTN256I	640	1.2V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640E-4FTN256I	640	1.2V	159	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-3TN100I	1200	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200E-4TN100I	1200	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200E-3TN144I	1200	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200E-4TN144I	1200	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200E-3MN132I	1200	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200E-4MN132I	1200	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200E-3BN256I	1200	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200E-4BN256I	1200	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200E-3FTN256I	1200	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200E-4FTN256I	1200	1.2V	211	-4	Lead-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-3TN100I	2280	1.2V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280E-4TN100I	2280	1.2V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280E-3TN144I	2280	1.2V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280E-4TN144I	2280	1.2V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280E-3MN132I	2280	1.2V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280E-4MN132I	2280	1.2V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280E-3BN256I	2280	1.2V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280E-4BN256I	2280	1.2V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280E-3FTN256I	2280	1.2V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280E-4FTN256I	2280	1.2V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280E-3FTN324I	2280	1.2V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280E-4FTN324I	2280	1.2V	271	-4	Lead-Free ftBGA	324	IND

For Further Information

A variety of technical notes for the MachXO family are available on the Lattice web site.

- TN1091, [MachXO sysIO Usage Guide](#)
- TN1089, [MachXO sysCLOCK Design and Usage Guide](#)
- TN1092, [Memory Usage Guide for MachXO Devices](#)
- TN1090, [Power Estimation and Management for MachXO Devices](#)
- TN1086, [MachXO JTAG Programming and Configuration User's Guide](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- TN1097, [MachXO Density Migration](#)
- AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
November 2006	02.3	DC and Switching Characteristics	Corrections to MachXO “C” Sleep Mode Timing table - value for $t_{WSLEEPN}$ (400ns) changed from max. to min. Value for t_{WAWAKE} (100ns) changed from min. to max.
			Added Flash Download Time table.
December 2006	02.4	Architecture	EBR Asynchronous Reset section added.
		Pinout Information	Power Supply and NC table; Pin/Ball orientation footnotes added.
February 2007	02.5	Architecture	Updated EBR Asynchronous Reset section.
August 2007	02.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table.
November 2007	02.7	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
June 2009	02.8	Introduction	Added 0.8-mm 256-pin caBGA package to MachXO Family Selection Guide table.
		Pinout Information	Added Logic Signal Connections table for 0.8-mm 256-pin caBGA package.
		Ordering Information	Updated Part Number Description diagram and Ordering Part Number tables with 0.8-mm 256-pin caBGA package information.
July 2010	02.9	DC and Switching Characteristics	Updated sysCLOCK PLL Timing table.
June 2013	03.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	MachXO1200 and MachXO2280 Hot Socketing Specifications table – Removed footnote 4.
			Added MachXO Programming/Erase Specifications table.