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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128gp706a-e-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section
 2. "CPU" (DS70204) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXGPX06A/X08A/X10A CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The dsPIC33FJXXXGPX06A/X08A/X10A devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33FJXXXGPX06A/X08A/X10A instruction set has two classes of instructions: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the dsPIC33FJXXXGPX06A/X08A/X10A is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1. The programmer's model for the dsPIC33FJXXXGPX06A/ X08A/X10A is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own indepen-

dent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space. The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value, up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

3.3 Special MCU Features

The dsPIC33FJXXXGPX06A/X08A/X10A features a 17-bit by 17-bit, single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed-sign multiplication, it also achieves accurate results for special operations, such as (-1.0) x (-1.0).

The dsPIC33FJXXXGPX06A/X08A/X10A supports 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A 40-bit barrel shifter is used to perform up to a 16-bit, left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

3.6.2.4 Data Space Write Saturation

In addition to adder/subtracter saturation, writes to data space can also be saturated but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These inputs are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly, For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF. For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000. The Most Significant bit of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

3.6.3 BARREL SHIFTER

The barrel shifter is capable of performing up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either of the two DSP accumulators or the X bus (to support multi-bit shifts of register or memory data).

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between bit positions 16 to 31 for right shifts, and between bit positions 0 to 16 for left shifts.

	-0.	LOANZ					100010		100/4/1						-0,			
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2RXF10EID	056A				EID<	15:8>							EID	<7:0>				xxxx
C2RXF11SID	056C				SID<	10:3>					SID<2:0>		—	EXIDE	_	EID<'	17:16>	xxxx
C2RXF11EID	056E				EID<	15:8>							EID	<7:0>				xxxx
C2RXF12SID	0570		SID<10:3>						SID<2:0> — EXIDE — EID<17:16:								xxxx	
C2RXF12EID	0572		EID<15:8>						EID<7:0>								xxxx	
C2RXF13SID	0574				SID<	10:3>				SID<2:0> — EXIDE — EID<'							17:16>	xxxx
C2RXF13EID	0576				EID<	15:8>				EID<7:0>								xxxx
C2RXF14SID	0578				SID<	10:3>					SID<2:0>		_	EXIDE	_	EID<'	17:16>	xxxx
C2RXF14EID	057A	EID<15:8>						EID<7:0>							xxxx			
C2RXF15SID	057C	SID<10:3>						SID<2:0> — EXIDE — EI					EID<	17:16>	xxxx			
C2RXF15EID	057E		EID<15:8>							EID<7:0>							xxxx	

TABLE 4-23: ECAN2 REGISTER MAP WHEN C2CTRL1.WIN = 1 FOR dsPIC33FJXXXGP706A/708A/710A DEVICES ONLY (CONTINUED)

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: PORTG REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	02E4	TRISG15	TRISG14	TRISG13	TRISG12	_	—	TRISG9	TRISG8	TRISG7	TRISG6	_	_	TRISG3	TRISG2	TRISG1	TRISG0	F3CF
PORTG	02E6	RG15	RG14	RG13	RG12	_	_	RG9	RG8	RG7	RG6	_	_	RG3	RG2	RG1	RG0	xxxx
LATG	02E8	LATG15	LATG14	LATG13	LATG12	_	_	LATG9	LATG8	LATG7	LATG6	_	_	LATG3	LATG2	LATG1	LATG0	xxxx
ODCG	06E4	ODCG15	ODCG14	ODCG13	ODCG12	_	_	ODCG9	ODCG8	ODCG7	ODCG6	_	_	ODCG3	ODCG2	ODCG1	ODCG0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-32: SYSTEM CONTROL REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	_	—	—	—	—	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxxx(1)
OSCCON	0742	_	(COSC<2:0	>	_	1	NOSC<2:0	>	CLKLOCK	_	LOCK	_	CF	_	LPOSCEN	OSWEN	₀₃₀₀ (2)
CLKDIV	0744	ROI	I	DOZE<2:0>	>	DOZEN	F	RCDIV<2:0)>	PLLPOS	ST<1:0>	_		F	PLLPRE<4:	:0>		3040
PLLFBD	0746	_	_	_	_	_	—	_					PLLDIV<8:0)>				0030
OSCTUN	0748	_	_	_	_	_	—	_	_	_				TUN	l<5:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register Reset values dependent on type of Reset.

2: OSCCON register Reset values dependent on the FOSC Configuration bits and by type of Reset.

TABLE 4-33: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	_	—	—	_	_	ERASE	—	-		NVMO	P<3:0>		0000(1)
NVMKEY	0766	_	_	_	_	_	—	—	_				NVMKE	Y<7:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-34: PMD REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	—	_	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0772	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	T9MD	T8MD	T7MD	T6MD	_	-		_	_	_	_	_	—	_	I2C2MD	AD2MD	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

-- -

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_		C1IP<2:0>		—		C1RXIP<2:0>	
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		SPI2IP<2:0>				SPI2EIP<2:0>	
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable I	oit	U = Unimple	mented bit, re	ad as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	own
bit 15	Unimpleme	ented: Read as '0)'				
bit 14-12	C1IP<2:0>:	ECAN1 Event In	terrupt Prior	ity bits			
	111 = Interr	rupt is priority 7 (h	nighest priori	ity interrupt)			
	•						
	•						
		rupt is priority 1	ablad				
bit 11		upt source is dis	ableu				
			j ivo Doto Bo	adv Interrupt D	riarity bita		
DIL TU-O	111 = Interr	unt is priority 7 (k	nighest prior	auy interrupt Fi	nonty bits		
	•	upt is priority 7 (i	lightest phon	ity interrupt)			
	•						
	• 001 – Inter	unt is priority 1					
	000 = Inter	rupt source is disa	abled				
bit 7	Unimpleme	ented: Read as '()'				
bit 6-4	SPI2IP<2:0	>: SPI2 Event Int	errupt Priori	ty bits			
	111 = Interr	rupt is priority 7 (ł	nighest prior	ity interrupt)			
	•						
	•						
	001 = Interr	rupt is priority 1					
	000 = Interr	rupt source is disa	abled				
bit 3	Unimpleme	ented: Read as 'o)'				
bit 2-0	SPI2EIP<2:	0>: SPI2 Error In	terrupt Prior	ity bits			
	111 = Interr	rupt is priority 7 (h	nighest prior	ity interrupt)			
	•						
	•						
	001 = Interr	rupt is priority 1					
	000 = Interr	rupt source is disa	abled				

8.0 DIRECT MEMORY ACCESS (DMA)

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 22. "Direct Memory Access (DMA)" (DS70182) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

Direct Memory Access (DMA) is a very efficient mechanism of copying data between peripheral SFRs (e.g., UART Receive register, Input Capture 1 buffer), and buffers or variables stored in RAM, with minimal CPU intervention. The DMA controller can automatically copy entire blocks of data without requiring the user software to read or write the peripheral Special Function Registers (SFRs) every time a peripheral interrupt occurs. The DMA controller uses a dedicated bus for data transfers and therefore, does not steal cycles from the code execution flow of the CPU. To exploit the DMA capability, the corresponding user buffers or variables must be located in DMA RAM.

The dsPIC33FJXXXGPX06A/X08A/X10A peripherals that can utilize DMA are listed in Table 8-1 along with their associated Interrupt Request (IRQ) numbers.

TABLE 8-1: PERIPHERALS WITH DMA SUPPORT

Peripheral	IRQ Number
INT0	0
Input Capture 1	1
Input Capture 2	5
Output Compare 1	2
Output Compare 2	6
Timer2	7
Timer3	8
SPI1	10
SPI2	33
UART1 Reception	11
UART1 Transmission	12
UART2 Reception	30
UART2 Transmission	31
ADC1	13
ADC2	21
DCI	60
ECAN1 Reception	34
ECAN1 Transmission	70
ECAN2 Reception	55
ECAN2 Transmission	71

The DMA controller features eight identical data transfer channels.

Each channel has its own set of control and status registers. Each DMA channel can be configured to copy data either from buffers stored in dual port DMA RAM to peripheral SFRs, or from peripheral SFRs to buffers in DMA RAM.

The DMA controller supports the following features:

- · Word or byte sized data transfers
- Transfers from peripheral to DMA RAM or DMA RAM to peripheral
- Indirect Addressing of DMA RAM locations with or without automatic post-increment
- Peripheral Indirect Addressing In some peripherals, the DMA RAM read/write addresses may be partially derived from the peripheral
- One-Shot Block Transfers Terminating DMA transfer after one block transfer
- Continuous Block Transfers Reloading DMA RAM buffer start address after every block transfer is complete
- Ping-Pong Mode Switching between two DMA RAM start addresses between successive block transfers, thereby filling two buffers alternately
- Automatic or manual initiation of block transfers
- Each channel can select from 20 possible sources of data sources or destinations

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled.

16.3 SPI Control Registers

REGISTER 16-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0			
SPIEN	—	SPISIDL	_	_	—	—	—			
bit 15							bit 8			
U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0			
—	SPIROV	—	—	—	—	SPITBF	SPIRBF			
bit 7							bit 0			
Legend:		C = Clearable	bit							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown			
bit 15	SPIEN: SPIx	SPIEN: SPIx Enable bit								
	1 = Enables module and configures SCKx, SDOx, SDIx and SSx as serial port pins									
L:4 4 4		0 = Disables module								
Dit 14	Unimplemen	ted: Read as 1).).							
DIT 13	SPISIDL: Sto	p in Idle Mode	DIT ration when d	ovice entern Id						
	1 = Discontinue 0 = Continue	module operati	ion in Idle mod	de	lie mode					
bit 12-7	Unimplemen	ted: Read as ')'							
bit 6	SPIROV: Rec	eive Overflow	- Flag bit							
	1 = A new by	te/word is com	pletely receive	ed and discard	led. The user so	oftware has not	read the			
	previous	data in the SPI	xBUF register	r						
	0 = No overfl	ow has occurre	ed							
bit 5-2	Unimplemen	ted: Read as '),							
bit 1	SPITBF: SPI	<pre>< Transmit Buff</pre>	er Full Status	bit						
	1 = Transmit not yet started, SPIxTXB is full									
	Automatically	set in hardwar	e when CPU v	writes SPIxBU	F location. loadi	na SPIxTXB.				
	Automatically	cleared in hard	dware when S	Plx module tra	ansfers data from	n SPIxTXB to S	SPIxSR.			
bit 0	SPIRBF: SPI	x Receive Buffe	er Full Status I	bit						
	1 = Receive c	complete, SPIx	RXB is full							
	0 = Receive is	s not complete,	SPIxRXB is e	empty						
	Automatically	set in hardwar	e when SPIx t	transters data	trom SPIxSR to	SPIXRXB.	'n			
	Automatically	cieareo in naro	aware when co	ore reads SPD	COUL IOCATION, L	eauing SPIXRX	D.			

REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

- **Note 1:** The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).
 - 2: Do not set both Primary and Secondary prescalers to a value of 1:1.
 - **3:** This bit must be cleared when FRMEN = 1.



FIGURE 17-1: I^2C^{TM} BLOCK DIAGRAM (X = 1 OR 2)

REGISTER 19-9: CiCFG1: ECAN[™] BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—	_	_	_	_	_
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW	<1:0>			BRF	P<5:0>		
bit 7							bit 0
							y
Legend:							
R = Readable	bit	W = Writable I	oit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-8	Unimplemen	ted: Read as 'o)'				
bit 7-6	SJW<1:0>: S	ynchronization	Jump Width I	bits			
	11 = Length i	s 4 x Tq					
	10 = Length i	s 3 x Tq					
	01 = Length i	s 2 x Tq					
	00 = Length I	SIXIQ					
bit 5-0	BRP<5:0>: E	Baud Rate Pres	caler bits				
	11 1111 = T	Q = 2 x 64 x 1/F	CAN				
	•						
	•						
	•						
	00 0010 = T	Q = 2 x 3 x 1/Fo	CAN				
	00 0001 = T	q = 2 x 2 x 1/Fo	CAN				
	00 0000 = T	Q = 2 x 1 x 1/Fo	CAN				

REGISTER 19-29: CiTRBnDLC: ECAN™ BUFFER n DATA LENGTH CONTROL (n = 0, 1, ..., 31)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
		EID<	:5:0>			RTR	RB1
bit 15							bit 8
U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_		—	RB0		DLC	C<3:0>	
bit 7				-			bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-10	EID<5:0>: EX	xtended Identifi	er bits				
bit 9	RTR: Remote	e Transmission	Request bit				
	1 = Message 0 = Normal n	will request re nessage	mote transmis	ssion			
bit 8	RB1: Reserv	ed Bit 1					
	11						

	User must set this bit to '0' per CAN protocol.
bit 7-5	Unimplemented: Read as '0'
bit 4	RB0: Reserved Bit 0
	User must set this bit to '0' per CAN protocol.
bit 3-0	DLC<3:0>: Data Length Code bits

REGISTER 19-30: CITRBnDm: ECAN™ BUFFER n DATA FIELD BYTE m

 $(n = 0, 1, ..., 31; m = 0, 1, ..., 7)^{(1)}$

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			TRBnD	m<7:0>			
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRBnDm<7:0>:** Data Field Buffer 'n' Byte 'm' bits

Note 1: The Most Significant Byte contains byte (m + 1) of the buffer.

20.0 DATA CONVERTER INTERFACE (DCI) MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 20. "Data Converter Interface (DCI)" (DS70288) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

20.1 Module Introduction

The dsPIC33FJXXXGPX06A/X08A/X10A Data Converter Interface (DCI) module allows simple interfacing of devices, such as audio coder/decoders (Codecs), ADC and D/A converters. The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I²S) Interface
- · AC-Link Compliant mode

The DCI module provides the following general features:

- · Programmable word size up to 16 bits
- Supports up to 16 time slots, for a maximum frame size of 256 bits
- Data buffering for up to 4 samples without CPU overhead

20.2 Module I/O Pins

There are four I/O pins associated with the module. When enabled, the module controls the data direction of each of the four pins.

20.2.1 CSCK PIN

The CSCK pin provides the serial clock for the DCI module. The CSCK pin may be configured as an input or output using the CSCKD control bit in the DCICON1 SFR. When configured as an output, the serial clock is provided by the dsPIC33FJXXXGPX06A/X08A/X10A. When configured as an input, the serial clock must be provided by an external device.

20.2.2 CSDO PIN

The Serial Data Output (CSDO) pin is configured as an output only pin when the module is enabled. The CSDO pin drives the serial bus whenever data is to be

transmitted. The CSDO pin is tri-stated, or driven to '0', during CSCK periods when data is not transmitted depending on the state of the CSDOM control bit. This allows other devices to place data on the serial bus during transmission periods not used by the DCI module.

20.2.3 CSDI PIN

The Serial Data Input (CSDI) pin is configured as an input only pin when the module is enabled.

20.2.3.1 COFS Pin

The Codec Frame Synchronization (COFS) pin is used to synchronize data transfers that occur on the CSDO and CSDI pins. The COFS pin may be configured as an input or an output. The data direction for the COFS pin is determined by the COFSD control bit in the DCICON1 register.

The DCI module accesses the shadow registers while the CPU is in the process of accessing the memory mapped buffer registers.

20.2.4 BUFFER DATA ALIGNMENT

Data values are always stored left justified in the buffers since most Codec data is represented as a signed 2's complement fractional number. If the received word length is less than 16 bits, the unused Least Significant bits in the Receive Buffer registers are set to '0' by the module. If the transmitted word length is less than 16 bits, the unused LSbs in the Transmit Buffer register are ignored by the module. The word length setup is described in subsequent sections of this document.

20.2.5 TRANSMIT/RECEIVE SHIFT REGISTER

The DCI module has a 16-bit shift register for shifting serial data in and out of the module. Data is shifted in/ out of the shift register, MSb first, since audio PCM data is transmitted in signed 2's complement format.

20.2.6 DCI BUFFER CONTROL

The DCI module contains a buffer control unit for transferring data between the shadow buffer memory and the Serial Shift register. The buffer control unit is a simple 2-bit address counter that points to word locations in the shadow buffer memory. For the receive memory space (high address portion of DCI buffer memory), the address counter is concatenated with a '0' in the MSb location to form a 3-bit address. For the transmit memory space (high portion of DCI buffer memory), the address counter is concatenated with a '1' in the MSb location.

Note: The DCI buffer control unit always accesses the same relative location in the transmit and receive buffers, so only one address counter is provided.

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	11.0		11.0						
	0-0		0-0						
bit 15		DCIGIDE	_	DLOOI	COCKD	COOKL	bit 8		
bit to							Site		
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0		
UNFM	CSDOM	DJST	_	_	_	COFSI	M<1:0>		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	<i>N</i> = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown					
bit 15	DCIEN: DCI N	Module Enable	bit						
	1 = Module is 0 = Module is	disabled							
bit 14	Unimplemen	ted: Read as '	o'						
bit 13	DCISIDL: DC	I Stop in Idle C	ontrol bit						
	1 = Module w	ill halt in CPU I	dle mode						
	0 = Module w	ill continue to c	perate in CP	U Idle mode					
bit 12	Unimplemen	ted: Read as '	כ'						
bit 11	DLOOP: Digit	tal Loopback M	ode Control	bit					
	1 = Digital Lo	opback mode is opback mode is	s enabled. C: s disabled	SDI and CSDO	pins internally o	connected			
bit 10	CSCKD: Sam	ple Clock Dire	ction Control	bit					
	1 = CSCK pin 0 = CSCK pin	n is an input wh n is an output w	en DCI modu hen DCI mod	ule is enabled dule is enabled					
bit 9	CSCKE: Sam	ple Clock Edge	e Control bit						
	1 = Data char 0 = Data char	nges on serial on serial of nges on serial of	clock falling e clock rising e	dge, sampled o dge, sampled o	on serial clock ri n serial clock fa	sing edge Iling edge			
bit 8	COFSD: Fran	ne Synchroniza	ation Direction	n Control bit					
	1 = COFS pin 0 = COFS pin	n is an input wh n is an output w	en DCI modu hen DCI mod	ile is enabled dule is enabled					
bit 7	UNFM: Under	rflow Mode bit							
	1 = Transmit 0 = Transmit '	last value writte '0's on a transn	en to the tran	smit registers o	on a transmit und	derflow			
bit 6	CSDOM: Seri	ial Data Output	Mode bit						
	1 = CSDO pir 0 = CSDO pir	n will be tri-state n drives '0's dui	ed during disa ring disabled	abled transmit f transmit time s	time slots lots				
bit 5	DJST: DCI Da	ata Justification	Control bit						
	1 = Data tran	smission/recep	otion is begur	n during the sar	me serial clock o	cycle as the fra	me		
	0 = Data tran	ismission/recep	otion is begur	n one serial clo	ck cycle after fra	ame synchroniz	ation pulse		
bit 4-2	Unimplemen	ted: Read as '	כ'						
bit 1-0	COFSM<1:0>	- Frame Sync	Mode bits						
	11 = 20-bit A(10 = 16-bit A(C-LINK mode							
	$01 = I^2 S Fran$	ne Sync mode							
	00 = Multi-Ch	annel Frame S	ync mode						

REGISTER 20-1: DCICON1: DCI CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0				
_	—	—	—	BLEN	l<1:0>	_	COFSG3				
bit 15							bit 8				
P/M/-0	P/M/ 0	P/M/0	11-0	P/M-0	P/M/ 0	P/M-0					
17/00-0	COESG<2.0>	10,00-0		10,00-0	WS	<3.0>	10,00-0				
bit 7	0010042.0					10.02	bit C				
Legend:											
R = Readabl	le bit	W = Writable b	pit	U = Unimplen	nented bit, read	d as '0'					
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unk	nown				
bit 15-12	Unimplement	ted: Read as '0)'								
bit 11-10	BLEN<1:0>: E	BLEN<1:0>: Buffer Length Control bits									
	11 = Four data	11 = Four data words will be buffered between interrupts									
	10 = Three da	10 = Three data words will be buffered between interrupts									
	01 = Iwo data	01 = Two data words will be buffered between interrupts									
	00 = One data		uffered betw	een interrupts							
bit 9	Unimplement	ted: Read as 'o)'								
bit 8-5	COFSG<3:0>	COFSG<3:0>: Frame Sync Generator Control bits									
	1111 = Data frame has 16 words										
	•	•									
	•										
	0010 = Data frame has 3 words										
	0001 = Data frame has 2 words										
	0000 = Data f	rame has 1 wo	rd								
bit 4	Unimplement	ted: Read as 'o)'								
bit 3-0	WS<3:0>: DC	WS<3:0>: DCI Data Word Size bits									
	1111 = Data v	1111 = Data word size is 16 bits									
	•										
	•										
	•										
	0100 = Data v	0100 = Data word size is 5 bits									
	0010 = Invali	d Selection D	0011 = Data word size is 4 bits								
	0010 = Invalid Selection. Do not use. Unexpected results may occur										
	0001 = Invali	d Selection. D	o not use. U	nexpected resul	ts may occur						

REGISTER 20-2: DCICON2: DCI CONTROL REGISTER 2

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0			
_	—	—	_		SLOT	<3:0>				
bit 15	•						bit 8			
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0			
—	—	—	—	ROV	RFUL	TUNF	TMPTY			
bit 7							bit 0			
Legend:										
R = Readabl	le bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'				
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown			
bit 15-12	Unimplement	ted: Read as ')'							
bit 11-8	SLOT<3:0>: [SLOT<3:0>: DCI Slot Status bits								
	1111 = Slot #	1111 = Slot #15 is currently active								
	•									
	•	•								
	0010 = Slot #	2 is currently a	ctive							
	0001 = Slot #	1 is currently a	ctive							
	0000 = Slot #	0 is currently a	ctive							
bit 7-4	Unimplement	ted: Read as ')'							
bit 3	ROV: Receive	ROV: Receive Overflow Status bit								
	1 = A receive	1 = A receive overflow has occurred for at least one receive register								
hit 2	0 - A leceive									
DIL Z	1 = New data	KFUL: Receive Buffer Full Status bit								
	1 - 1 The receive registers have old data									
bit 1	TUNF: Transr	TUNF: Transmit Buffer Underflow Status bit								
	1 = A transmit	1 = A transmit underflow has occurred for at least one transmit register								
	0 = A transmit	t underflow has	not occurred		· ·					
bit 0	TMPTY: Trans	smit Buffer Em	pty Status bit							
	1 = The transi 0 = The transi	mit registers ar mit registers ar	e empty e not empty							

REGISTER 20-4: DCISTAT: DCI STATUS REGISTER

21.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/ X08A/X10A family of devices. However, it is not intended to be a comprereference source. То hensive complement the information in this data sheet, refer to Section 16. "Analog-to-Digital Converter (ADC)" (DS70183) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXGPX06A/X08A/X10A devices have up to 32 ADC input channels. These devices also have up to 2 ADC modules (ADCx, where 'x' = 1 or 2), each with its own set of Special Function Registers.

The AD12B bit (ADxCON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4-sample/hold ADC (default configuration) or a 12-bit, 1-sample/hold ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

21.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- Up to 32 analog input pins
- External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan mode
- Selectable conversion trigger source
- Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- · Operation during CPU Sleep and Idle modes

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only 1 sample/hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 32 analog input pins, designated AN0 through AN31. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins. The actual number of analog input pins and external voltage reference input configuration will depend on the specific device.

A block diagram of the ADC is shown in Figure 21-1.

21.2 ADC Initialization

The following configuration steps should be performed.

- 1. Configure the ADC module:
 - a) Select port pins as analog inputs (ADxPCFGH<15:0> or ADxPCFGL<15:0>).
 - b) Select voltage reference source to match expected range on analog inputs (ADxCON2<15:13>).
 - Select the analog conversion clock to match desired data rate with processor clock (ADxCON3<7:0>).
 - d) Determine how many S/H channels will be used (ADxCON2<9:8> and ADxPCFGH<15:0> or ADxPCFGL<15:0>).
 - e) Select the appropriate sample/conversion sequence (ADxCON1<7:5> and ADxCON3<12:8>).
 - f) Select how conversion results are presented in the buffer (ADxCON1<9:8>).
 - g) Turn on ADC module (ADxCON1<15>).
- 2. Configure ADC interrupt (if required):
 - a) Clear the ADxIF bit.
 - b) Select ADC interrupt priority.

21.3 ADC and DMA

If more than one conversion result needs to be buffered before triggering an interrupt, DMA data transfers can be used. Both ADC1 and ADC2 can trigger a DMA data transfer. If ADC1 or ADC2 is selected as the DMA IRQ source, a DMA transfer occurs when the AD1IF or AD2IF bit gets set as a result of an ADC1 or ADC2 sample conversion sequence.

The SMPI<3:0> bits (ADxCON2<5:2>) are used to select how often the DMA RAM buffer pointer is incremented.

The ADDMABM bit (ADxCON1<12>) determines how the conversion results are filled in the DMA RAM buffer area being used for ADC. If this bit is set, DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer. If the ADDMABM bit is cleared, then DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

21.4 ADC Helpful Tips

- 1. The SMPI<3:0> (AD1CON2<5:2>) control bits:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated if enabled.
 - b) When the CSCNA bit (AD1CON2<10>) is set to '1', determines when the ADC analog scan channel list defined in the AD1CSSL/ AD1CSSH registers starts over from the beginning.
 - c) On devices without a DMA peripheral, determines when ADC result buffer pointer to ADC1BUF0-ADC1BUFF, gets reset back to the beginning at ADC1BUF0.
- On devices without a DMA module, the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF regardless of which analog inputs are being used subject to the SMPI<3:0> bits (AD1CON2<5:2>) and the condition described in 1c above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- On devices with a DMA module, the ADC module has only 1 ADC result buffer, (i.e., ADC1BUF0), per ADC peripheral and the ADC conversion result must be read either by the CPU or DMA controller before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in manual sample mode, particularly where the users code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
- 5. On devices with two ADC modules, the ADCxPCFG registers for both ADC modules must be set to a logic '1' to configure a target I/O pin as a digital I/O pin. Failure to do so means that any alternate digital input function will always see only a logic '0' as the digital input buffer is held in Disable mode.

21.5 ADC Resources

Many useful resources related to ADC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en546064

21.5.1 KEY RESOURCES

- Section 16. "Analog-to-Digital Converter (ADC)" (DS70183)
- Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

Note:	For more de	etails on the	instruction set,
	refer to th	e "16-bit N	ICU and DSC
	Programmer	's Refere	nce Manual"
	(DS70157).		

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.W	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x00000x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal ∈ {031}
lit8	8-bit unsigned literal ∈ {0255}
lit10	10-bit unsigned literal ∈ {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {016384}
lit16	16-bit unsigned literal ∈ {065535}
lit23	23-bit unsigned literal ∈ {08388608}; LSb must be '0'
None	Field does not require an entry, may be blank
OA, OB, SA, SB	DSP Status bits: AccA Overflow, AccB Overflow, AccA Saturate, AccB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal ∈ {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)

TABLE 23-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

FIGURE 25-17: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)))ī SCLx IM34 IM31_ IM30 IM33 1 SDAx)) ((Start Stop Condition Condition Note: Refer to Figure 25-1 for load conditions.



FIGURE 25-18: **I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Dimension Limits	MIN	NOM	MAX		
Number of Leads	Ν		64			
Lead Pitch	е		0.50 BSC			
Overall Height	А	1	_	1.20		
Molded Package Thickness	A2	0.95	1.00	1.05		
Standoff	A1	0.05	_	0.15		
Foot Length	L	0.45	0.60	0.75		
Footprint	L1	1.00 REF				
Foot Angle	φ	0°	3.5°	7°		
Overall Width	E	12.00 BSC				
Overall Length	D	12.00 BSC				
Molded Package Width	E1	10.00 BSC				
Molded Package Length	D1	10.00 BSC				
Lead Thickness	С	0.09	-	0.20		
Lead Width	b	0.17	0.22	0.27		
Mold Draft Angle Top	α	11°	12°	13°		
Mold Draft Angle Bottom	β	11°	12°	13°		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B