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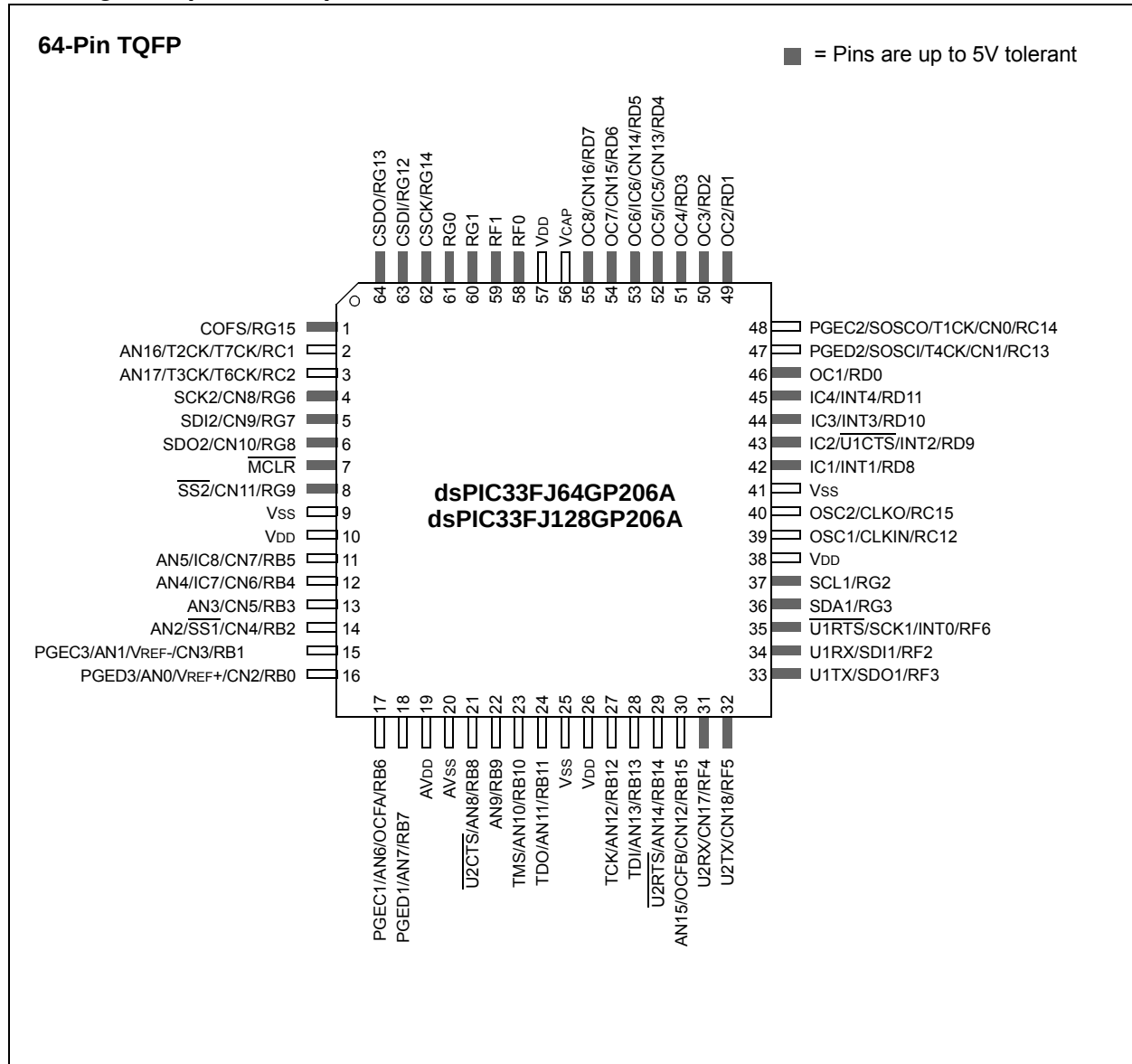
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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128gp706at-i-mr

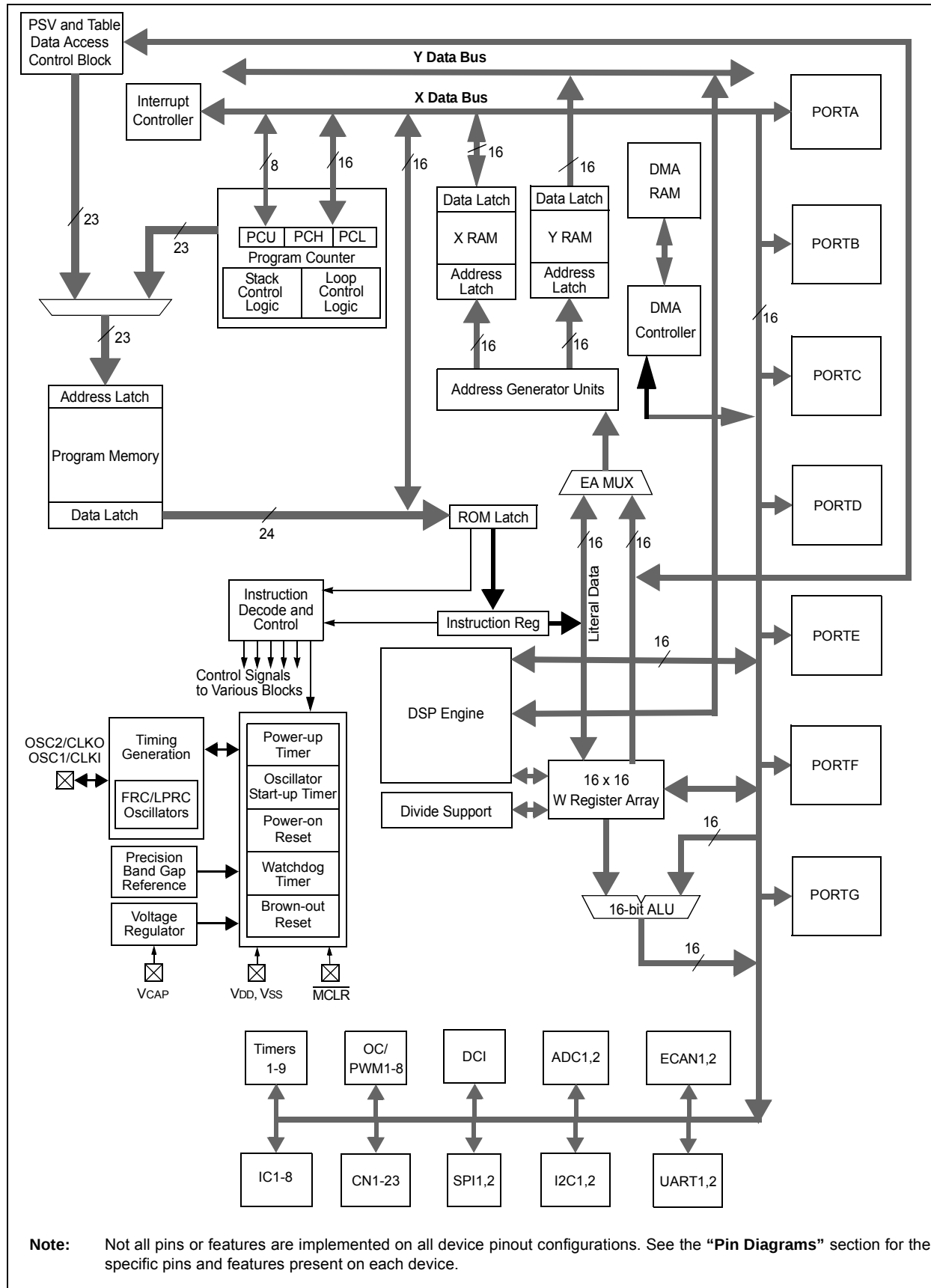
dsPIC33FJXXXGPX06A/X08A/X10A

Pin Diagrams (Continued)



dsPIC33FJXXXGPX06A/X08A/X10A

FIGURE 1-1: dsPIC33FJXXXGPX06A/X08A/X10A GENERAL BLOCK DIAGRAM



dsPIC33FJXXXGPX06A/X08A/X10A

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT ⁽¹⁾	DL<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	PSV	RND	IF
bit 7							bit 0

Legend:	C = Clear only bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x' = Bit is unknown	U = Unimplemented bit, read as '0'	

bit 15-13	Unimplemented: Read as '0'
bit 12	US: DSP Multiply Unsigned/Signed Control bit 1 = DSP engine multiplies are unsigned 0 = DSP engine multiplies are signed
bit 11	EDT: Early D0 Loop Termination Control bit ⁽¹⁾ 1 = Terminate executing D0 loop at end of current loop iteration 0 = No effect
bit 10-8	DL<2:0>: D0 Loop Nesting Level Status bits 111 = 7 D0 loops active : : : 001 = 1 D0 loop active 000 = 0 D0 loops active
bit 7	SATA: AccA Saturation Enable bit 1 = Accumulator A saturation enabled 0 = Accumulator A saturation disabled
bit 6	SATB: AccB Saturation Enable bit 1 = Accumulator B saturation enabled 0 = Accumulator B saturation disabled
bit 5	SATDW: Data Space Write from DSP Engine Saturation Enable bit 1 = Data space write saturation enabled 0 = Data space write saturation disabled
bit 4	ACCSAT: Accumulator Saturation Mode Select bit 1 = 9.31 saturation (super saturation) 0 = 1.31 saturation (normal saturation)
bit 3	IPL3: CPU Interrupt Priority Level Status bit 3 ⁽²⁾ 1 = CPU interrupt priority level is greater than 7 0 = CPU interrupt priority level is 7 or less
bit 2	PSV: Program Space Visibility in Data Space Enable bit 1 = Program space visible in data space 0 = Program space not visible in data space
bit 1	RND: Rounding Mode Select bit 1 = Biased (conventional) rounding enabled 0 = Unbiased (convergent) rounding enabled
bit 0	IF: Integer or Fractional Multiplier Mode Select bit 1 = Integer mode enabled for DSP multiply ops 0 = Fractional mode enabled for DSP multiply ops

Note 1: This bit will always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

dsPIC33FJXXXGPX06A/X08A/X10A

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 3. “Data Memory”** (DS70202) and **Section 4. “Program Memory”** (DS70203) in the “dsPIC33F/PIC24H Family Reference Manual”, which are available from the Microchip web site (www.microchip.com).

The dsPIC33FJXXXGPX06A/X08A/X10A architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33FJXXXGPX06A/X08A/X10A devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.6 “Interfacing Program and Data Memory Spaces”**.

User access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space. Memory usage for the dsPIC33FJXXXGPX06A/X08A/X10A of devices is shown in Figure 4-1.

FIGURE 4-1: PROGRAM MEMORY FOR dsPIC33FJXXXGPX06A/X08A/X10A DEVICES

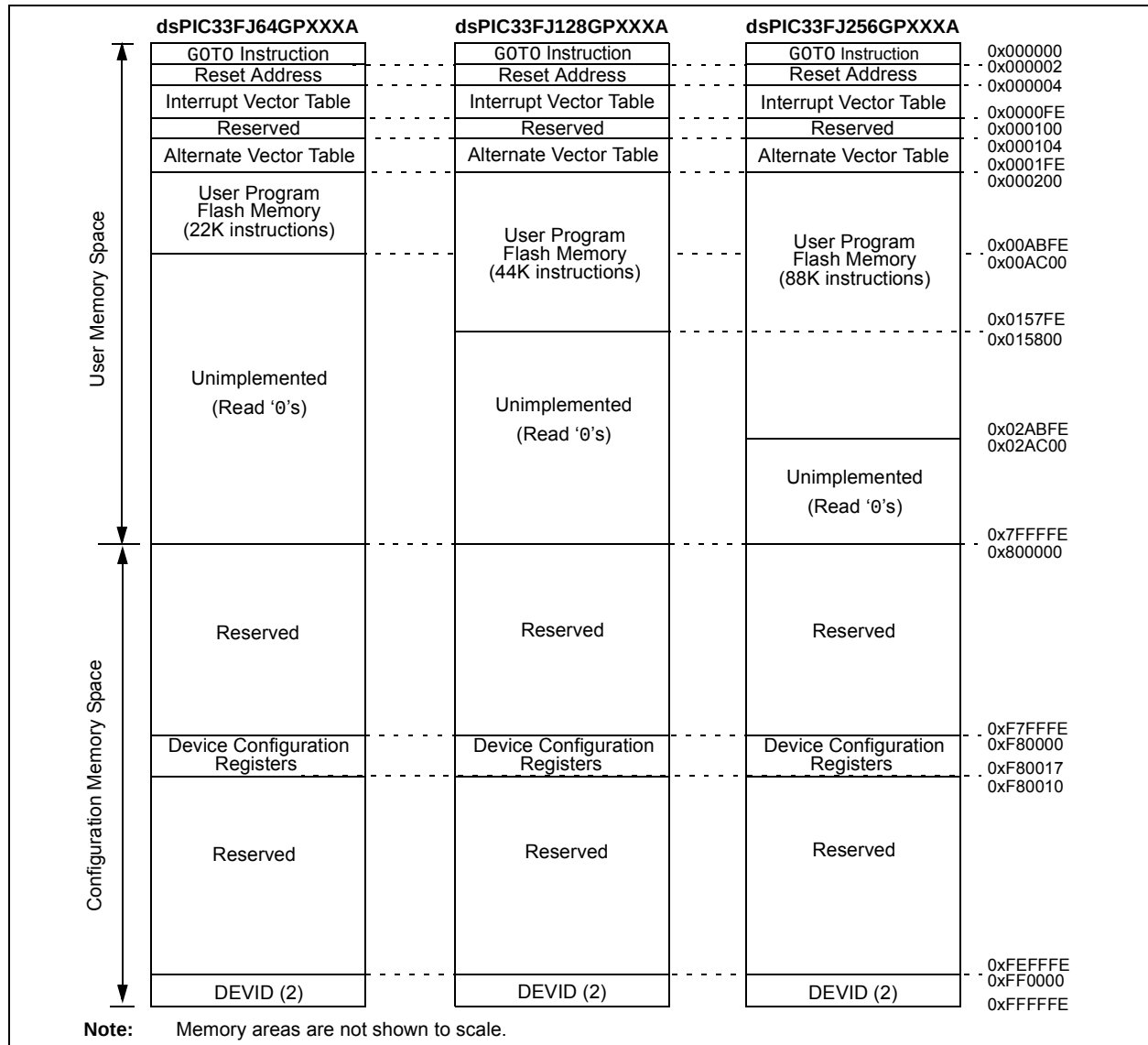


TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS2	0088	T6IF	DMA4IF	—	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	008A	—	—	DMA5IF	DCIIF	DCIEIF	—	—	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	008C	—	—	—	—	—	—	—	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	—	U2EIF	U1EIF	—	0000
IEC0	0094	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC2	0098	T6IE	DMA4IE	—	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	009A	—	—	DMA5IE	DCIIE	DCIEIE	—	—	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	009C	—	—	—	—	—	—	—	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	—	U2EIE	U1EIE	—	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	00AC	—	CNIP<2:0>			—	—	—	—	—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4044
IPC5	00AE	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	00B0	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	00B2	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	00B4	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	00B6	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	00B8	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	00BA	—	T6IP<2:0>			—	DMA4IP<2:0>			—	—	—	—	—	OC8IP<2:0>			4404
IPC12	00BC	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	00BE	—	C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	00C0	—	DCIEIP<2:0>			—	—	—	—	—	—	—	—	—	C2IP<2:0>			4004
IPC15	00C2	—	—	—	—	—	—	—	—	—	DMA5IP<2:0>			—	DCIIP<2:0>			0044
IPC16	00C4	—	—	—	—	—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	0440
IPC17	00C6	—	C2TXIP<2:0>			—	C1TXIP<2:0>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			4444
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJXXXGPX06A/X08A/X10A

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15			bit 8				

U-0	R/W-0 ⁽¹⁾	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
—	ERASE	—	—	NVMOP<3:0> ⁽²⁾			
bit 7				bit 0			

Legend:	SO = Settable only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **WR:** Write Control bit
1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once operation is complete
0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit
1 = Enable Flash program/erase operations
0 = Inhibit Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit
1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
0 = The program or erase operation completed normally
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **ERASE:** Erase/Program Enable bit
1 = Perform the erase operation specified by NVMOP<3:0> on the next WR command
0 = Perform the program operation specified by NVMOP<3:0> on the next WR command
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits⁽²⁾
If ERASE = 1:
1111 = Memory bulk erase operation
1110 = Reserved
1101 = Erase General Segment
1100 = Erase Secure Segment
1011 = Reserved
0011 = No operation
0010 = Memory page erase operation
0001 = No operation
0000 = Erase a single Configuration register byte

If ERASE = 0:
1111 = No operation
1110 = Reserved
1101 = No operation
1100 = No operation
1011 = Reserved
0011 = Memory word program operation
0010 = No operation
0001 = Memory row program operation
0000 = Program a single Configuration register byte

Note 1: These bits can only be reset on POR.

2: All other combinations of NVMOP<3:0> are unimplemented.

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REGISTER 5-2: NVMKEY: NON-VOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:	SO = Settable only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (Write Only) bits

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TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC 1
22	14	0x000030	0x000130	DMA1 – DMA Channel 1
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	ADC2 – ADC 2
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	DMA2 – DMA Channel 2
33	25	0x000046	0x000146	OC3 – Output Compare 3
34	26	0x000048	0x000148	OC4 – Output Compare 4
35	27	0x00004A	0x00014A	T4 – Timer4
36	28	0x00004C	0x00014C	T5 – Timer5
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	U2RX – UART2 Receiver
39	31	0x000052	0x000152	U2TX – UART2 Transmitter
40	32	0x000054	0x000154	SPI2E – SPI2 Error
41	33	0x000056	0x000156	SPI1 – SPI1 Transfer Done
42	34	0x000058	0x000158	C1RX – ECAN1 Receive Data Ready
43	35	0x00005A	0x00015A	C1 – ECAN1 Event
44	36	0x00005C	0x00015C	DMA3 – DMA Channel 3
45	37	0x00005E	0x00015E	IC3 – Input Capture 3
46	38	0x000060	0x000160	IC4 – Input Capture 4
47	39	0x000062	0x000162	IC5 – Input Capture 5
48	40	0x000064	0x000164	IC6 – Input Capture 6
49	41	0x000066	0x000166	OC5 – Output Compare 5
50	42	0x000068	0x000168	OC6 – Output Compare 6
51	43	0x00006A	0x00016A	OC7 – Output Compare 7
52	44	0x00006C	0x00016C	OC8 – Output Compare 8
53	45	0x00006E	0x00016E	Reserved

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REGISTER 7-19: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CNIP<2:0>			—	—	—	—
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP<2:0>			—	SI2C1IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CNIP<2:0>:** Change Notification Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as '0'

bit 6-4 **MI2C1IP<2:0>:** I2C1 Master Events Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SI2C1IP<2:0>:** I2C1 Slave Events Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

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NOTES:

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REGISTER 8-5: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PAD<15:0>**: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-6: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CNT<9:8> ⁽²⁾	
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **CNT<9:0>**: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: Number of DMA transfers = CNT<9:0> + 1.

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REGISTER 19-8: CiEC: ECAN™ TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **TERRCNT<7:0>**: Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>**: Receive Error Count bits

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TABLE 23-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD f	$f = f + \text{WREG}$	1	1	C,DC,N,OV,Z
		ADD f, WREG	$\text{WREG} = f + \text{WREG}$	1	1	C,DC,N,OV,Z
		ADD #lit10, Wn	$\text{Wd} = \text{lit10} + \text{Wd}$	1	1	C,DC,N,OV,Z
		ADD Wb, Ws, Wd	$\text{Wd} = \text{Wb} + \text{Ws}$	1	1	C,DC,N,OV,Z
		ADD Wb, #lit5, Wd	$\text{Wd} = \text{Wb} + \text{lit5}$	1	1	C,DC,N,OV,Z
		ADD Ws0, #Slit4, Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC f	$f = f + \text{WREG} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC f, WREG	$\text{WREG} = f + \text{WREG} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC #lit10, Wn	$\text{Wd} = \text{lit10} + \text{Wd} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC Wb, Ws, Wd	$\text{Wd} = \text{Wb} + \text{Ws} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC Wb, #lit5, Wd	$\text{Wd} = \text{Wb} + \text{lit5} + (\text{C})$	1	1	C,DC,N,OV,Z
3	AND	AND f	$f = f \text{ .AND. } \text{WREG}$	1	1	N,Z
		AND f, WREG	$\text{WREG} = f \text{ .AND. } \text{WREG}$	1	1	N,Z
		AND #lit10, Wn	$\text{Wd} = \text{lit10} \text{ .AND. } \text{Wd}$	1	1	N,Z
		AND Wb, Ws, Wd	$\text{Wd} = \text{Wb} \text{ .AND. } \text{Ws}$	1	1	N,Z
		AND Wb, #lit5, Wd	$\text{Wd} = \text{Wb} \text{ .AND. } \text{lit5}$	1	1	N,Z
4	ASR	ASR f	$f = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR f, WREG	$\text{WREG} = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR Ws, Wd	$\text{Wd} = \text{Arithmetic Right Shift } \text{Ws}$	1	1	C,N,OV,Z
		ASR Wb, Wns, Wnd	$\text{Wnd} = \text{Arithmetic Right Shift } \text{Wb} \text{ by } \text{Wns}$	1	1	N,Z
		ASR Wb, #lit5, Wnd	$\text{Wnd} = \text{Arithmetic Right Shift } \text{Wb} \text{ by } \text{lit5}$	1	1	N,Z
5	BCLR	BCLR f, #bit4	Bit Clear f	1	1	None
		BCLR Ws, #bit4	Bit Clear Ws	1	1	None
6	BRA	BRA C, Expr	Branch if Carry	1	1 (2)	None
		BRA GE, Expr	Branch if greater than or equal	1	1 (2)	None
		BRA GEU, Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA GT, Expr	Branch if greater than	1	1 (2)	None
		BRA GTU, Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA LE, Expr	Branch if less than or equal	1	1 (2)	None
		BRA LEU, Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA LT, Expr	Branch if less than	1	1 (2)	None
		BRA LTU, Expr	Branch if unsigned less than	1	1 (2)	None
		BRA N, Expr	Branch if Negative	1	1 (2)	None
		BRA NC, Expr	Branch if Not Carry	1	1 (2)	None
		BRA NN, Expr	Branch if Not Negative	1	1 (2)	None
		BRA NOV, Expr	Branch if Not Overflow	1	1 (2)	None
		BRA NZ, Expr	Branch if Not Zero	1	1 (2)	None
		BRA OA, Expr	Branch if Accumulator A overflow	1	1 (2)	None
		BRA OB, Expr	Branch if Accumulator B overflow	1	1 (2)	None
		BRA OV, Expr	Branch if Overflow	1	1 (2)	None
		BRA SA, Expr	Branch if Accumulator A saturated	1	1 (2)	None
		BRA SB, Expr	Branch if Accumulator B saturated	1	1 (2)	None
		BRA Expr	Branch Unconditionally	1	2	None
		BRA Z, Expr	Branch if Zero	1	1 (2)	None
		BRA Wn	Computed Branch	1	2	None
7	BSET	BSET f, #bit4	Bit Set f	1	1	None
		BSET Ws, #bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C Ws, Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z Ws, Wb	Write Z bit to Ws<Wb>	1	1	None
9	BTG	BTG f, #bit4	Bit Toggle f	1	1	None
		BTG Ws, #bit4	Bit Toggle Ws	1	1	None

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25.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33FJXXXGPX06A/X08A/X10A AC characteristics and timing parameters.

TABLE 25-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
	Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial
	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended
Operating voltage V_{DD} range as described in Table 25-1.	

FIGURE 25-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

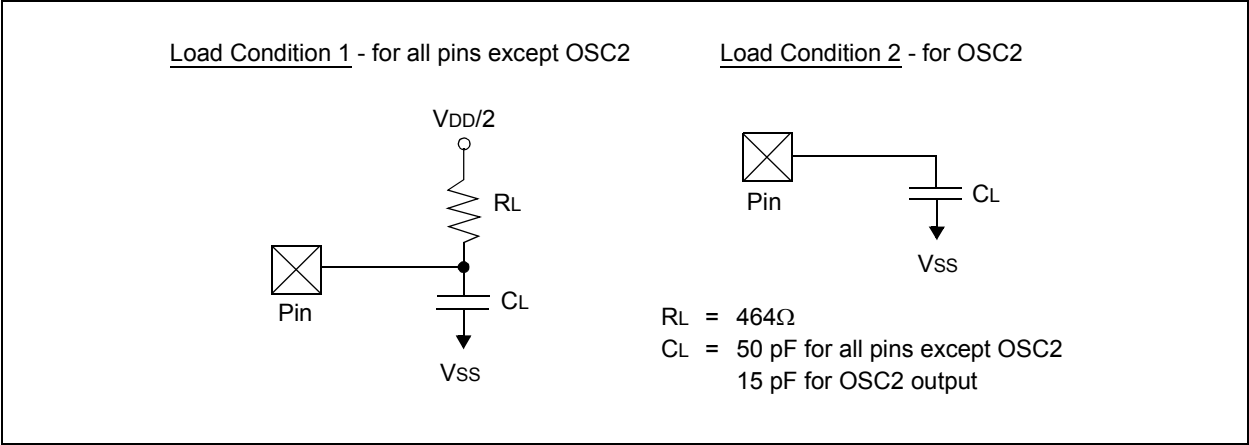


TABLE 25-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO50	Cosc2	OSC2/SOSC2 pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Cio	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	Cb	SCLx, SDAx	—	—	400	pF	In I ² C™ mode

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FIGURE 25-6: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS

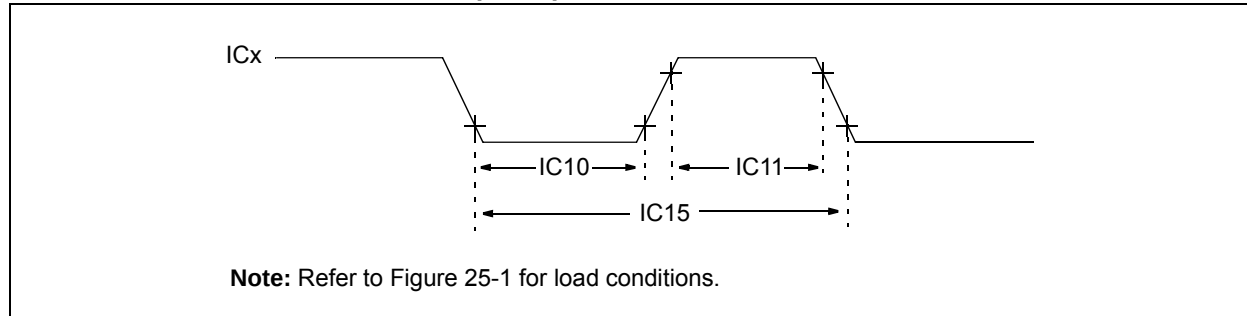


TABLE 25-25: INPUT CAPTURE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time	No Prescaler	$0.5 T_{CY} + 20$	—	ns	—
			With Prescaler	10	—	ns	
IC11	TccH	ICx Input High Time	No Prescaler	$0.5 T_{CY} + 20$	—	ns	—
			With Prescaler	10	—	ns	
IC15	TccP	ICx Input Period		$(T_{CY} + 40)/N$	—	ns	N = prescale value (1, 4, 16)

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 25-7: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS

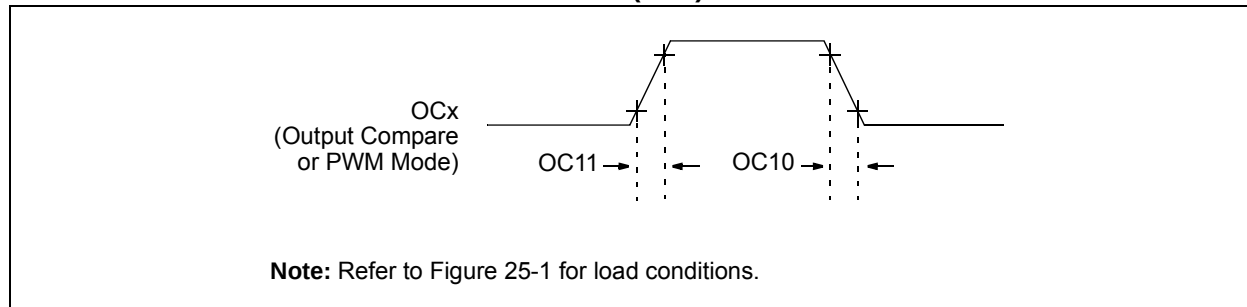


TABLE 25-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter D032
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter D031

Note 1: These parameters are characterized but not tested in manufacturing.

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TABLE 25-45: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50b	TAD	ADC Clock Period	76	—	—	ns	—
AD51b	TRC	ADC Internal RC Oscillator Period	—	250	—	ns	—
Conversion Rate							
AD55b	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56b	FCNV	Throughput Rate	—	—	1.1	Msp/s	—
AD57b	TSAMP	Sample Time	2 TAD	—	—	—	—
Timing Parameters							
AD60b	TPCS	Conversion Start from Sample Trigger ⁽²⁾	2.0 TAD	—	3.0 TAD	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61b	TPSS	Sample Start from Setting Sample (SAMP) bit ⁽²⁾	2.0 TAD	—	3.0 TAD	—	—
AD62b	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽²⁾	—	0.5 TAD	—	—	—
AD63b	TDPV	Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3)	—	—	20	μs	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: TDPV is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.

TABLE 25-46: DMA READ/WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min.	Typ	Max.	Units	Conditions	
DM1a	DMA Read/Write Cycle Time	—	—	2 TCY	ns	This characteristic applies to dsPIC33FJ256GPX06A/X08A/X10A devices only.	
DM1b	DMA Read/Write Cycle Time	—	—	1 TCY	ns	This characteristic applies to all devices with the exception of the dsPIC33FJ256GPX06A/X08A/X10A.	

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26.0 HIGH TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJXXXGPX06A/X08A/X10A electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 25.0 “Electrical Characteristics”** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter DC10 in **Section 25.0 “Electrical Characteristics”** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33FJXXXGPX06A/X08A/X10A high temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ⁽⁴⁾	-40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS ⁽⁵⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽⁵⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽⁵⁾	-0.3V to 5.6V
Voltage on VCAP with respect to VSS	2.25V to 2.75V
Maximum current out of VSS pin	60 mA
Maximum current into VDD pin ⁽²⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 2x I/O pin ⁽³⁾	2 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽³⁾	4 mA
Maximum current sourced/sunk by any 8x I/O pin ⁽³⁾	8 mA
Maximum current sunk by all ports combined	10 mA
Maximum current sourced by all ports combined ⁽²⁾	10 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 26-2).

3: Unlike devices at 125°C and below, the specifications in this section also apply to the CLKOUT, VREF+, VREF-, SCLx, SDAx, PGECx, and PGEDx pins.

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

5: Refer to the “Pin Diagrams” section for 5V tolerant pins.

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TABLE 26-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for High Temperature				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
HDO10	VOL	Output Low Voltage I/O Pins: 2x Sink Driver Pins - All pins not defined by 4x or 8x driver pins	—	—	0.4	V	$I_{OL} \leq 1.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output Low Voltage I/O Pins: 4x Sink Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	—	—	0.4	V	$I_{OL} \leq 3.6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - OSC2, CLKO, RC15	—	—	0.4	V	$I_{OL} \leq 6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
HDO20	VOH	Output High Voltage I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	2.4	—	—	V	$I_{OH} \geq -1.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage I/O Pins: 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	2.4	—	—	V	$I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage I/O Pins: 8x Source Driver Pins - OSC2, CLKO, RC15	2.4	—	—	V	$I_{OH} \geq -6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
HDO20A	VOH1	Output High Voltage I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	1.5	—	—	V	$I_{OH} \geq -1.9 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			2.0	—	—		$I_{OH} \geq -1.85 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			3.0	—	—		$I_{OH} \geq -1.4 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	1.5	—	—	V	$I_{OH} \geq -3.9 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			2.0	—	—		$I_{OH} \geq -3.7 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			3.0	—	—		$I_{OH} \geq -2 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage 8x Source Driver Pins - OSC2, CLKO, RC15	1.5	—	—	V	$I_{OH} \geq -7.5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			2.0	—	—		$I_{OH} \geq -6.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			3.0	—	—		$I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1

Note 1: Parameters are characterized, but not tested.

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TABLE 26-17: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Clock Parameters							
HAD50	TAD	ADC Clock Period ⁽¹⁾	147	—	—	ns	—
Conversion Rate							
HAD56	FCNV	Throughput Rate ⁽¹⁾	—	—	400	Ksps	—

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-18: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Clock Parameters							
HAD50	TAD	ADC Clock Period ⁽¹⁾	104	—	—	ns	—
Conversion Rate							
HAD56	FCNV	Throughput Rate ⁽¹⁾	—	—	800	Ksps	—

Note 1: These parameters are characterized but not tested in manufacturing.

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