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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128gp708a-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128gp708a-i-pt</a>

## Referenced Sources

This device data sheet is based on the following individual chapters of the “dsPIC33F/PIC24H Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the documents listed below, browse to the documentation section of the dsPIC33FJ256GP710A product page on the Microchip web site ([www.microchip.com](http://www.microchip.com)) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. “Introduction”** (DS70197)
- **Section 2. “CPU”** (DS70204)
- **Section 3. “Data Memory”** (DS70202)
- **Section 4. “Program Memory”** (DS70203)
- **Section 5. “Flash Programming”** (DS70191)
- **Section 6. “Interrupts”** (DS70184)
- **Section 7. “Oscillator”** (DS70186)
- **Section 8. “Reset”** (DS70192)
- **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS70196)
- **Section 10. “I/O Ports”** (DS70193)
- **Section 11. “Timers”** (DS70205)
- **Section 12. “Input Capture”** (DS70198)
- **Section 13. “Output Compare”** (DS70209)
- **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70183)
- **Section 17. “UART”** (DS70188)
- **Section 18. “Serial Peripheral Interface (SPI)”** (DS70206)
- **Section 19. “Inter-Integrated Circuit™ (I2C™)”** (DS70195)
- **Section 20. “Data Converter Interface (DCI)”** (DS70288)
- **Section 21. “Enhanced Controller Area Network (ECAN™)”** (DS70185)
- **Section 22. “Direct Memory Access (DMA)”** (DS70182)
- **Section 23. “CodeGuard™ Security”** (DS70199)
- **Section 24. “Programming and Diagnostics”** (DS70207)
- **Section 25. “Device Configuration”** (DS70194)

# dsPIC33FJXXXGPX06A/X08A/X10A

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NOTES:

**TABLE 4-7: INPUT CAPTURE REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140	Input 1 Capture Register																xxxx
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC2BUF	0144	Input 2 Capture Register																xxxx
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC3BUF	0148	Input 3 Capture Register																xxxx
IC3CON	014A	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC4BUF	014C	Input 4 Capture Register																xxxx
IC4CON	014E	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC5BUF	0150	Input 5 Capture Register																xxxx
IC5CON	0152	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC6BUF	0154	Input 6 Capture Register																xxxx
IC6CON	0156	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC7BUF	0158	Input 7 Capture Register																xxxx
IC7CON	015A	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC8BUF	015C	Input 8 Capture Register																xxxx
IC8CON	015E	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-31: PORTG REGISTER MAP<sup>(1)</sup>**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	02E4	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	TRISG1	TRISG0	F3CF
PORTG	02E6	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	RG1	RG0	xxxx
LATG	02E8	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	LATG1	LATG0	xxxx
ODCG	06E4	ODCG15	ODCG14	ODCG13	ODCG12	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	ODCG1	ODCG0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

**Note 1:** The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

**TABLE 4-32: SYSTEM CONTROL REGISTER MAP**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	—	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx <sup>(1)</sup>
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	LOCK	—	CF	—	LPOSCEN	OSWEN	0300 <sup>(2)</sup>
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** RCON register Reset values dependent on type of Reset.

**Note 2:** OSCCON register Reset values dependent on the FOSC Configuration bits and by type of Reset.

**TABLE 4-33: NVM REGISTER MAP**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP<3:0>				0000 <sup>(1)</sup>
NVMKEY	0766	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

**TABLE 4-34: PMD REGISTER MAP**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0772	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	T9MD	T8MD	T7MD	T6MD	—	—	—	—	—	—	—	—	—	—	I2C2MD	AD2MD	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# dsPIC33FJXXXGPX06A/X08A/X10A

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## REGISTER 6-1: RCON: RESET CONTROL REGISTER<sup>(1)</sup> (CONTINUED)

bit 0      **POR:** Power-on Reset Flag bit  
            1 = A Power-on Reset has occurred  
            0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.
- 3:** For dsPIC33FJ256GPX06A/X08A/X10A devices, this bit is unimplemented and reads back programmed value.

## REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2 (CONTINUED)

- bit 2      **C1RXIF:** ECAN1 Receive Data Ready Interrupt Flag Status bit  
            1 = Interrupt request has occurred  
            0 = Interrupt request has not occurred
- bit 1      **SPI2IF:** SPI2 Event Interrupt Flag Status bit  
            1 = Interrupt request has occurred  
            0 = Interrupt request has not occurred
- bit 0      **SPI2EIF:** SPI2 Error Interrupt Flag Status bit  
            1 = Interrupt request has occurred  
            0 = Interrupt request has not occurred

# dsPIC33FJXXXGPX06A/X08A/X10A

## REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	—	DMA5IF	DCIIF	DCIEIF	—	—	C2IF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **DMA5IF:** DMA Channel 5 Data Transfer Complete Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 12 **DCIIF:** DCI Event Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 11 **DCIEIF:** DCI Error Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 10-9 **Unimplemented:** Read as '0'
- bit 8 **C2IF:** ECAN2 Event Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 7 **C2RXIF:** ECAN2 Receive Data Ready Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 6 **INT4IF:** External Interrupt 4 Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 5 **INT3IF:** External Interrupt 3 Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 4 **T9IF:** Timer9 Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 3 **T8IF:** Timer8 Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 2 **MI2C2IF:** I2C2 Master Events Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 1 **SI2C2IF:** I2C2 Slave Events Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred
- bit 0 **T7IF:** Timer7 Interrupt Flag Status bit  
1 = Interrupt request has occurred  
0 = Interrupt request has not occurred



# dsPIC33FJXXXGPX06A/X08A/X10A

## REGISTER 7-15: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP<2:0>			—	OC1IP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC1IP<2:0>			—	INT0IP<2:0>		
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T1IP<2:0>:** Timer1 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **INT0IP<2:0>:** External Interrupt 0 Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

# dsPIC33FJXXGPX06A/X08A/X10A

## REGISTER 7-20: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC8IP<2:0>			—	IC7IP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD2IP<2:0>			—	INT1IP<2:0>		
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **IC8IP<2:0>:** Input Capture Channel 8 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **IC7IP<2:0>:** Input Capture Channel 7 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **AD2IP<2:0>:** ADC2 Conversion Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

# dsPIC33FJXXXGPX06A/X08A/X10A

**REGISTER 8-5: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **PAD<15:0>**: Peripheral Address Register bits

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**REGISTER 8-6: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER<sup>(1)</sup>**

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CNT<9:8> <sup>(2)</sup>	
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0> <sup>(2)</sup>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10      **Unimplemented:** Read as '0'

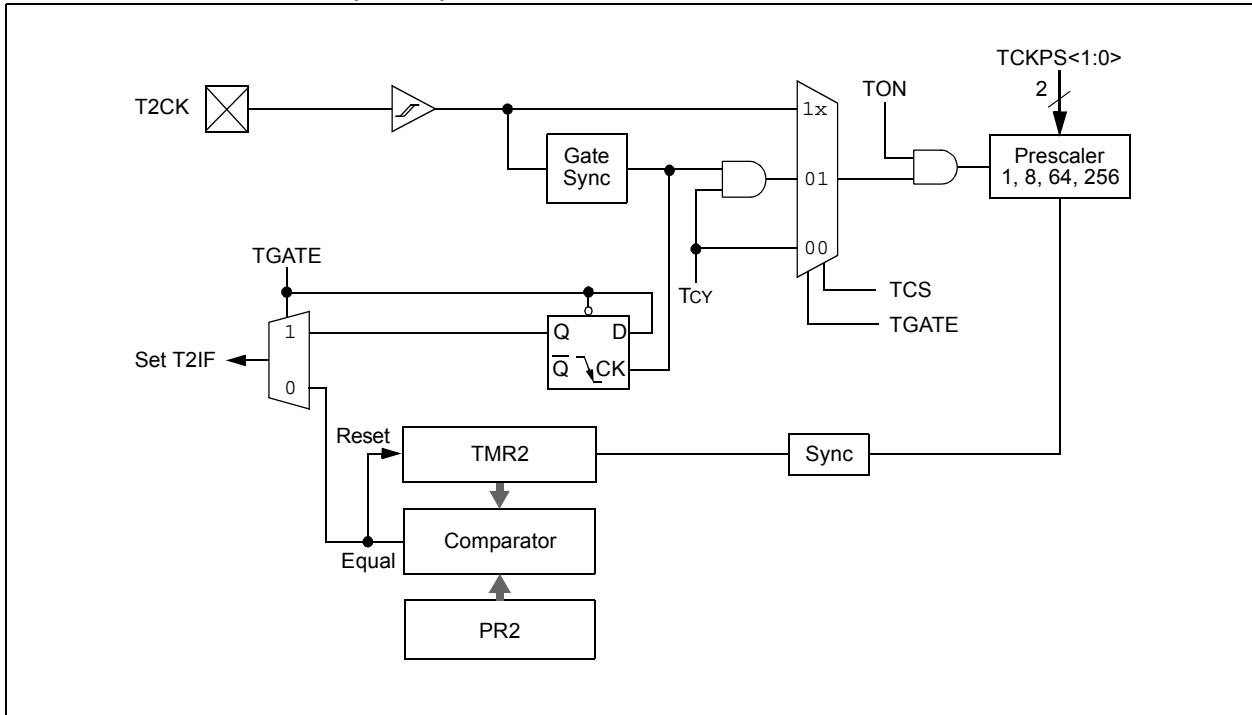
bit 9-0      **CNT<9:0>**: DMA Transfer Count Register bits<sup>(2)</sup>

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**2:** Number of DMA transfers = CNT<9:0> + 1.

# dsPIC33FJXXGPX06A/X08A/X10A

FIGURE 13-2: TIMER2 (16-BIT) BLOCK DIAGRAM



# dsPIC33FJXXXGPX06A/X08A/X10A

**REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN <sup>(3)</sup>	CKP	MSTEN	SPRE<2:0> <sup>(2)</sup>			PPRE<1:0> <sup>(2)</sup>	
bit 7							bit 0

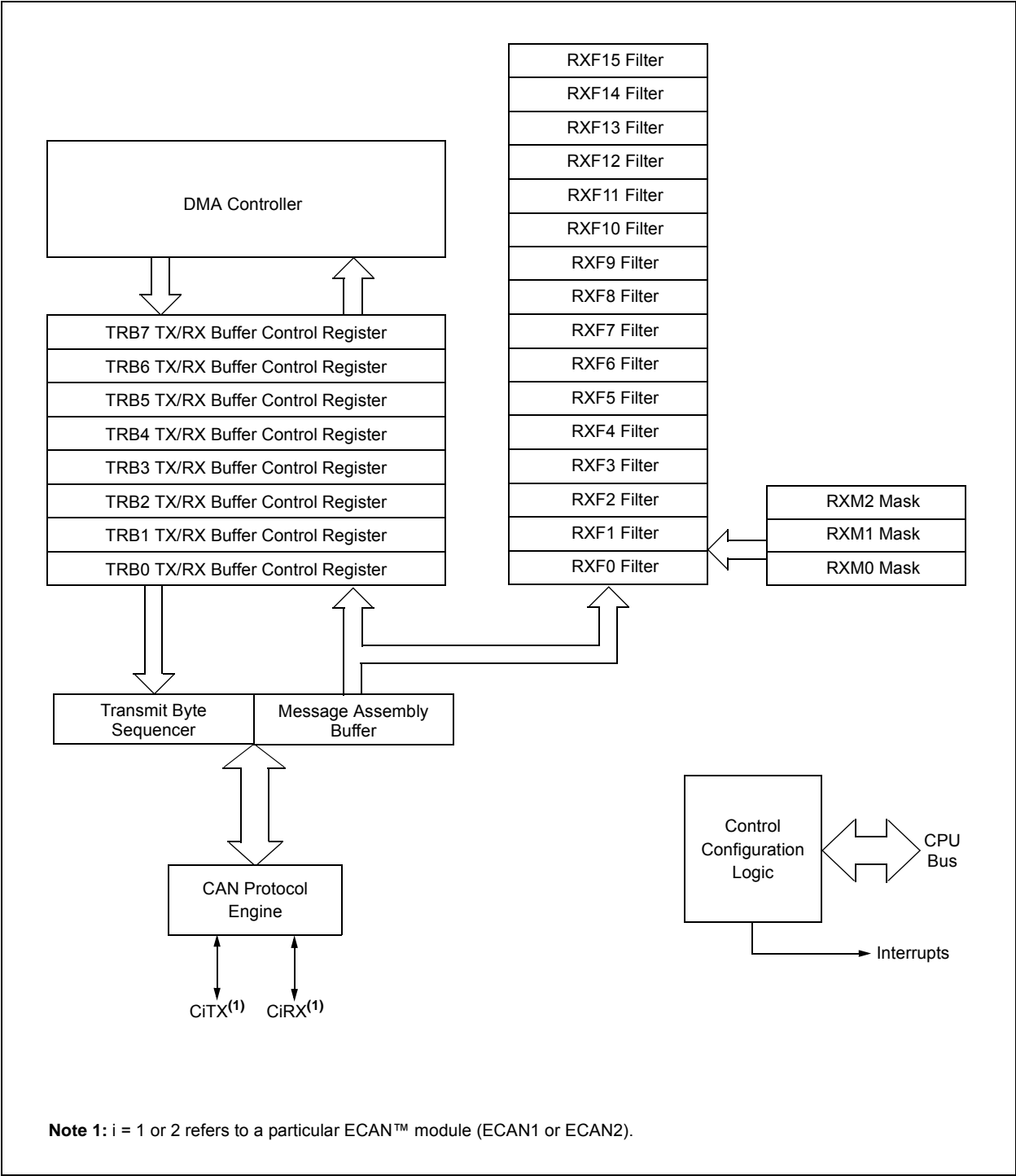
**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-13      **Unimplemented:** Read as '0'
- bit 12      **DISSCK:** Disable SCKx pin bit (SPI Master modes only)  
               1 = Internal SPI clock is disabled, pin functions as I/O  
               0 = Internal SPI clock is enabled
- bit 11      **DISSDO:** Disable SDOx pin bit  
               1 = SDOx pin is not used by module; pin functions as I/O  
               0 = SDOx pin is controlled by the module
- bit 10      **MODE16:** Word/Byte Communication Select bit  
               1 = Communication is word-wide (16 bits)  
               0 = Communication is byte-wide (8 bits)
- bit 9      **SMP:** SPIx Data Input Sample Phase bit  
               Master mode:  
               1 = Input data sampled at end of data output time  
               0 = Input data sampled at middle of data output time  
               Slave mode:  
               SMP must be cleared when SPIx is used in Slave mode.
- bit 8      **CKE:** SPIx Clock Edge Select bit<sup>(1)</sup>  
               1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)  
               0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)
- bit 7      **SSEN:** Slave Select Enable bit (Slave mode)<sup>(3)</sup>  
               1 =  $\overline{SSx}$  pin used for Slave mode  
               0 =  $\overline{SSx}$  pin not used by module. Pin controlled by port function
- bit 6      **CKP:** Clock Polarity Select bit  
               1 = Idle state for clock is a high level; active state is a low level  
               0 = Idle state for clock is a low level; active state is a high level
- bit 5      **MSTEN:** Master Mode Enable bit  
               1 = Master mode  
               0 = Slave mode

- Note 1:** The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).
- 2:** Do not set both Primary and Secondary prescalers to a value of 1:1.
- 3:** This bit must be cleared when FRMEN = 1.

FIGURE 19-1: ECAN™ MODULE BLOCK DIAGRAM



# dsPIC33FJXXGPX06A/X08A/X10A

**REGISTER 19-6: CiINTF: ECAN™ INTERRUPT FLAG REGISTER**

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							
							bit 8

R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							
							bit 0

<b>Legend:</b>	C = Clear only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-14	<b>Unimplemented:</b> Read as '0'
bit 13	<b>TXBO:</b> Transmitter in Error State Bus Off bit 1 = Transmitter is in Bus Off state 0 = Transmitter is not in Bus Off state
bit 12	<b>TXBP:</b> Transmitter in Error State Bus Passive bit 1 = Transmitter is in Bus Passive state 0 = Transmitter is not in Bus Passive state
bit 11	<b>RXBP:</b> Receiver in Error State Bus Passive bit 1 = Receiver is in Bus Passive state 0 = Receiver is not in Bus Passive state
bit 10	<b>TXWAR:</b> Transmitter in Error State Warning bit 1 = Transmitter is in Error Warning state 0 = Transmitter is not in Error Warning state
bit 9	<b>RXWAR:</b> Receiver in Error State Warning bit 1 = Receiver is in Error Warning state 0 = Receiver is not in Error Warning state
bit 8	<b>EWARN:</b> Transmitter or Receiver in Error State Warning bit 1 = Transmitter or receiver is in Error Warning state 0 = Transmitter or receiver is not in Error Warning state
bit 7	<b>IVRIF:</b> Invalid Message Received Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 6	<b>WAKIF:</b> Bus Wake-up Activity Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 5	<b>ERRIF:</b> Error Interrupt Flag bit (multiple sources in CiINTF<13:8> register) 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 4	<b>Unimplemented:</b> Read as '0'
bit 3	<b>FIFOIF:</b> FIFO Almost Full Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	<b>RBOVIF:</b> RX Buffer Overflow Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 1	<b>RBIF:</b> RX Buffer Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 0	<b>TBIF:</b> TX Buffer Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

# dsPIC33FJXXXGPX06A/X08A/X10A

## REGISTER 19-8: CIEC: ECAN™ TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8      **TERRCNT<7:0>**: Transmit Error Count bits

bit 7-0      **RERRCNT<7:0>**: Receive Error Count bits



# dsPIC33FJXXXGPX06A/X08A/X10A

## 21.4 ADC Helpful Tips

1. The SMPI<3:0> (AD1CON2<5:2>) control bits:
  - a) Determine when the ADC interrupt flag is set and an interrupt is generated if enabled.
  - b) When the CSCNA bit (AD1CON2<10>) is set to '1', determines when the ADC analog scan channel list defined in the AD1CSSL/AD1CSSH registers starts over from the beginning.
  - c) On devices without a DMA peripheral, determines when ADC result buffer pointer to ADC1BUF0-ADC1BUFF, gets reset back to the beginning at ADC1BUF0.
2. On devices without a DMA module, the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF regardless of which analog inputs are being used subject to the SMPI<3:0> bits (AD1CON2<5:2>) and the condition described in 1c above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. On devices with a DMA module, the ADC module has only 1 ADC result buffer, (i.e., ADC1BUF0), per ADC peripheral and the ADC conversion result must be read either by the CPU or DMA controller before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in manual sample mode, particularly where the users code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
5. On devices with two ADC modules, the ADCxPCFG registers for both ADC modules must be set to a logic '1' to configure a target I/O pin as a digital I/O pin. Failure to do so means that any alternate digital input function will always see only a logic '0' as the digital input buffer is held in Disable mode.

## 21.5 ADC Resources

Many useful resources related to ADC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<b>Note:</b>	In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en546064">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en546064</a>
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### 21.5.1 KEY RESOURCES

- **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70183)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

# dsPIC33FJXXXGPX06A/X08A/X10A

## REGISTER 21-5: ADxCHS123: ADCx INPUT CHANNEL 1, 2, 3 SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NB<1:0>		CH123SB
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NA<1:0>		CH123SA
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **CH123NB<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample B bits

**When AD12B = 1, CHxNB is: U-0, Unimplemented, Read as '0'**

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11

10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

0x = CH1, CH2, CH3 negative input is VREF-

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample B bit

**When AD12B = 1, CHxSB is: U-0, Unimplemented, Read as '0'**

1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5

0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

bit 7-3 **Unimplemented:** Read as '0'

bit 2-1 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample A bits

**When AD12B = 1, CHxNA is: U-0, Unimplemented, Read as '0'**

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11

10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

0x = CH1, CH2, CH3 negative input is VREF-

bit 0 **CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample A bit

**When AD12B = 1, CHxSA is: U-0, Unimplemented, Read as '0'**

1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5

0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

# dsPIC33FJXXXGPX06A/X08A/X10A

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## 24.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 24.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

## 24.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 24.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 24.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

# dsPIC33FJXXXGPX06A/X08A/X10A

**TABLE 25-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Parameter No. <sup>(3)</sup>	Typical <sup>(2)</sup>	Max	Units	Conditions		
Operating Current (IDD) <sup>(1)</sup>						
DC20d	27	30	mA	-40°C	3.3V	10 MIPS
DC20a	27	30	mA	+25°C		
DC20b	27	30	mA	+85°C		
DC20c	27	35	mA	+125°C		
DC21d	36	40	mA	-40°C	3.3V	16 MIPS
DC21a	37	40	mA	+25°C		
DC21b	38	45	mA	+85°C		
DC21c	39	45	mA	+125°C		
DC22d	43	50	mA	-40°C	3.3V	20 MIPS
DC22a	46	50	mA	+25°C		
DC22b	46	55	mA	+85°C		
DC22c	47	55	mA	+125°C		
DC23d	65	70	mA	-40°C	3.3V	30 MIPS
DC23a	65	70	mA	+25°C		
DC23b	65	70	mA	+85°C		
DC23c	65	70	mA	+125°C		
DC24d	84	90	mA	-40°C	3.3V	40 MIPS
DC24a	84	90	mA	+25°C		
DC24b	84	90	mA	+85°C		
DC24c	84	90	mA	+125°C		

**Note 1:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLK0 is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to VSS
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing `while(1)` statement
- JTAG is disabled

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** These parameters are characterized but not tested in manufacturing.

# dsPIC33FJXXXGPX06A/X08A/X10A

**TABLE 26-9: INTERNAL LPRC ACCURACY**

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature						
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	LPRC @ 32.768 kHz <sup>(1)</sup>						
HF21	LPRC	-70 <sup>(2)</sup>	—	+70 <sup>(2)</sup>	%	$-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$	

**Note 1:** Change of LPRC frequency as VDD changes.

**2:** Characterized but not tested.

**TABLE 26-10: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	—	—	ns	—
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	—	—	ns	—

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 26-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns	—
HSP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	35	—	—	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	—	—	ns	—
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	—	—	ns	—

**Note 1:** These parameters are characterized but not tested in manufacturing.