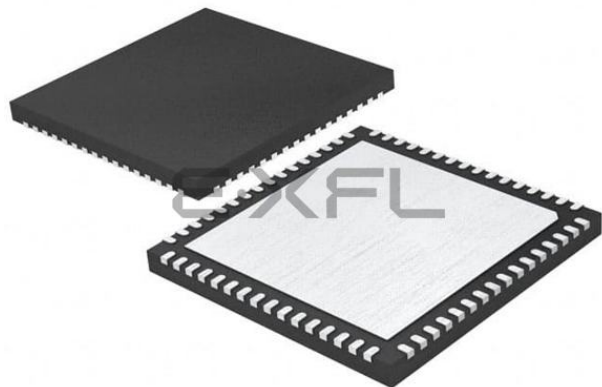




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Details

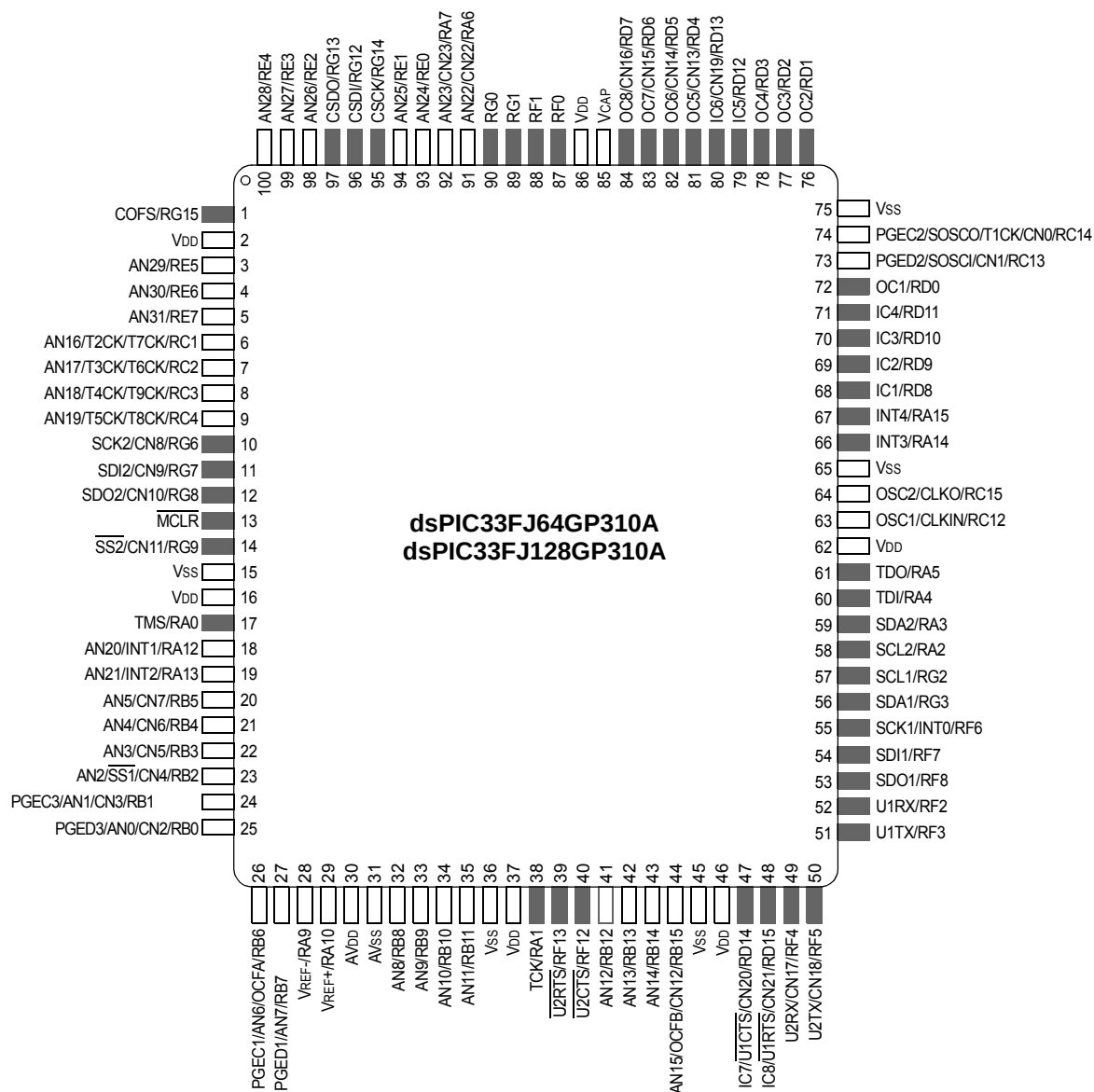
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj256gp506a-i-mr

dsPIC33FJXXXGPX06A/X08A/X10A

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant



dsPIC33FJXXXGPX06A/X08A/X10A

3.5 Arithmetic Logic Unit (ALU)

The dsPIC33FJXXXGPX06A/X08A/X10A ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the “16-bit MCU and DSC Programmer's Reference Manual” (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJXXXGPX06A/X08A/X10A CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

3.5.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.5.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.6 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtractor (with two target accumulators, round and saturation logic).

The dsPIC33FJXXXGPX06A/X08A/X10A is a single-cycle, instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources may be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine also has the capability to perform inherent accumulator-to-accumulator operations which require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has various options selected through various bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed or unsigned DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for AccA (SATA)
- Automatic saturation on/off for AccB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

Table 3-1 provides a summary of DSP instructions. A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	$A = 0$	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \cdot y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \cdot y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \cdot y$	No
MSC	$A = A - x \cdot y$	Yes

TABLE 4-9: I2C1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	—	Baud Rate Generator Register								0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	Address Mask Register										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: I2C2 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C2RCV	0210	—	—	—	—	—	—	—	—	Receive Register								0000
I2C2TRN	0212	—	—	—	—	—	—	—	—	Transmit Register								00FF
I2C2BRG	0214	—	—	—	—	—	—	—	—	Baud Rate Generator Register								0000
I2C2CON	0216	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C2ADD	021A	—	—	—	—	—	—	Address Register										0000
I2C2MSK	021C	—	—	—	—	—	—	Address Mask Register										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 FOR dsPIC33FJXXXGP506A/510A/706A/708A/710A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets			
	0400-041E	See definition when WIN = x																			
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000			
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000			
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000			
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000			
C1RXM0SID	0430	SID<10:3>								SID<2:0>				—	MIDE	—	EID<17:16>		xxxx		
C1RXM0EID	0432	EID<15:8>								EID<7:0>											xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>				—	MIDE	—	EID<17:16>		xxxx		
C1RXM1EID	0436	EID<15:8>								EID<7:0>											xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>				—	MIDE	—	EID<17:16>		xxxx		
C1RXM2EID	043A	EID<15:8>								EID<7:0>											xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF0EID	0442	EID<15:8>								EID<7:0>											xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF1EID	0446	EID<15:8>								EID<7:0>											xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF2EID	044A	EID<15:8>								EID<7:0>											xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF3EID	044E	EID<15:8>								EID<7:0>											xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF4EID	0452	EID<15:8>								EID<7:0>											xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF5EID	0456	EID<15:8>								EID<7:0>											xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF6EID	045A	EID<15:8>								EID<7:0>											xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF7EID	045E	EID<15:8>								EID<7:0>											xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF8EID	0462	EID<15:8>								EID<7:0>											xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF9EID	0466	EID<15:8>								EID<7:0>											xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>				—	EXIDE	—	EID<17:16>		xxxx		
C1RXF10EID	046A	EID<15:8>								EID<7:0>											xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: ECAN2 REGISTER MAP WHEN C2CTRL1.WIN = 1 FOR dsPIC33FJXXXGP706A/708A/710A DEVICES ONLY (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2RXF10EID	056A	EID<15:8>								EID<7:0>								xxxx
C2RXF11SID	056C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C2RXF11EID	056E	EID<15:8>								EID<7:0>								xxxx
C2RXF12SID	0570	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C2RXF12EID	0572	EID<15:8>								EID<7:0>								xxxx
C2RXF13SID	0574	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C2RXF13EID	0576	EID<15:8>								EID<7:0>								xxxx
C2RXF14SID	0578	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C2RXF14EID	057A	EID<15:8>								EID<7:0>								xxxx
C2RXF15SID	057C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C2RXF15EID	057E	EID<15:8>								EID<7:0>								xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJXXXGPX06A/X08A/X10A

5.4.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase page that contains the desired row. The general process is:

1. Read eight rows of program memory (512 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block (see Example 5-1):
 - a) Set the NVMOP bits (NVMCON<3:0>) to '0010' to configure for block erase. Set the ERASE bit (NVMCON<6>) and the WREN bit (NVMCON<14>).
 - b) Write the starting address of the page to be erased into the TBLPAG and W registers.
 - c) Write 0x55 to NVMKEY.
 - d) Write 0xAA to NVMKEY.
 - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 64 instructions from data RAM into the program memory buffers (see Example 5-2).
5. Write the program block to Flash memory:
 - a) Set the NVMOP bits to '0001' to configure for row programming. Clear the ERASE bit and set the WREN bit.
 - b) Write 0x55 to NVMKEY.
 - c) Write 0xAA to NVMKEY.
 - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
6. Repeat steps 4 and 5, using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG, until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as shown in Example 5-3.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY PAGE

```
; Set up NVMCON for block erase operation
MOV    #0x4042, W0          ;
MOV    W0, NVMCON           ; Initialize NVMCON
; Init pointer to row to be ERASED
MOV    #tblpage(PROG_ADDR), W0 ;
MOV    W0, TBLPAG           ; Initialize PM Page Boundary SFR
MOV    #tbloffset(PROG_ADDR), W0 ; Initialize in-page EA[15:0] pointer
TBLWTL W0, [W0]             ; Set base address of erase block
DISI    #5                  ; Block all interrupts with priority <7
                                ; for next 5 instructions

MOV    #0x55, W0
MOV    W0, NVMKEY           ; Write the 55 key
MOV    #0xAA, W1
MOV    W1, NVMKEY           ; Write the AA key
BSET    NVMCON, #WR         ; Start the erase sequence
NOP                                ; Insert two NOPs after the erase
NOP                                ; command is asserted
```

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TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC 1
22	14	0x000030	0x000130	DMA1 – DMA Channel 1
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	ADC2 – ADC 2
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	DMA2 – DMA Channel 2
33	25	0x000046	0x000146	OC3 – Output Compare 3
34	26	0x000048	0x000148	OC4 – Output Compare 4
35	27	0x00004A	0x00014A	T4 – Timer4
36	28	0x00004C	0x00014C	T5 – Timer5
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	U2RX – UART2 Receiver
39	31	0x000052	0x000152	U2TX – UART2 Transmitter
40	32	0x000054	0x000154	SPI2E – SPI2 Error
41	33	0x000056	0x000156	SPI1 – SPI1 Transfer Done
42	34	0x000058	0x000158	C1RX – ECAN1 Receive Data Ready
43	35	0x00005A	0x00015A	C1 – ECAN1 Event
44	36	0x00005C	0x00015C	DMA3 – DMA Channel 3
45	37	0x00005E	0x00015E	IC3 – Input Capture 3
46	38	0x000060	0x000160	IC4 – Input Capture 4
47	39	0x000062	0x000162	IC5 – Input Capture 5
48	40	0x000064	0x000164	IC6 – Input Capture 6
49	41	0x000066	0x000166	OC5 – Output Compare 5
50	42	0x000068	0x000168	OC6 – Output Compare 6
51	43	0x00006A	0x00016A	OC7 – Output Compare 7
52	44	0x00006C	0x00016C	OC8 – Output Compare 8
53	45	0x00006E	0x00016E	Reserved

7.3 Interrupt Control and Status Registers

dsPIC33FJXXGPX06A/X08A/X10A devices implement a total of 30 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFS0 through IFS4
- IEC0 through IEC4
- IPC0 through IPC17
- INTTREG

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a Status bit, which is set by the respective peripherals or external signal and is cleared via software.

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPC registers are used to set the interrupt priority level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into vector number (VECNUM<6:0>) and Interrupt level bits (ILR<3:0>) in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0>, and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt priority level. The user can change the current CPU priority level by writing to the IPL bits.

The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-1 through Register 7-32.

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REGISTER 7-21: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T4IP<2:0>			—	OC4IP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	OC3IP<2:0>			—	DMA2IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T4IP<2:0>:** Timer4 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OC4IP<2:0>:** Output Compare Channel 4 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **OC3IP<2:0>:** Output Compare Channel 3 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DMA2IP<2:0>:** DMA Channel 2 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

dsPIC33FJXXXGPX06A/X08A/X10A

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IRQSEL6 ⁽²⁾	IRQSEL5 ⁽²⁾	IRQSEL4 ⁽²⁾	IRQSEL3 ⁽²⁾	IRQSEL2 ⁽²⁾	IRQSEL1 ⁽²⁾	IRQSEL0 ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA request

bit 14-7 **Unimplemented:** Read as '0'

bit 6-0 **IRQSEL<6:0>:** DMA Peripheral IRQ Number Select bits⁽²⁾

1111111 = DMAIRQ127 selected to be Channel DMAREQ

•

•

•

0000000 = DMAIRQ0 selected to be Channel DMAREQ

Note 1: The FORCE bit cannot be cleared by the user. The FORCE bit is cleared by hardware when the forced DMA transfer is complete.

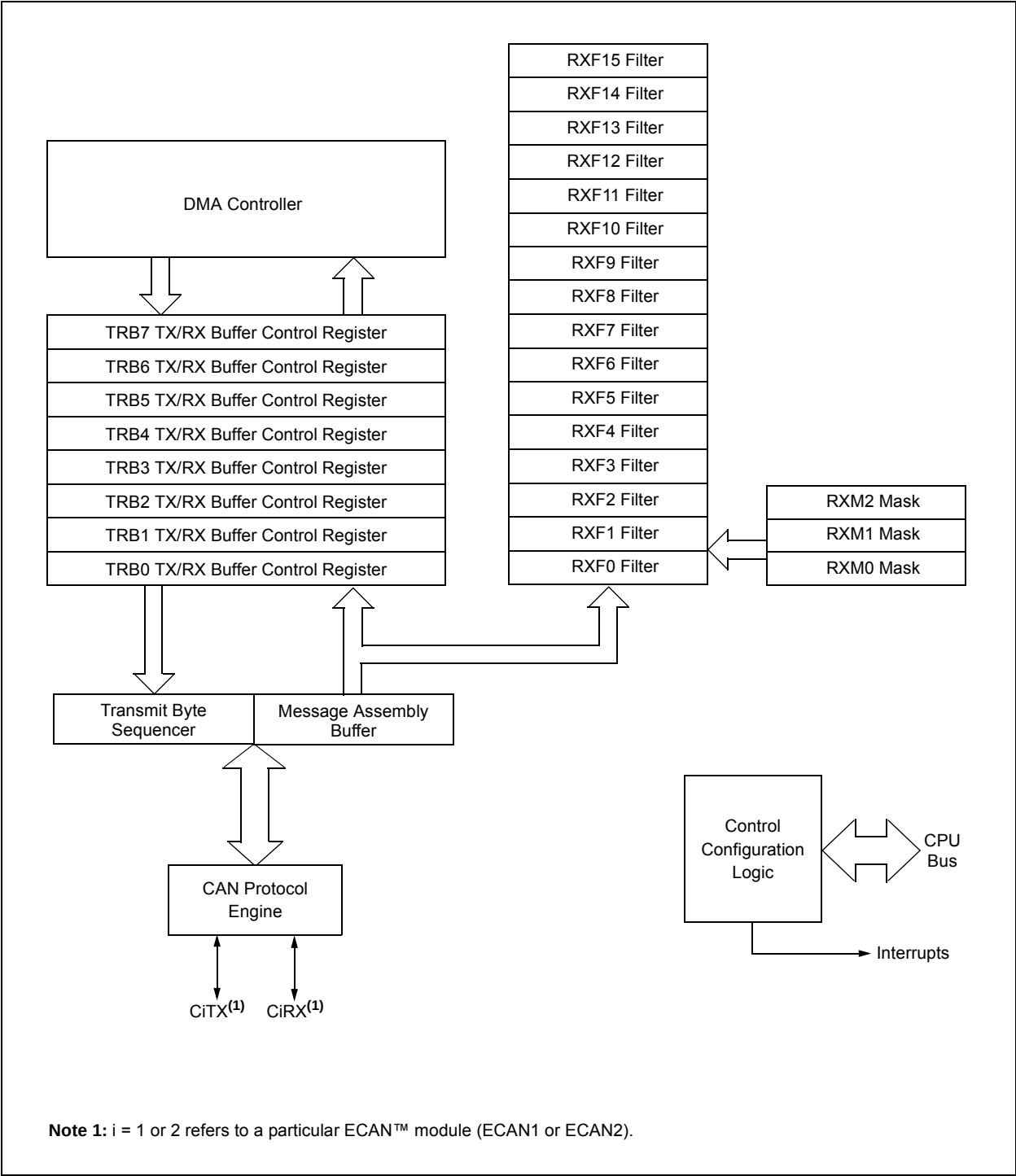
2: Please see Table 8-1 for a complete listing of IRQ numbers for all interrupt sources.

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NOTES:

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FIGURE 19-1: ECAN™ MODULE BLOCK DIAGRAM



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REGISTER 19-13: CiBUFNT2: ECAN™ FILTER 4-7 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F7BP<3:0>**: RX Buffer Written when Filter 7 Hits bits
 1111 = Filter hits received in RX FIFO buffer
 1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1
 0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>**: RX Buffer Written when Filter 6 Hits bits
 1111 = Filter hits received in RX FIFO buffer
 1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1
 0000 = Filter hits received in RX Buffer 0

bit 7-4 **F5BP<3:0>**: RX Buffer Written when Filter 5 Hits bits
 1111 = Filter hits received in RX FIFO buffer
 1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1
 0000 = Filter hits received in RX Buffer 0

bit 3-0 **F4BP<3:0>**: RX Buffer Written when Filter 4 Hits bits
 1111 = Filter hits received in RX FIFO buffer
 1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1
 0000 = Filter hits received in RX Buffer 0

dsPIC33FJXXXGPX06A/X08A/X10A

TABLE 22-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
FPWRT<2:0>	FPOR	Immediate	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled
JTAGEN	FICD	Immediate	JTAG Enable bits 1 = JTAG enabled 0 = JTAG disabled
ICS<1:0>	FICD	Immediate	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved

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TABLE 25-8: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Parameter No.	Typical ⁽²⁾	Max	Doze Ratio	Units	Conditions		
Doze Current (I _{DOZE}) ⁽¹⁾							
DC73a	11	35	1:2	mA	-40°C	3.3V	40 MIPS
DC73f	11	30	1:64	mA			
DC73g	11	30	1:128	mA			
DC70a	42	50	1:2	mA	+25°C	3.3V	40 MIPS
DC70f	26	30	1:64	mA			
DC70g	25	30	1:128	mA			
DC71a	41	50	1:2	mA	+85°C	3.3V	40 MIPS
DC71f	25	30	1:64	mA			
DC71g	24	30	1:128	mA			
DC72a	42	50	1:2	mA	+125°C	3.3V	40 MIPS
DC72f	26	30	1:64	mA			
DC72g	25	30	1:128	mA			

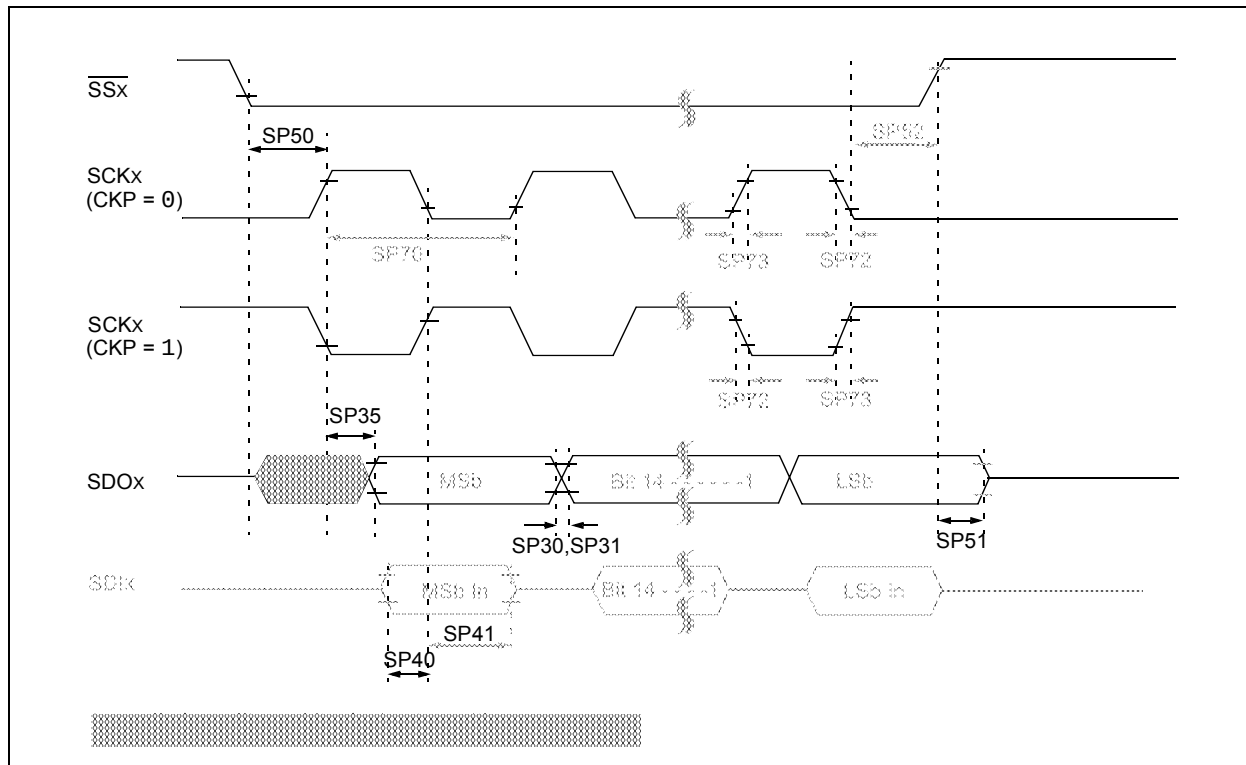
Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail with overshoot/undershoot < 250 mV
- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}} = \text{VDD}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing `while(1)` statement
- JTAG is disabled

2: Data in the "Typ" column is at 3.3V, $+25^{\circ}\text{C}$ unless otherwise stated.

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FIGURE 25-15: SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



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TABLE 26-9: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature						
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	LPRC @ 32.768 kHz ⁽¹⁾						
HF21	LPRC	-70 ⁽²⁾	—	+70 ⁽²⁾	%	$-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$	

Note 1: Change of LPRC frequency as VDD changes.

2: Characterized but not tested.

TABLE 26-10: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	—	—	ns	—
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 26-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns	—
HSP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	35	—	—	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	—	—	ns	—
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

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TABLE 26-14: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Reference Inputs							
HAD08	IREF	Current Drain	—	250	600	μA	ADC operating, See Note 1
			—	—	50	μA	ADC off, See Note 1

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but are not tested in manufacturing.

TABLE 26-15: ADC MODULE SPECIFICATIONS (12-BIT MODE)⁽³⁾

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾							
AD23a	GERR	Gain Error	—	5	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24a	E0FF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF- ⁽¹⁾							
AD23a	GERR	Gain Error	2	10	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24a	E0FF	Offset Error	2	5	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (12-bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	—

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 26-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽³⁾

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾							
AD23b	GERR	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24b	E0FF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF- ⁽¹⁾							
AD23b	GERR	Gain Error	—	7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24b	E0FF	Offset Error	—	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (10-bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	—

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

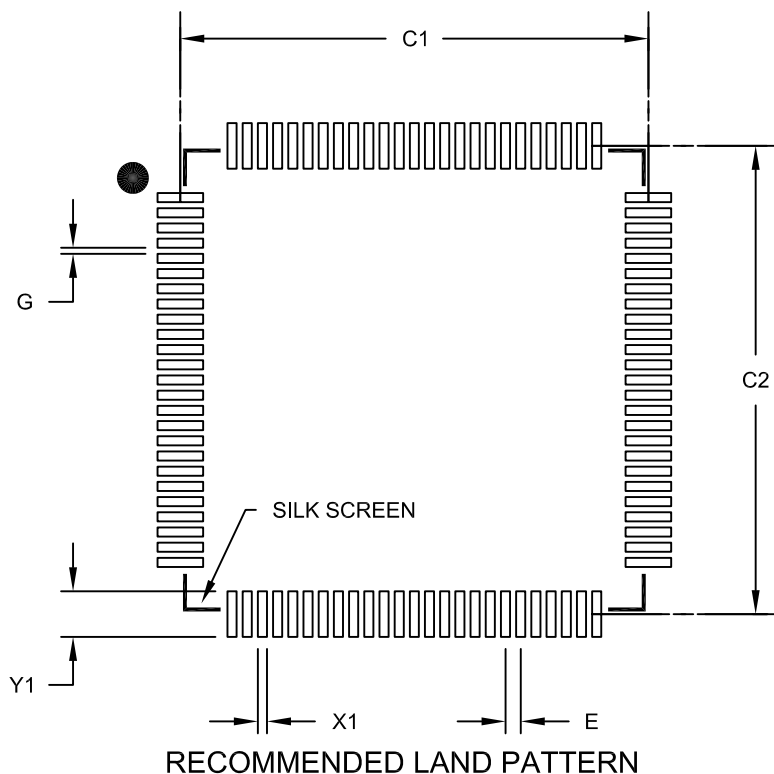
2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

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100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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