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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj256gp510at-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name	Pin Type	Buffer Type	Description
AN0-AN31	I	Analog	Analog input channels.
AVDD	Р	Р	Positive supply for analog modules. This pin must be connected at all times.
AVss	Р	Р	Ground reference for analog modules.
CLKI CLKO	- 0	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
COFS CSCK	I/O I/O	ST ST	Data Converter Interface frame synchronization pin. Data Converter Interface serial clock input/output pin.
CSDI		ST	Data Converter Interface serial data input pin.
CSDO	0	—	Data Converter Interface serial data output pin.
C1RX		ST	ECAN1 bus receive pin.
C11X C2RX	0	ST ST	ECAN I bus transmit pin. ECAN2 bus receive nin
C2TX	0	_	ECAN2 bus transmit pin.
PGED1	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGEC1	I	ST	Clock input pin for programming/debugging communication channel 1.
PGED2	I/O	ST	Data I/O pin for programming/debugging communication channel 2.
PGEC2	I	ST	Clock input pin for programming/debugging communication channel 2.
PGED3	1/0	SI	Data I/O pin for programming/debugging communication channel 3.
PGECS	1	51 0T	Clock input pin for programming/debugging communication channel 3.
	1	51	
		SI	External Interrupt 0.
		ST	External interrupt 1.
INT3	1	ST	External interrupt 3
INT4	I	ST	External interrupt 4.
MCLR	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OCFA	I	ST	Compare Fault A input (for Compare Channels 1, 2, 3 and 4).
OCFB	I	ST	Compare Fault B input (for Compare Channels 5, 6, 7 and 8).
OC1-OC8	0	—	Compare outputs 1 through 8.
OSC1	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
RA0-RA7	I/O	ST	PORTA is a bidirectional I/O port.
RA9-RA10	I/O	ST	
RA12-RA15	I/O	ST	
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1-RC4 RC12-RC15	1/0 1/0	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE7	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8	I/O	ST	PORTF is a bidirectional I/O port.
RF12-RF13	1/0	S compatible	a input or output: Analog = Analog input: D = Power

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Legend: CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; P = Pow O = Output; I = Input

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to \leq 8 MHz for start-up with PLL enabled to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration word.

2.8 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as "digital" pins, by setting all bits in the ADPCFG and ADPCFG2 registers.

The bits in the registers that correspond to the A/D pins that are initialized by ICD 3 or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must clear the corresponding bits in the ADPCFG and ADPCFG2 registers during initialization of the ADC module.

When ICD 3 or REAL ICE is used as a programmer, the user application firmware must correctly configure the ADPCFG and ADPCFG2 registers. Automatic initialization of these registers is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic '0', which may affect user application functionality.

2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic-low state.

Alternatively, connect a 1k to 10k resistor between Vss and the unused pins.

3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value which is sign-extended to 40 bits. Integer data is inherently represented as a signed two's complement value, where the Most Significant bit (MSb) is defined as a sign bit. Generally speaking, the range of an N-bit two's complement integer is -2^{N-1} to 2^{N-1} - 1. For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0. For a 32-bit integer, the data is -2,147,483,648 (0x8000 0000) range to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a two's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit two's complement fraction with this implied radix point is -1.0 to $(1 - 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518×10^{-5} . In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product which has a precision of 4.65661×10^{-10} .

The same multiplier is used to support the MCU multiply instructions which include integer 16-bit signed, unsigned and mixed sign multiplies.

The MUL instruction may be directed to use byte or word sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/ subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled via the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true, or complement data into the other input. In the case of addition, the Carry/Borrow input is active-high and the other input is true data (not complemented), whereas in the case of subtraction, the Carry/Borrow input is active-low and the other input is complemented. The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block which controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described above and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS register bits have been provided to support saturation and overflow; they are:

- OA: AccA overflowed into guard bits
- OB: AccB overflowed into guard bits
- SA: AccA saturated (bit 31 overflow and saturation) or

AccA overflowed into guard bits and saturated (bit 39 overflow and saturation)

 SB: AccB saturated (bit 31 overflow and saturation) or

AccB overflowed into guard bits and saturated (bit 39 overflow and saturation)

- OAB: Logical OR of OA and OB
- SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when set and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register (refer to **Section 7.0 "Interrupt Controller"**) are set. This allows the user to take immediate action, for example, to correct system gain.

TABLE 4-27: PORTC REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02CC	TRISC15	TRISC14	TRISC13	TRISC12	_	_	_	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	_	F01E
PORTC	02CE	RC15	RC14	RC13	RC12	_	_	_	_	_	—	—	RC4	RC3	RC2	RC1	_	xxxx
LATC	02D0	LATC15	LATC14	LATC13	LATC12	_	_	_	-		—	—	LATC4	LATC3	LATC2	LATC1	_	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-28: PORTD REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	02D2	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
PORTD	02D4	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	02D6	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	06D2	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-29: PORTE REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	02D8	—	—	—	-	—	_	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
PORTE	02DA	_	_	_	_	_	_	_	_	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
LATE	02DC	_	—	—	—	_	—	_	_	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-30: PORTF REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	02DE	—	—	TRISF13	TRISF12	—	—	—	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	31FF
PORTF	02E0	_	—	RF13	RF12	_	_	_	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
LATF	02E2	_	_	LATF13	LATF12	_	_	_	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
ODCF	06DE	_	_	ODCF13	ODCF12	_	_	_	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit		nented bit, read	I as '0'	
-n = Value at P	OR	'1' = Bit is set		0' = Bit is clear	ared	x = Bit is unkn	iown
h:: 45							
DIT 15		rrupt Nesting L	visable bit				
	0 = Interrupt r	nesting is usat	led				
bit 14	OVAERR: Ac	cumulator A O	verflow Trap F	laq bit			
	1 = Trap was	caused by ove	rflow of Accun	nulator A			
	0 = Trap was	not caused by	overflow of Ac	ccumulator A			
bit 13	OVBERR: Ac	cumulator B O	verflow Trap F	lag bit			
	1 = Trap was	caused by ove	rflow of Accun	nulator B			
bit 10		not caused by	Cotootrophia C		log bit		
DIL 12	1 = Trap was	caused by cat	strophic over	flow of Accum	lator A		
	0 = Trap was	not caused by	catastrophic c	overflow of Acc	umulator A		
bit 11	COVBERR: A	Accumulator B	Catastrophic C	Overflow Trap F	lag bit		
	1 = Trap was	caused by cata	astrophic over	flow of Accumu	lator B		
	0 = Trap was	not caused by	catastrophic c	overflow of Acc	umulator B		
bit 10	OVATE: Accu	mulator A Ove	rflow Trap Ena	able bit			
	1 = Trap over 0 = Trap disal	flow of Accumı bled	ulator A				
bit 9		imulator B Ove	erflow Trap En	able bit			
Site	1 = Trap over	flow of Accum	ulator B				
	0 = Trap disal	bled					
bit 8	COVTE: Cata	strophic Overf	low Trap Enab	ole bit			
	1 = Trap on c 0 = Trap disal	atastrophic ove bled	erflow of Accur	mulator A or B	enabled		
bit 7	SFTACERR:	Shift Accumula	tor Error Statu	ıs bit			
	1 = Math erro	r trap was caus	sed by an inva	ilid accumulato	r shift lator shift		
bit 6	DIVOFRR: Ari	ithmetic Error S	Status bit				
	1 = Math erro	r trap was caus	sed by a divide	e by zero			
	0 = Math erro	r trap was not	caused by a d	ivide by zero			
bit 5	DMACERR: [OMA Controller	Error Status b	bit			
	1 = DMA cont	troller error trap	has occurred	 rrod			
hit 4			Status bit	neu			
	1 = Math erro	r tran has occu	irred				
	0 = Math erro	r trap has not o	occurred				

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	_	—	—	—	
bit 15			·				bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	<u> </u>		INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	ALTIVT: Enab	ble Alternate In	terrupt Vector	lable bit			
	1 = Use alternoise 0 = Use stand	late vector tab	ector table				
bit 14		struction Statu	s bit				
	1 = DISI inst	ruction is active	9				
	0 = DISI inst	ruction is not a	ctive				
bit 13-5	Unimplemen	ted: Read as '	0'				
bit 4	INT4EP: Exte	ernal Interrupt 4	Edge Detect	Polarity Selec	t bit		
	1 = Interrupt o	on negative ed	ge				
1.11.0	0 = Interrupt o	on positive edg	e				
bit 3	INI 3EP: Exte	ernal Interrupt 3	Edge Detect	Polarity Selec	t bit		
	1 = Interrupt 0	on positive edg	ye e				
bit 2	INT2EP: Exte	ernal Interrupt 2	2 Edae Detect	Polarity Selec	t bit		
	1 = Interrupt of	on negative ed	qe				
	0 = Interrupt o	on positive edg	e				
bit 1	INT1EP: Exte	ernal Interrupt 1	Edge Detect	Polarity Selec	t bit		
	1 = Interrupt of	on negative ed	ge				
	0 = Interrupt o	on positive edg	e				
bit 0	INTOEP: Exte	ernal Interrupt C	Edge Detect	Polarity Selec	t bit		
	1 = interrupt (0 = Interrupt (on negative edg	ye e				
		poolaro oug	-				

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

REGISTER 7	7-7: IFS2: I	INTERRUPT	FLAG STAT	US REGIST	ER 2		
R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T6IF	DMA4IF		OC8IF	OC7IF	OC6IF	OC5IF	IC6IF
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15	T6IF: Timer6	Interrupt Flag	Status bit				
	1 = Interrupt i 0 = Interrupt i	request has oc request has no	curred t occurred				
bit 14	DMA4IF: DM	A Channel 4 D	ata Transfer C	omplete Interr	upt Flag Status	bit	
	1 = Interrupt i 0 = Interrupt i	request has oc request has no	curred t occurred				
bit 13	Unimplemen	ted: Read as '	0'				
bit 12	OC8IF: Outpu	ut Compare Ch	annel 8 Interru	upt Flag Status	s bit		
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 11	OC7IF: Outpu	ut Compare Ch	annel 7 Interru	upt Flag Status	s bit		
	1 = Interrupt i 0 = Interrupt i	request has oc request has no	curred t occurred				
bit 10	OC6IF: Outpu	ut Compare Ch	annel 6 Interru	upt Flag Status	s bit		
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 9	OC5IF: Outpu	ut Compare Ch	annel 5 Interru	upt Flag Status	s bit		
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 8	IC6IF: Input C	Capture Chann	el 6 Interrupt F	lag Status bit			
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 7	IC5IF: Input C	Capture Chann	el 5 Interrupt F	lag Status bit			
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 6	IC4IF: Input C	Capture Chann	el 4 Interrupt F	lag Status bit			
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 5	IC3IF: Input C	Capture Chann	el 3 Interrupt F	lag Status bit			
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 4	DMA3IF: DM	A Channel 3 D	ata Transfer C	omplete Interr	upt Flag Status	bit	
	1 = Interrupt ı 0 = Interrupt ı	request has oc request has no	curred t occurred				
bit 3	C1IF: ECAN1	Event Interrup	ot Flag Status	bit			
	1 = Interrupt i 0 = Interrupt i	request has oc request has no	curred t occurred				

REGISTER 7	-33: INTTR	EG: INTERRU	JPT CONT	ROL AND ST	ATUS REGIS	TER	
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	_	—			ILR<	<3:0>	
bit 15		•					bit 8
U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
				VECNUM<6:0	>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown
bit 15-12	Unimplemer	ted: Read as '0	3				
bit 11-8	ILR<3:0>: No	ew CPU Interrup	t Priority Lev	vel bits			
	1111 = CPU	Interrupt Priority	/ Level is 15				
	•						
	•						
	0001 = CPU	Interrupt Priority	/ Level is 1				
	0000 = CPU	Interrupt Priority	Level is 0				
bit 7	Unimplemer	ted: Read as '0	,				
bit 6-0	VECNUM<6:	0>: Vector Numl	ber of Pendi	ing Interrupt bits			
	0111111 = 	nterrupt Vector p	ending is nu	umber 135			
	•		C C				
	•						
	•	nterrunt Vector n	ondina is nu	umber 0			
	0000001 = 1	menupi vector p	renaing is ht				

0000000 = Interrupt Vector pending is number 8

NOTES:

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
			_	—		_	_
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit /							bit C
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-8	Unimpleme	nted: Read as ')'				
bit 7	IVRIE: Invali	d Message Inter	rupt Enable	bit			
	1 = Interrupt	request enable) Ibled				
bit 6	WAKIE: Bus	Wake-up Activi	tv Interrupt F	nable bit			
	1 = Interrupt	request enable	d				
	0 = Interrupt	request not ena	bled				
bit 5	ERRIE: Erro	r Interrupt Enab	le bit				
	1 = Interrupt	request enable) blad				
hit 4		request not ena	ibieu				
bit 2		Almost Full In	orrunt Enabl	o hit			
DIL J	1 = Interrupt	request enable		ebit			
	0 = Interrupt	request not ena	bled				
bit 2	RBOVIE: RX	Buffer Overflov	v Interrupt Ei	nable bit			
	1 = Interrupt	request enable	1 				
1.11.4	0 = Interrupt	request not ena	bled				
bit 1	1 = Interrunt	uffer Interrupt Er	hable bit				
	0 = Interrupt	request not ena	bled				
bit 0	TBIE: TX Bu	ffer Interrupt En	able bit				
	1 = Interrupt	request enable	ł				
	0 = Interrupt	request not ena	bled				

REGISTER 19-7: CIINTE: ECAN™ INTERRUPT ENABLE REGISTER

REGISTER 19-14: CIBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F11BF	P<3:0>			F10E	3P<3:0>	
bit 15							bit 8
R/M_0	R/M/_0	R/M_0	R///-0	R/M/_0	R/M/0	R/M_0	R/M-0
FX/VV-0	FORD	<3.0>	F\/ VV-U	R/W-0	F8R	P<3.05	10/00-0
bit 7	F9DF	<3.0>			FOD	F \3.0>	bit 0
							DILO
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplem	nented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-12 bit 11-8	F11BP<3:0> 1111 = Filter 1110 = Filter 0001 = Filter 0000 = Filter F10BP<3:0> 1111 = Filter 1110 = Filter 0001 = Filter 0000 = Filter	RX Buffer Writ hits received in hits received in hits received in hits received in RX Buffer Writ hits received in hits received in hits received in	ten when Filt RX FIFO bu RX Buffer 14 RX Buffer 1 RX Buffer 0 tten when Filt RX FIFO bu RX FIFO bu RX Buffer 14 RX Buffer 1	er 11 Hits bits ffer 4 er 10 Hits bits ffer 4			
bit 7-4	F9BP<3:0>: 1111 = Filter 1110 = Filter • • • • • • • • • • • • • • • • • • •	RX Buffer Writte hits received in hits received in hits received in hits received in	en when Filte RX FIFO bu RX Buffer 14 RX Buffer 1 RX Buffer 1 RX Buffer 0	r 9 Hits bits ffer 4			
bit 3-0	F8BP<3:0>: 1111 = Filter 1110 = Filter • • • • • • • • • • • • • • • • • • •	RX Buffer Writte hits received in hits received in hits received in hits received in	en when Filte RX FIFO bu RX Buffer 14 RX Buffer 1 RX Buffer 1 RX Buffer 0	r 8 Hits bits ffer 4			

REGISTER 19-18: CiFMSKSEL1: ECAN™ FILTER 7-0 MASK SELECTION REGISTER

R/V	V-0 R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F7MSK<1:0>	F6MSł	<<1:0>	F5MS	K<1:0>	F4MS	K<1:0>
bit 15							bit 8
		D 444 A	5				
R/V	V-0 R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 7	F31013K < 1.02	FZIVIST	<1.0>	F IIVIS	NS1.02	FUIMS	hit 0
							511.0
Legen	d:						
R = Re	adable bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Va	lue at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15-1	 F7MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta 	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 7 b gisters contair gisters contair gisters contair	it 1 mask 1 mask 1 mask			
bit 13-1	2 F6MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 6 b gisters contair gisters contair gisters contair	it n mask n mask n mask			
bit 11-1	0 F5MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source ed; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 5 b gisters contair gisters contair gisters contair	it n mask n mask n mask			
bit 9-8	F4MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source ed; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 4 b gisters contair gisters contair gisters contair	it n mask n mask n mask			
bit 7-6	F3MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source ed; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 3 b gisters contair gisters contair gisters contair	it n mask n mask n mask			
bit 5-4	F2MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 2 bi gisters contair gisters contair gisters contair	it n mask n mask n mask			
bit 3-2	F1MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 1 b gisters contair gisters contair gisters contair	it n mask n mask n mask			
bit 1-0	F0MSK<1:0> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	: Mask Source ed; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	e for Filter 0 b gisters contair gisters contair gisters contair	it n mask n mask n mask			

Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers are located in DMA RAM.

REGISTER 19-27: CITRBnSID: ECAN™ BUFFER n STANDARD IDENTIFIER (n = 0, 1, ..., 31)

- - SID<10:6> bit 15 bit bit	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
bit 15 bi	—	—	—	SID<10:6>					
	bit 15					bit 8			
R/W-x R/W-x R/W-x R/W-x R/W-x R/W-x R/W-x									
	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	

	SID<5:0>	SRR	IDE
bit 7			bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-2	SID<10:0>: Standard Identifier bits
bit 1	SRR: Substitute Remote Request bit
	 1 = Message will request remote transmission 0 = Normal message
bit 0	IDE: Extended Identifier bit
	1 = Message will transmit extended identifier

0 = Message will transmit standard identifier

REGISTER 19-28: CITRBnEID: ECAN™ BUFFER n EXTENDED IDENTIFIER (n = 0, 1, ..., 31)

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—		—	—		EID<	17:14>	
bit 15						bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID<	:13:6>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits

REGISTER 20-3: DCICON3: DCI CONTROL REGISTER 3

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—		BCG	i<11:8>	
bit 15						bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			BCG	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	e bit W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-12 Unimplemented: Read as '0'

bit 11-0 BCG<11:0>: DCI Bit Clock Generator Control bits

REGISTER 21-4: ADxCON4: ADCx CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	_	_	_	_		DMABL<2:0>	

bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as 'O'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 Unimplemented: Read as '0'

bit 7

bit 2-0

DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits

111 = Allocates 128 words of buffer to each analog input

110 = Allocates 64 words of buffer to each analog input

101 = Allocates 32 words of buffer to each analog input

100 = Allocates 16 words of buffer to each analog input

011 = Allocates 8 words of buffer to each analog input

010 = Allocates 4 words of buffer to each analog input

001 = Allocates 2 words of buffer to each analog input

000 = Allocates 1 word of buffer to each analog input

Base Instr	Assembly		Assembly Syntax	Description	# of Words	# of	Status Flags
#	wittentionic		C 10 1 4		worus	Cycles	Allecteu
10	BISC	BISC	I,#DIC4	Bit lest I, Skip II Clear	I	(2 or 3)	None
		BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST	f,#bit4	Bit Test f	1	1	Z
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	С
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C	Ws,Wb	Bit Test Ws <wb> to C</wb>	1	1	С
		BTST.Z	Ws,Wb	Bit Test Ws <wb> to Z</wb>	1	1	Z
13	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	С
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL	lit23	Call subroutine	2	2	None
		CALL	Wn	Call indirect subroutine	1	2	None
15	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WREG = 0x0000	1	1	None
		CLR	Ws	Ws = 0x0000	1	1	None
		CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM	f	f = f	1	1	N,Z
		COM	f,WREG	WREG = \overline{f}	1	1	N,Z
		COM	Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit5	Compare Wb with lit5	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit5	Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,Ws	Compare Wb with Ws, with Borrow $(Wb - Ws - C)$	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ	Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT	Wb, Wn	Compare Wb with Wn, skip if >	1	(2 or 3)	None
23	CPSLT	CPSLT	Wb, Wn	Compare Wb with Wn, skip if <	1	(2 or 3)	None
24	CPSNE	CPSNE	Wb, Wn	Compare Wb with Wn, skip if ≠	1	(2 or 3)	None
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC.N.OV.Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC.N.OV.Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N.OV.Z
27	DEC2	DEC2	f	f = f - 2	1	1	C,DC,N,OV.Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None

TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

TABLE 25-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Parameter No. ⁽³⁾	Typical ⁽²⁾	Мах	Units	Conditions				
Operating Current (IDD) ⁽¹⁾								
DC20d	27	30	mA	-40°C				
DC20a	27	30	mA	+25°C	2 2)/			
DC20b	27	30	mA	+85°C	3.3V			
DC20c	27	35	mA	+125°C				
DC21d	36	40	mA	-40°C		16 MIPS		
DC21a	37	40	mA	+25°C	2 2\/			
DC21b	38	45	mA	+85°C	5.5 V			
DC21c	39	45	mA	+125°C				
DC22d	43	50	mA	-40°C				
DC22a	46	50	mA	+25°C	2 2\/			
DC22b	46	55	mA	+85°C	5.5 V	20 WIF 3		
DC22c	47	55	mA	+125°C				
DC23d	65	70	mA	-40°C				
DC23a	65	70	mA	+25°C	2 2\/	30 MIDS		
DC23b	65	70	mA	+85°C	3.3V	30 MIF 3		
DC23c	65	70	mA	+125°C				
DC24d	84	90	mA	-40°C				
DC24a	84	90	mA	+25°C	2 2\/			
DC24b	84	90	mA	+85°C	5.5V	40 WIF 3		
DC24c	84	90	mA	+125°C				

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing while(1) statement
- · JTAG is disabled
- **2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: These parameters are characterized but not tested in manufacturing.

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions			
ADC Accuracy (10-bit Mode) - Measurements with external VREF+/VREF-										
AD20b	Nr	Resolution	1	0 data bi	its	bits				
AD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD22b	DNL	Differential Nonlinearity	>-1	_	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD23b	Gerr	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD24b	EOFF	Offset Error	— 2 5		LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
AD25b	D25b — Monotonicity ⁽¹⁾ — —					_	Guaranteed			
		ADC Accuracy (10-bit Mod	de) - Measu	rements	with interna	I VREF+	NREF-			
AD20b	Nr	Resolution	1	0 data bi	its	bits				
AD21b	INL	Integral Nonlinearity	-1	—	+1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD22b	DNL	Differential Nonlinearity	>-1	-	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD23b	Gerr	Gain Error	—	7	15	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD24b	EOFF	Offset Error	—	3	7	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V			
AD25b	—	Monotonicity ⁽¹⁾				_	Guaranteed			
		Dynamic	Performan	ce (10-bi	it Mode)	•				
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB	—			
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	—	dB				
AD32b	SFDR	Spurious Free Dynamic Range	72	_		dB	_			
AD33b	Fnyq	Input Signal Bandwidth	—	—	550	kHz	—			
AD34b	ENOB	Effective Number of Bits	9.16	9.4		bits				

TABLE 25-43: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽²⁾

Note 1: The ADC conversion result never decreases with an increase in the input voltage, and has no missing codes.

2: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

Revision C (March 2011)

This revision includes typographical and formatting changes throughout the data sheet text. In addition, all instances of VDDCORE have been removed.

All other major changes are referenced by their respective section in the following table.

TABLE B-2:	MAJOR	SECTION	UPDATES
		02011011	0. 5/1150

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers"	Updated the title of Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)".
	The frequency limitation for device PLL start-up conditions was updated in Section 2.7 "Oscillator Value Conditions on Device Start-up ".
	The second paragraph in Section 2.9 "Unused I/Os" was updated.
Section 4.0 "Memory Organization"	The All Resets values for the following SFRs in the Timer Register Map were changed (see Table 4-6): • TMR1 • TMR2 • TMR3 • TMR4 • TMR5 • TMR6 • TMR7 • TMR8 • TMR9
Section 9.0 "Oscillator Configuration"	Added Note 3 to the OSCCON: Oscillator Control Register (see Register 9-1).
	Added Note 2 to the CLKDIV: Clock Divisor Register (see Register 9-2).
	Added Note 1 to the PLLFBD: PLL Feedback Divisor Register (see Register 9-3).
	Added Note 2 to the OSCTUN: FRC Oscillator Tuning Register (see Register 9-4).
Section 21.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	Updated the VREFL references in the ADC1 module block diagram (see Figure 21-1).
Section 22.0 "Special Features"	Added a new paragraph and removed the third paragraph in Section 22.1 "Configuration Bits" .
	Added the column "RTSP Effects" to the Configuration Bits Descriptions (see Table 22-2).

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DSADR (Most Recent DMA RAM Address) I2CxCON (I2Cx Control) I2CxMSK (I2Cx Slave Mode Address Mask) I2CxSTAT (I2Cx Status) ICxCON (Input Capture x Control) IEC0 (Interrupt Enable Control 0) IEC1 (Interrupt Enable Control 1)	144 190 194 192 176 106 108
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