## What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "[Embedded - Microcontrollers](#)"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 40 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | AC'97, Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 32x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gp310a-e-pf |

**FIGURE 3-3:** **DSP ENGINE BLOCK DIAGRAM**
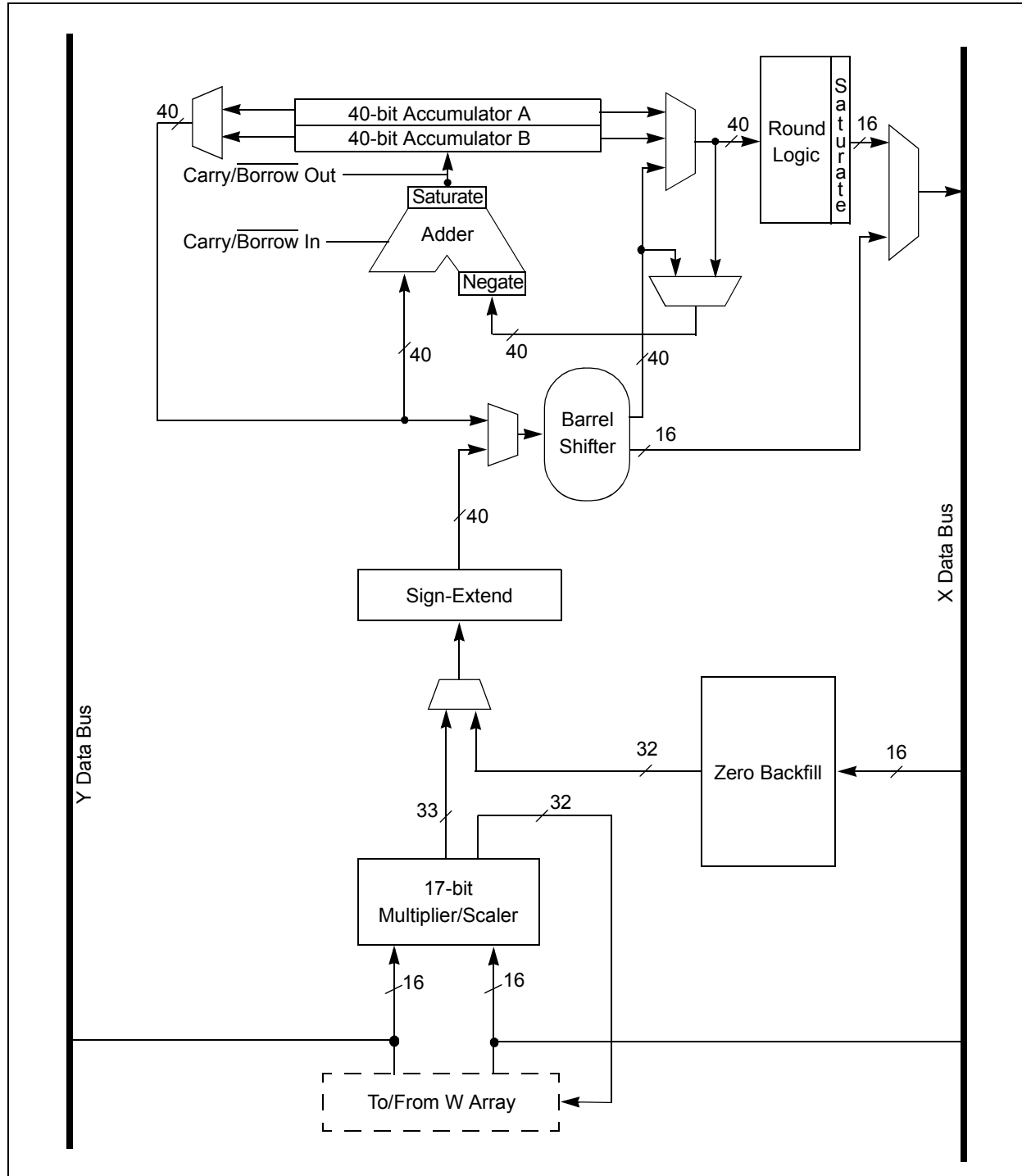
## 4.6 Interfacing Program and Data Memory Spaces

The dsPIC33FJXXXGPX06A/X08A/X10A architecture uses a 24-bit wide program space and a 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33FJXXXGPX06A/X08A/X10A architecture provides two methods by which program space can be accessed during operation:

• Using table instructions to access individual bytes or words anywhere in the program space
• Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. It can only access the least significant word of the program word.

### 4.6.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Page register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 8-bit Program Space Visibility register (PSVPAG) is used to define a 16K word page in the program space. When the Most Significant bit of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area.

Table 4-37 and Figure 4-9 show how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

**TABLE 4-37: PROGRAM SPACE ADDRESS CONSTRUCTION**

| Access Type | Access Space | Program Space Address | | | | |
|---|---|---|---|---|---|---|
| | | **<23>** | **<22:16>** | **<15>** | **<14:1>** | **<0>** |
| Instruction Access (Code Execution) | User | 0 | PC<22:1> | | | 0 |
| | | 0xx  xxxx  xxxx  xxxx  xxxx xxx0 | | | | |
| TBLRD/TBLWT (Byte/Word Read/Write) | User | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 0xxx xxxx    xxxx xxxx xxxx xxxx | | | | |
| | Configuration | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 1xxx xxxx    xxxx xxxx xxxx xxxx | | | | |
| Program Space Visibility (Block Remap/Read) | User | 0 | PSVPAG<7:0> | Data EA<14:0>[1] | | |
| | | 0     xxxx xxxx    xxx xxxx xxxx xxxx | | | | |

**Note 1:** Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

## 6.0 RESET

**Note 1:** This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Reset"** (DS70192) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

• POR: Power-on Reset
• BOR: Brown-out Reset
• MCLR: Master Clear Pin Reset
• SWR: RESET Instruction
• WDT: Watchdog Timer Reset
• TRAPR: Trap Conflict Reset
• IOPUWR: Illegal Opcode and Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

**Note:** Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1). A POR will clear all bits, except for the POR bit (RCON<0>), that are set. The user can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

**Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

**FIGURE 6-1:** **RESET SYSTEM BLOCK DIAGRAM**
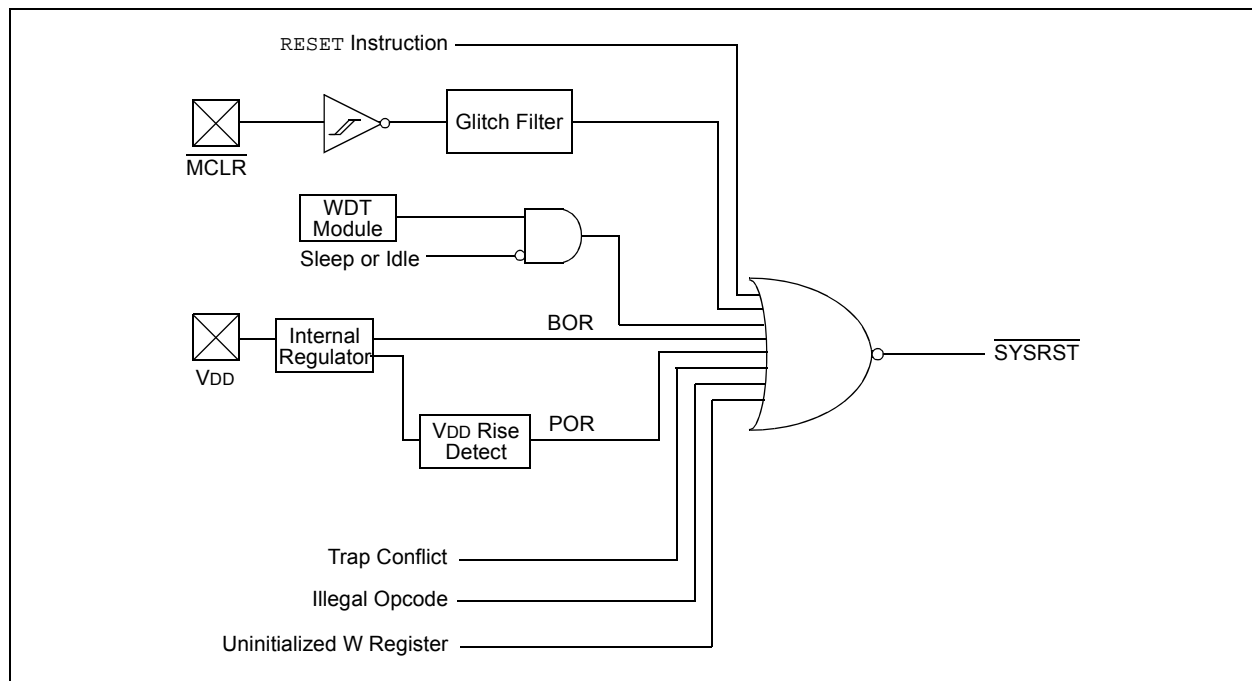
## REGISTER 6-1: RCON: RESET CONTROL REGISTER[1]

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|-------|-------|-----|-----|-----|-----|-----|-------|
| TRAPR | IOPUWR | — | — | — | — | — | VREGS[3] |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EXTR | SWR | SWDTEN[2] | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15　　**TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14　　**IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-9　**Unimplemented:** Read as '0'

bit 8　　**VREGS:** Voltage Regulator Standby During Sleep bit[3]
1 = Voltage Regulator is active during Sleep mode
0 = Voltage Regulator goes into standby mode during Sleep

bit 7　　**EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6　　**SWR:** Software Reset (Instruction) Flag bit
1 = A `RESET` instruction has been executed
0 = A `RESET` instruction has not been executed

bit 5　　**SWDTEN:** Software Enable/Disable of WDT bit[2]
1 = WDT is enabled
0 = WDT is disabled

bit 4　　**WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3　　**SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2　　**IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1　　**BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

**Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**3:** For dsPIC33FJ256GPX06A/X08A/X10A devices, this bit is unimplemented and reads back programmed value.

# dsPIC33FJXXXGPX06A/X08A/X10A

## 7.0 INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Interrupts"** (DS70184) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXGPX06A/X08A/X10A interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJXXXGPX06A/X08A/X10A CPU. It has the following features:

- Up to eight processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

### 7.1 Interrupt Vector Table

The Interrupt Vector Table is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of eight non-maskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this priority is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address.

dsPIC33FJXXXGPX06A/X08A/X10A devices implement up to 67 unique interrupts and five non-maskable traps. These are summarized in Table 7-1 and Table 7-2.

### 7.1.1 ALTERNATE VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

### 7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJXXXGPX06A/X08A/X10A device clears its registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. The user programs a GOTO instruction at the Reset address which redirects program execution to the appropriate start-up routine.

> **Note:** Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

**REGISTER 7-6:      IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)**

bit 3          **CNIF:** Input Change Notification Interrupt Flag Status bit
               1 = Interrupt request has occurred
               0 = Interrupt request has not occurred

bit 2          **Unimplemented:** Read as '0'

bit 1          **MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit
               1 = Interrupt request has occurred
               0 = Interrupt request has not occurred

bit 0          **SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit
               1 = Interrupt request has occurred
               0 = Interrupt request has not occurred

**REGISTER 7-9:    IFS4: INTERRUPT FLAG STATUS REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|-------|-------|-------|-------|-----|-------|-------|-----|
| C2TXIF | C1TXIF | DMA7IF | DMA6IF | — | U2EIF | U1EIF | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared          x = Bit is unknown |

bit 15-8      **Unimplemented:** Read as '0'

bit 7         **C2TXIF:** ECAN2 Transmit Data Request Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6         **C1TXIF:** ECAN1 Transmit Data Request Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5         **DMA7IF:** DMA Channel 7 Data Transfer Complete Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4         **DMA6IF:** DMA Channel 6 Data Transfer Complete Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3         **Unimplemented:** Read as '0'

bit 2         **U2EIF:** UART2 Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1         **U1EIF:** UART1 Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0         **Unimplemented:** Read as '0'

**REGISTER 7-23:    IPC8: INTERRUPT PRIORITY CONTROL REGISTER 8**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|-----|-------|-------|-------|-----|-------|-------|-------|
| — | C1IP<2:0> | | | — | C1RXIP<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|-----|-------|-------|-------|-----|-------|-------|-------|
| — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15      **Unimplemented:** Read as '0'

bit 14-12   **C1IP<2:0>:** ECAN1 Event Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11      **Unimplemented:** Read as '0'

bit 10-8    **C1RXIP<2:0>:** ECAN1 Receive Data Ready Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7       **Unimplemented:** Read as '0'

bit 6-4     **SPI2IP<2:0>:** SPI2 Event Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3       **Unimplemented:** Read as '0'

bit 2-0     **SPI2EIP<2:0>:** SPI2 Error Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

## 9.2 Clock Switching Operation

Applications are free to switch between any of the four clock sources (Primary, LP, FRC and LPRC) under software control at any time. To limit the possible side effects that could result from this flexibility, dsPIC33FJXXXGPX06A/X08A/X10A devices have a safeguard lock built into the switch process.

> **Note:** Primary Oscillator mode has three different submodes (XT, HS and EC) which are determined by the POSCMD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

### 9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the Configuration register must be programmed to '0'. (Refer to **Section 22.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled. It is held at '0' at all times.

### 9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.

2. If a valid clock switch has been initiated, the status bits, LOCK (OSCCON<5>) and CF (OSCCON<3>) are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware waits until the Oscillator Start-up Timer (OST) expires. If the new source is using the PLL, the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM are enabled) or LP (if LPOSCEN remains set).

> **Note 1:** The processor continues to execute code throughout the clock switching sequence. Timing sensitive code should not be executed during this time.
>
> **2:** Direct clock switches between any primary oscillator mode with PLL and FRC-PLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
>
> **3:** Refer to **Section 7. "Oscillator"** (DS70186) in the *"dsPIC33F/PIC24H Family Reference Manual"* for details.

## 9.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

In the event of an oscillator failure, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. Then the application program can either attempt to restart the oscillator or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

If the PLL multiplier is used to scale the system clock, the internal FRC is also multiplied by the same factor on clock failure. Essentially, the device switches to FRC with PLL on a clock failure.

## 13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

> **Note 1:** This data sheet summarizes the features of the dsPIC33FJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. "Timers"** (DS70205) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-bit Timers (e.g., Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit Timer
- Single 32-bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)
- ADC2 Event Trigger (Timer4/5 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2, Timer4, Timer6 or Timer8 is the least significant word; Timer3, Timer5, Timer7 or Timer9 is the most significant word of the 32-bit timers.

> **Note:** For 32-bit operation, T3CON, T5CON, T7CON and T9CON control bits are ignored. Only T2CON, T4CON, T6CON and T8CON control bits are used for setup and control. Timer2, Timer4, Timer6 and Timer8 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3, Timer5, Ttimer7 and Timer9 interrupt flags.

To configure Timer2/3, Timer4/5, Timer6/7 or Timer8/9 for 32-bit operation:

1. Set the corresponding T32 control bit.
2. Select the prescaler ratio for Timer2, Timer4, Timer6 or Timer8 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
4. Load the timer period value. PR3, PR5, PR7 or PR9 contains the most significant word of the value, while PR2, PR4, PR6 or PR8 contains the least significant word.
5. If interrupts are required, set the interrupt enable bit, T3IE, T5IE, T7IE or T9IE. Use the priority bits, T3IP<2:0>, T5IP<2:0>, T7IP<2:0> or T9IP<2:0>, to set the interrupt priority. While Timer2, Timer4, Timer6 or Timer8 control the timer, the interrupt appears as a Timer3, Timer5, Timer7 or Timer9 interrupt.
6. Set the corresponding TON bit.

The timer value at any point is stored in the register pair, TMR3:TMR2, TMR5:TMR4, TMR7:TMR6 or TMR9:TMR8. TMR3, TMR5, TMR7 or TMR9 always contains the most significant word of the count, while TMR2, TMR4, TMR6 or TMR8 contains the least significant word.

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer.
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit.

A block diagram for a 32-bit timer pair (Timer4/5) example is shown in Figure 13-1 and a timer (Timer4) operating in 16-bit mode example is shown in Figure 13-2.

> **Note:** Only Timer2 and Timer3 can trigger a DMA data transfer.

---

**FIGURE 13-1:** **TIMER2/3 (32-BIT) BLOCK DIAGRAM[1]**



**Note 1:** The 32-bit timer control bit, T32, must be set for 32-bit timer/counter operation. All control bits are respective to the T2CON register.

**2:** The ADC event trigger is available only on Timer2/3.
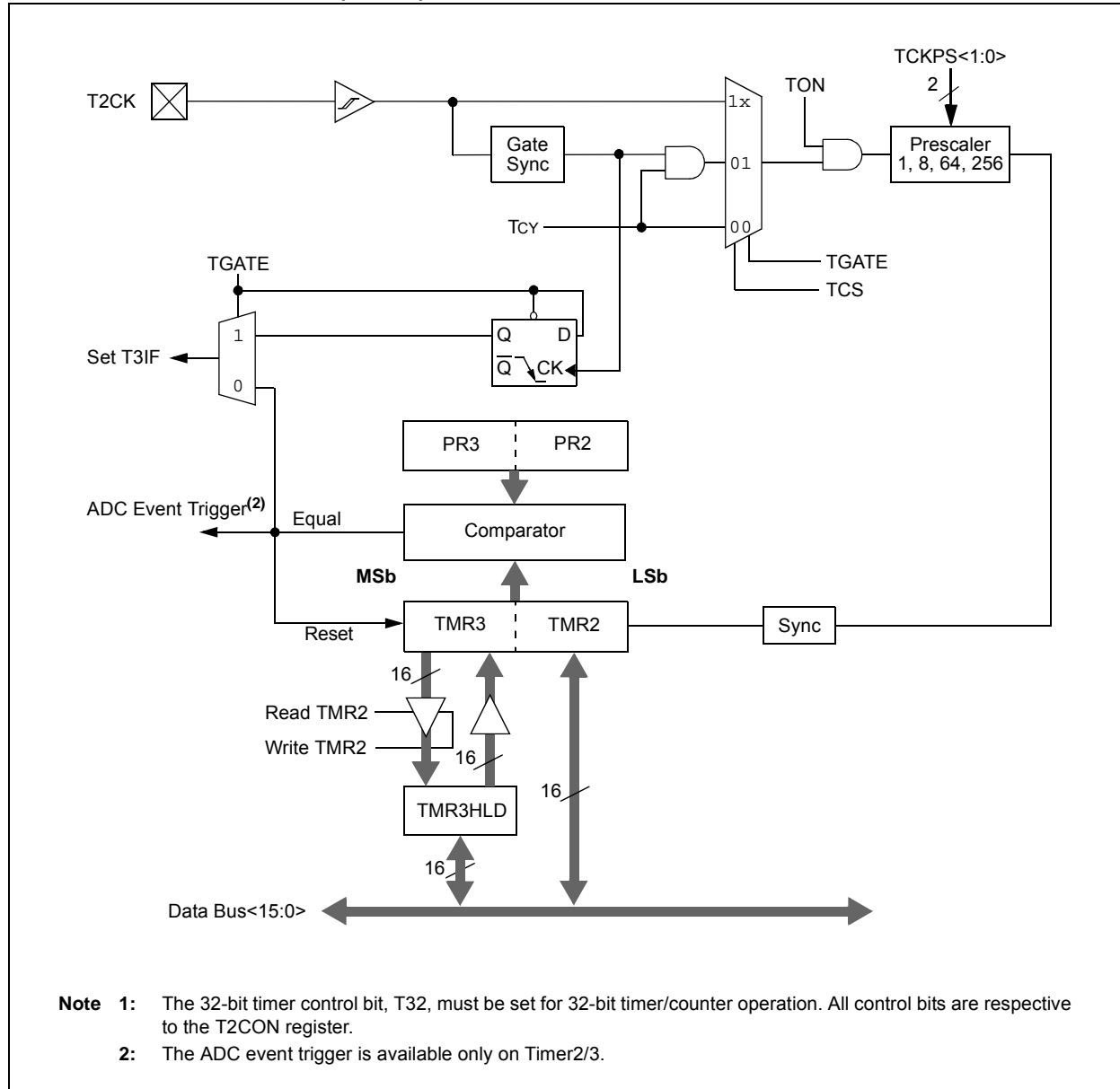
**REGISTER 16-3:** **SPIxCON2: SPIx CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| FRMEN | SPIFSD | FRMPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| — | — | — | — | — | — | FRMDLY | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15        **FRMEN:** Framed SPIx Support bit

                     1 = Framed SPIx support enabled ($\overline{\text{SS}}$x pin used as frame sync pulse input/output)
                     0 = Framed SPIx support disabled

bit 14        **SPIFSD:** Frame Sync Pulse Direction Control bit

                     1 = Frame sync pulse input (slave)
                     0 = Frame sync pulse output (master)

bit 13        **FRMPOL:** Frame Sync Pulse Polarity bit

                     1 = Frame sync pulse is active-high
                     0 = Frame sync pulse is active-low

bit 12-2      **Unimplemented:** Read as '0'

bit 1         **FRMDLY:** Frame Sync Pulse Edge Select bit

                     1 = Frame sync pulse coincides with first bit clock
                     0 = Frame sync pulse precedes first bit clock

bit 0         **Unimplemented:** Read as '0'

                     This bit must not be set to '1' by the user application.

**REGISTER 19-29: CiTRBnDLC: ECAN™ BUFFER n DATA LENGTH CONTROL (n = 0, 1, ..., 31)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID<5:0> | | | | | | RTR | RB1 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-----|-----|-----|-------|-------|-------|-------|-------|
| — | — | — | RB0 | DLC<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10     **EID<5:0>:** Extended Identifier bits

bit 9     **RTR:** Remote Transmission Request bit
1 = Message will request remote transmission
0 = Normal message

bit 8     **RB1:** Reserved Bit 1
User must set this bit to '0' per CAN protocol.

bit 7-5     **Unimplemented:** Read as '0'

bit 4     **RB0:** Reserved Bit 0
User must set this bit to '0' per CAN protocol.

bit 3-0     **DLC<3:0>:** Data Length Code bits

**REGISTER 19-30: CiTRBnDm: ECAN™ BUFFER n DATA FIELD BYTE m**
**(n = 0, 1, ..., 31; m = 0, 1, ..., 7)[1]**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TRBnDm<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0     **TRBnDm<7:0>:** Data Field Buffer 'n' Byte 'm' bits

**Note 1:** The Most Significant Byte contains byte (m + 1) of the buffer.

**REGISTER 21-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-----|-----|-------|-------|-------|-------|-------|
| CH0NB | — | — | CH0SB<4:0>[1] | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-----|-----|-------|-------|-------|-------|-------|
| CH0NA | — | — | CH0SA<4:0>[1] | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15      **CH0NB:** Channel 0 Negative Input Select for Sample B bit
         Same definition as bit 7.

bit 14-13      **Unimplemented:** Read as '0'

bit 12-8      **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample B bits[1]
         11111 = Channel 0 positive input is AN31
         11110 = Channel 0 positive input is AN30
         •
         •
         •
         00010 = Channel 0 positive input is AN2
         00001 = Channel 0 positive input is AN1
         00000 = Channel 0 positive input is AN0

bit 7      **CH0NA:** Channel 0 Negative Input Select for Sample A bit
         1 = Channel 0 negative input is AN1
         0 = Channel 0 negative input is V$_{REF-}$

bit 6-5      **Unimplemented:** Read as '0'

bit 4-0      **CH0SA<4:0>:** Channel 0 Positive Input Select for Sample A bits[1]
         11111 = Channel 0 positive input is AN31
         11110 = Channel 0 positive input is AN30
         •
         •
         •
         00010 = Channel 0 positive input is AN2
         00001 = Channel 0 positive input is AN1
         00000 = Channel 0 positive input is AN0

**Note 1:** ADC2 can only select AN0 through AN15 as positive input.
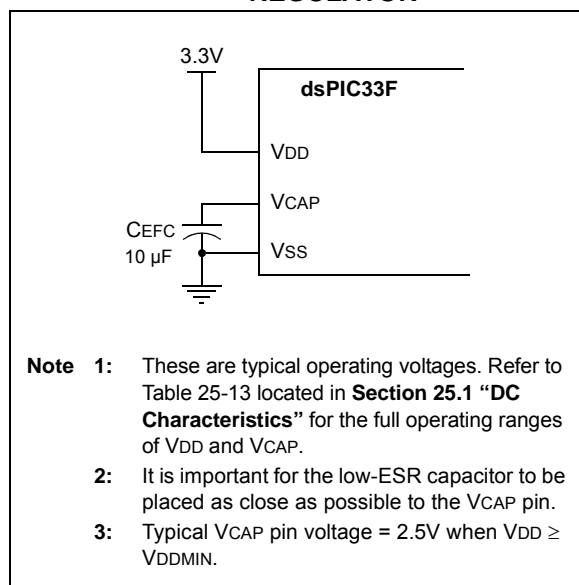
## 22.2 On-Chip Voltage Regulator

All of the dsPIC33FJXXXGPX06A/X08A/X10A devices power their core digital logic at a nominal 2.5V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJXXXGPX06A/X08A/X10A family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. The regulator requires that a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) be connected to the VCAP pin (Figure 22-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 25-13 of **Section 25.0 "Electrical Characteristics"**.

| Note: | It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin. |
|---|---|

On a POR, it takes approximately 20 μs for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

**FIGURE 22-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR[1,2,3]**



**Note 1:** These are typical operating voltages. Refer to Table 25-13 located in **Section 25.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

**2:** It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

**3:** Typical VCAP pin voltage = 2.5V when VDD ≥ VDDMIN.

## 22.3 BOR: Brown-out Reset

The BOR (Brown-out Reset) module is based on an internal voltage reference circuit that monitors the regulated voltage VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (i.e., missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR will generate a Reset pulse which will reset the device. The BOR will select the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>). Furthermore, if an oscillator mode is selected, the BOR will activate the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, then the clock will be held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) will be applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) will be set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and will reset the device should VDD fall below the BOR threshold voltage.

**TABLE 25-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ $T_A$ ≤ +85°C for Industrial                                        -40°C ≤ $T_A$ ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ[1] | Max | Units | Conditions |
| **Operating Voltage** | | | | | | | |
| DC10 | **Supply Voltage** | | | | | | |
| | $V_{DD}$ | — | 3.0 | — | 3.6 | V | — |
| DC12 | $V_{DR}$ | **RAM Data Retention Voltage[2]** | 1.8 | — | — | V | — |
| DC16 | $V_{POR}$ | **$V_{DD}$ Start Voltage** to ensure internal Power-on Reset signal | — | — | $V_{SS}$ | V | — |
| DC17 | $S_{VDD}$ | **$V_{DD}$ Rise Rate** to ensure internal Power-on Reset signal | 0.03 | — | — | V/ms | 0-3.0V in 0.1s |

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.
    **2:** This is the limit to which $V_{DD}$ can be lowered without losing RAM data.

**TABLE 25-8: DC CHARACTERISTICS: DOZE CURRENT (I_DOZE)**

| DC CHARACTERISTICS | | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial                                        -40°C ≤ TA ≤ +125°C for Extended | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Typical[2] | Max | Doze Ratio | Units | Conditions | | |
| **Doze Current (I_DOZE)[1]** | | | | | | | |
| DC73a | 11 | 35 | 1:2 | mA | -40°C | 3.3V | 40 MIPS |
| DC73f | 11 | 30 | 1:64 | mA | | | |
| DC73g | 11 | 30 | 1:128 | mA | | | |
| DC70a | 42 | 50 | 1:2 | mA | +25°C | 3.3V | 40 MIPS |
| DC70f | 26 | 30 | 1:64 | mA | | | |
| DC70g | 25 | 30 | 1:128 | mA | | | |
| DC71a | 41 | 50 | 1:2 | mA | +85°C | 3.3V | 40 MIPS |
| DC71f | 25 | 30 | 1:64 | mA | | | |
| DC71g | 24 | 30 | 1:128 | mA | | | |
| DC72a | 42 | 50 | 1:2 | mA | +125°C | 3.3V | 40 MIPS |
| DC72f | 26 | 30 | 1:64 | mA | | | |
| DC72g | 25 | 30 | 1:128 | mA | | | |

**Note 1:** I_DOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_DOZE measurements are as follows:
  • Oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail with overshoot/undershoot < 250 mV
  • CLKO is configured as an I/O input pin in the Configuration word
  • All I/O pins are configured as inputs and pulled to VSS
  • MCLR = VDD, WDT and FSCM are disabled
  • CPU, SRAM, program memory and data memory are operational
  • No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
  • CPU executing while(1) statement
  • JTAG is disabled

**2:** Data in the "Typ" column is at 3.3V, +25ºC unless otherwise stated.

**TABLE 25-28:    SPIx MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial                                          -40°C ≤ TA ≤ +125°C for Extended | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 25-29 | — | — | 0,1 | 0,1 | 0,1 |
| 10 MHz | — | Table 25-30 | — | 1 | 0,1 | 1 |
| 10 MHz | — | Table 25-31 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 25-32 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 25-33 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 25-34 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 25-35 | 0 | 0 | 0 |

**FIGURE 25-9:    SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS**



Note: Refer to Figure 25-1 for load conditions.
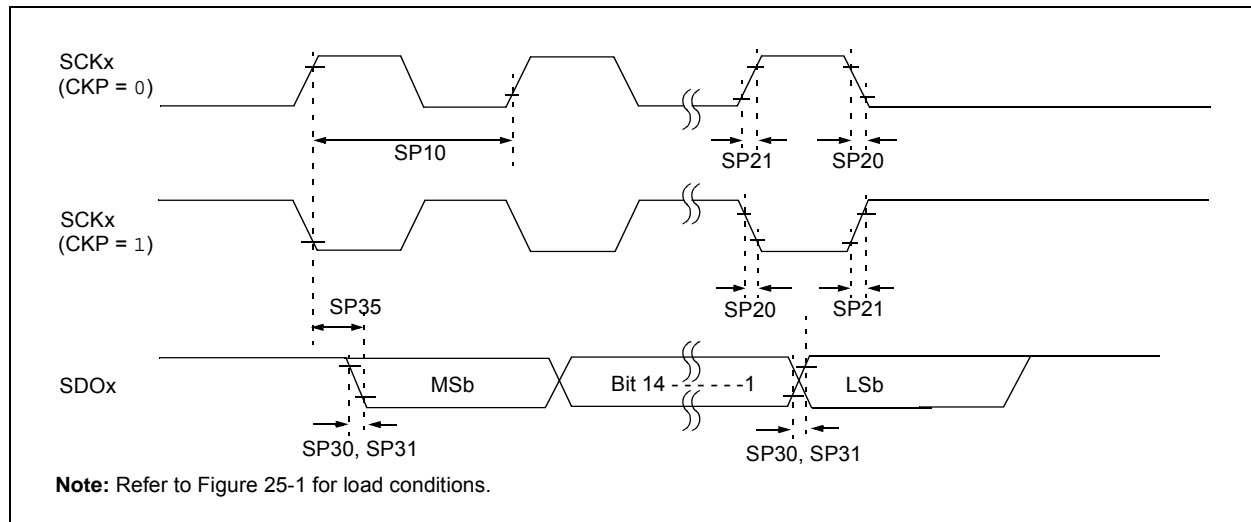
**TABLE 25-45: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature  -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min. | Typ[1] | Max. | Units | Conditions |
| **Clock Parameters** | | | | | | | |
| AD50b | $T_{AD}$ | ADC Clock Period | 76 | — | — | ns | — |
| AD51b | $T_{RC}$ | ADC Internal RC Oscillator Period | — | 250 | — | ns | — |
| **Conversion Rate** | | | | | | | |
| AD55b | $T_{CONV}$ | Conversion Time | — | 12 $T_{AD}$ | — | — | — |
| AD56b | $F_{CNV}$ | Throughput Rate | — | — | 1.1 | Msps | — |
| AD57b | $T_{SAMP}$ | Sample Time | 2 $T_{AD}$ | — | — | — | — |
| **Timing Parameters** | | | | | | | |
| AD60b | $T_{PCS}$ | Conversion Start from Sample Trigger[2] | 2.0 $T_{AD}$ | — | 3.0 $T_{AD}$ | — | Auto-Convert Trigger (SSRC<2:0> = 111) not selected |
| AD61b | $T_{PSS}$ | Sample Start from Setting Sample (SAMP) bit[2] | 2.0 $T_{AD}$ | — | 3.0 $T_{AD}$ | — | — |
| AD62b | $T_{CSS}$ | Conversion Completion to Sample Start (ASAM = 1)[2] | — | 0.5 $T_{AD}$ | — | — | — |
| AD63b | $T_{DPU}$ | Time to Stabilize Analog Stage from ADC Off to ADC On[2,3] | — | — | 20 | µs | — |

**Note  1:**  These parameters are characterized but not tested in manufacturing.

**2:**  Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

**3:**  $T_{DPU}$ is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.
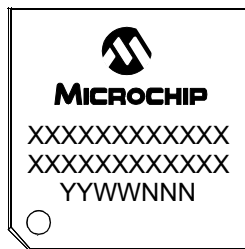
**TABLE 25-46: DMA READ/WRITE TIMING REQUIREMENTS**

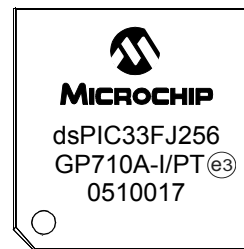| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature  -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min. | Typ | Max. | Units | Conditions |
| DM1a | DMA Read/Write Cycle Time | — | — | 2 $T_{CY}$ | ns | This characteristic applies to dsPIC33FJ256GPX06A/X08A/X10A devices only. |
| DM1b | DMA Read/Write Cycle Time | — | — | 1 $T_{CY}$ | ns | This characteristic applies to all devices with the exception of the dsPIC33FJ256GPX06A/X08A/X10A. |

## 28.1 Package Marking Information (Continued)

100-Lead TQFP (12x12x1 mm)
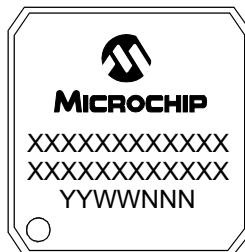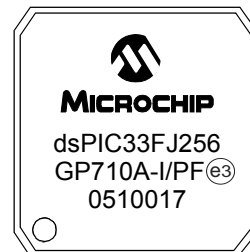
Example

XXXXXXXXXXXX
XXXXXXXXXXXX
YYWWNNN

dsPIC33FJ256
GP710A-I/PT (e3)
0510017

100-Lead TQFP (14x14x1mm)

Example

XXXXXXXXXXXX
XXXXXXXXXXXX
YYWWNNN

dsPIC33FJ256
GP710A-I/PF (e3)
0510017

| Legend: | XX...X | Customer-specific information |
| --- | --- | --- |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.