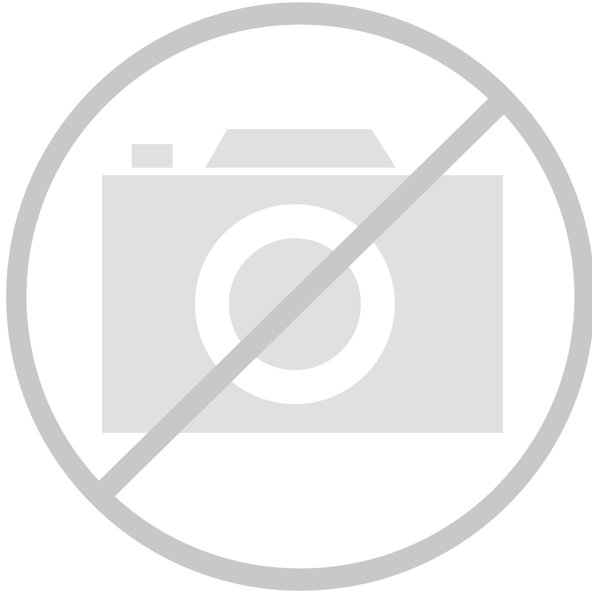

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	255-BBGA Exposed Pad
Supplier Device Package	255-PBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx745bvzfu300le

- Fixed Point Units (FXUs) that share 32 GPRs for Integer Operands
  - – Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
  - – Fixed Point Unit 2 (FXU2)-shift, rotate, arithmetic, logical
  - – Single-cycle arithmetic, shifts, rotates, logical
  - – Multiply and divide support (multi-cycle)
  - – Early out multiply
- Floating-point Unit and a 32-entry FPR File
  - – Support for IEEE-754 standard single and double precision floating point arithmetic
  - – Hardware support for divide
  - – Hardware support for denormalized numbers
  - – Single-entry reservation station
  - – Supports non-IEEE mode for time-critical operations
- System Unit
  - – Executes CR logical instructions and miscellaneous system instructions
  - – Special register transfer instructions
- Load/Store Unit
  - – One cycle load or store cache access (byte, half-word, word, double-word)
  - – Effective address generation
  - – Hits under misses (one outstanding miss)
  - – Single-cycle unaligned access within double word boundary
  - – Alignment, zero padding, sign extend for integer register file
  - – Floating point internal format conversion (alignment, normalization)
  - – Sequencing for load/store multiples and string operations
  - – Store gathering
  - – Cache and TLB instructions
  - – Big and Little-endian byte addressing supported
  - – Misaligned Little-endian supported
  - – Level 1 Cache structure
  - – 32K, 32 bytes line, 8-way set associative instruction cache (iL1)
  - – 32K, 32 bytes line, 8-way set associative data cache (dL1)
  - – Cache locking for both instruction and data caches, selectable by group of ways
  - – Single-cycle cache access
  - – Pseudo least-recently used (PLRU) replacement
  - – Copy-back or Write Through data cache (on a page per page basis)
  - – Supports all PowerPC memory coherency modes
  - – Non-Blocking instruction and data cache (one outstanding miss under hits)
  - – No snooping of instruction cache
- Level 2 (L2) Cache Interface (not implemented on PC745)
  - – Internal L2 cache controller and tags; external data SRAMs
  - – 256K, 512K, and 1-Mbyte 2-way set associative L2 cache support

2.1 Pinout Listings

Table 2-1 provides the pinout listing for the PC745, 255 PBGA package.

Table 2-1. Pinout Listing for the PC745, 255 PBGA and HiTCE CBGA Packages

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	–	–
AACK	L2	Low	Input	–	–
ABB	K4	Low	I/O	–	–
AP[0-3]	C1, B4, B3, B2	High	I/O	–	–
ARTRY	J4	Low	I/O	–	–
AVDD	A10	–	–	2V	2V
BG	L1	Low	Input	–	–
BR	B6	Low	Output	–	–
BVSEL[3][4][5]	B1	High	Input	GND	3.3V
CI	E1	Low	Output	–	–
CKSTP_IN	D8	Low	Input	–	–
CKSTP_OUT	A6	Low	Output	–	–
CLK_OUT	D7	–	Output	–	–
DBB	J14	Low	I/O	–	–
DBG	N1	Low	Input	–	–
DBDIS	H15	Low	Input	–	–
DBWO	G4	Low	Input	–	–
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	–	–
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	–	–
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	–	–
DRTRY	G16	Low	Input	–	–
GBL	F1	Low	I/O	–	–
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12				
$\overline{\text{HRESET}}$	A7	Low	Input	–	–
INT	B15	Low	Input	–	–
L1_TSTCLK[2]	D11	High	Input	–	–
L2_TSTCLK[2]	D12	High	Input	–	–
LSSD_MODE[2]	B10	Low	Input	–	–

Table 2-1. Pinout Listing for the PC745, 255 PBGA and HiTCE CBGA Packages (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
MCP	C13	Low	Input	–	–
NC (No-Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	–	–	–	–
OVDD	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	–	–	1.8V/2.0V	3.3V
PLL_CFG[0-3]	A8, B9, A9, D9	High	Input	–	–
$\overline{\text{QACK}}$	D3	Low	Input	–	–
QREQ	J3	Low	Output	–	–
RSRV	D1	Low	Output	–	–
SMI	A16	Low	Input	–	–
SRESET	B14	Low	Input	–	–
SYSCLK	C9	–	Input	–	–
TA	H14	Low	Input	–	–
TBEN	C2	High	Input	–	–
TBST	A14	Low	I/O	–	–
TCK	C11	High	Input	–	–
TDI[5]	A11	High	Input	–	–
TDO	A12	High	Output	–	–
TEA	H13	Low	Input	–	–
TLBISYNC	C4	Low	Input	–	–
TMS[5]	B11	High	Input	–	–
$\overline{\text{TRST}}$[5]	C10	Low	Input	–	–
TS	J13	Low	I/O	–	–
TSIZ[0-2]	A13, D10, B12	High	Output	–	–
TT[0-4]	B13, A15, B16, C14, C15	High	I/O	–	–
WT	D2	Low	Output	–	–
V_{DD} 2	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	–	–	2V	2V
VOLTDET[6]	F3	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals and V_{DD} supplies power to the processor core and the PLL (after filtering to become AVDD). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 5-1 on page 15 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see "Absolute Maximum Ratings[1]" on page 14.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. Uses one of 15 existing no-connects in PC745's 255-BGA package.
5. Internal pull up on die.
6. Internally tied to GND in the PC745 255-BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
L2AVDD	L13	–	–	2V	2V
L2CE (active low)	P17	Low	Output	–	–
L2CLKOUTA	N15	–	Output	–	–
L2CLKOUTB	L16	–	Output	–	–
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	–	–
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	–	–
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	–	–	1.8V/2V	3.3V
L2SYNC_IN	L14	–	Input	–	–
L2SYNC_OUT	M14	–	Output	–	–
L2_TSTCLK[2]	F7	High	Input	–	–
L2VSEL[1][3][5][6]	A19	High	Input	GND	3.3V
L2WE (active low)	N16	Low	Output	–	–
L2ZZ	G17	High	Output	–	–
LSSD_MODE (active low)[2]	F9	Low	Input	–	–
MCP (active low)	B11	Low	Input	–	–
NC (No-Connect)	B3, B4, B5, W19, K9, K11[4], K19[4]	–	–	–	–
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	–	–	1.8V/2V	3.3V
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input	–	–
QACK (active low)	B2	Low	Input	–	–
QREQ (active low)	J3	Low	Output	–	–
RSRV (active low)	D3	Low	Output	–	–
SMI (active low)	A12	Low	Input	–	–
SRESET (active low)	E10	Low	Input	–	–
SYSCLK	H9	–	Input	–	–
TA (active low)	F1	Low	Input	–	–
TBEN	A2	High	Input	–	–
TBST (active low)	A11	Low	I/O	–	–
TCK	B10	High	Input	–	–
TDI[6]	B7	High	Input	–	–
TDO	D9	High	Output	–	–

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
$\overline{TEA}$	J1	Low	Input	–	–
$\overline{TLBISYNC}$	A3	Low	Input	–	–
TMS[6]	C8	High	Input	–	–
$\overline{TRST}$[6]	A10	Low	Input	–	–
$\overline{TS}$	K7	Low	I/O	–	–
TSIZ[0-2]	A9, B9, C9	High	Output	–	–
TT[0-4]	C10, D11, B12, C12, F11	High	I/O	–	–
$\overline{WT}$	C3	Low	Output	–	–
VDD	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	–	–	2V	2V
VOLTDET[7]	K13	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0-16], L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 5-1 on page 15 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see "Recommended Operating Conditions[1]" on page 16.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of 9 existing no-connects in PC750's 360-BGA package.
6. Internal pull up on die.
7. Internally tied to $L2OV_{DD}$ in the PC755 360-BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.
8. This is different from the PC745 255-BGA package.

4. Detailed Specifications

This specification describes the specific requirements for the microprocessor PC755, in compliance with Atmel Grenoble standard screening.

5. Applicable Documents

1) MIL-STD-883: Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

Depending on the package, the terminal connections is shown in Table 2-1 on page 8, Table 2-2 on page 10 and Figure 3-1 on page 13.

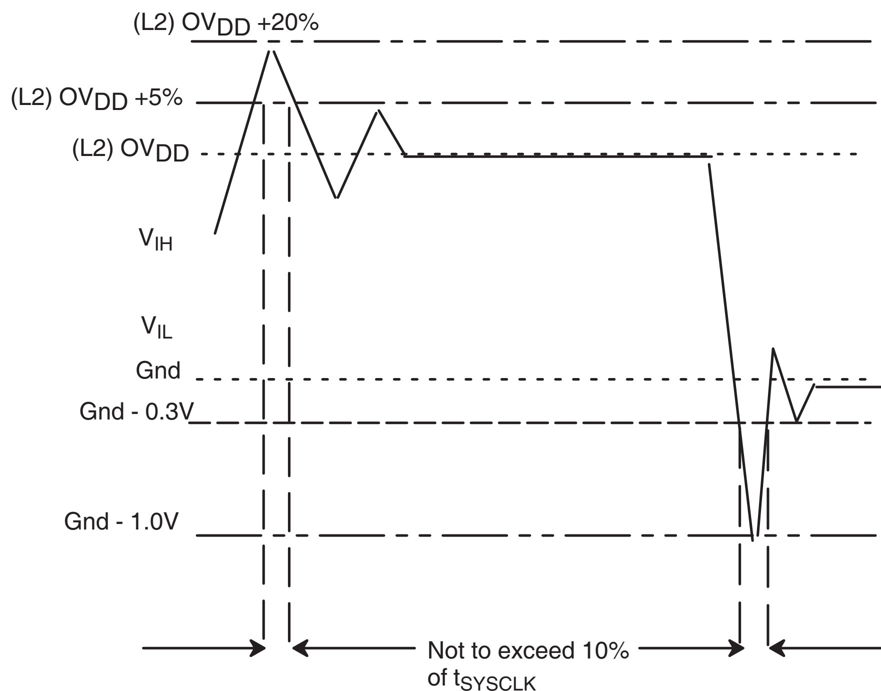
5.1.2 Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage[4]		V_{DD}	-0.3 to 2.5	V
PLL supply voltage[4]		AV_{DD}	-0.3 to 2.5	V
L2 DLL supply voltage[4]		$L2AV_{DD}$	-0.3 to 2.5	V
Processor bus supply voltage[3]		OV_{DD}	-0.3 to 3.6	V
L2 bus supply voltage[3]		$L2OV_{DD}$	-0.3 to 3.6	V
Input voltage	Processor bus[2][5]	V_{IN}	-0.3 to OV_{DD} + 0.3V	V
	L2 Bus[2][5]	V_{IN}	-0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{IN}	-0.3 to 3.6	V
Storage temperature range		T_{STG}	-55/+150	°C

Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions[1]" on page 16. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3V for up to 20 ms, or by 2.5V for up to 40 ms. Excursions beyond 3.3V or 40 ms are not supported.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0V for up to 20 ms, or by 0.7V for up to 40 ms. Excursions beyond 1.0V or 40 ms are not supported.
5. This is a DC specifications only. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5-1 on page 15.

Figure 5-1 shows the allowable undershoot and overshoot voltage on the PC755 and PC745.

Figure 5-1. Overshoot/Undershoot Voltage



The PC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC755 core voltage must always be provided at nominal 2.0V (see "Recommended Operating Conditions[1]" on page 16 for actual recommended core voltage). Voltage to the L2 I/Os and Processor Interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 5-1. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 5-1 describes the input threshold voltage setting.

Table 5-1. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5V/3.3V	1	2.5V/3.3V

Notes: 1. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.

2. The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, contact your local Atmel sales office.

6. Thermal Characteristics

6.1 Package Characteristics

Table 6-1 provides the package thermal characteristics for the PC755.

Table 6-1. Package Thermal Characteristics

Characteristic	Symbol	Value			Unit
		PC755 CBGA	PC755 PBGA	PC745 PBGA	
Junction-to-ambient thermal resistance, natural convection[()(2)]	$R\theta_{JA}$	24	31	34	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board[()(3)]	$R\theta_{JMA}$	17	25	26	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board[()(3)]	$R\theta_{JMA}$	18	25	27	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board[()(3)]	$R\theta_{JMA}$	14	21	22	°C/W
Junction-to-board thermal resistance[(4)]	$R\theta_{JB}$	8	17	17	°C/W
Junction-to-case thermal resistance[(5)]	$R\theta_{JC}$	< 0.1	< 0.1	< 0.1	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R\theta_{JC}$ for the part is less than 0.1°C/W.

Note: Refer to Section 6.1.3 "Thermal Management Information" on page 19 for more details about thermal management.

6.1.1 Package Thermal Characteristics for HiTCE

Table 6-2 provides the package thermal characteristics for the PC755, HiTCE.

Table 6-2. Package Thermal Characteristics for HiTCE Package

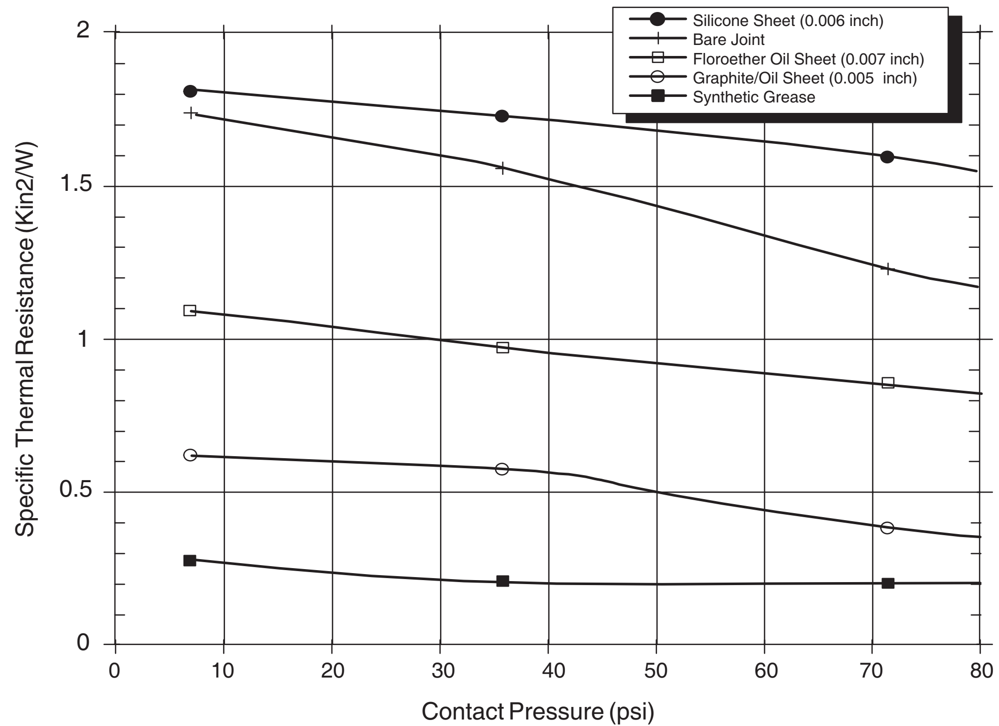
Characteristic	Symbol	Value		Unit
		PC755 HiTCE	PC745 HiTCE	
Junction-to-bottom of balls[(1)]	$R\theta_{J}$	6.8	6.5	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R\theta_{JMA}$	20.7[(1)(2)]	20.9[(1)(4)]	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.0	10.2[(3)]	°C/W

Notes:
1. Simulation, no convection air flow
2. Per JEDEC JESD51-6 with the board horizontal
3. Per JEDEC JESD51-8
4. Per JEDEC JESD51-2 with the board horizontal

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6.1.4 Adhesives and Thermal Interface Materials

Figure 6-3. Thermal Performance of Select Thermal Interface Material



A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-3 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 6-2 on page 19). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

6.1.5 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

Where:

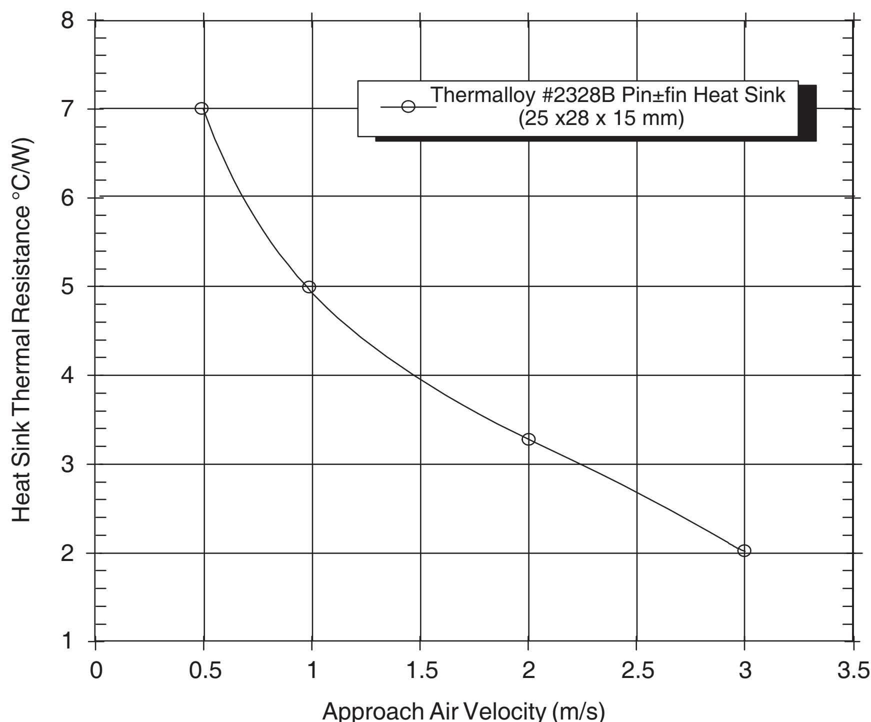
T_J is the die-junction temperature
T_A is the inlet cabinet ambient temperature
T_R is the air temperature rise within the computer cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the adhesive or interface material thermal resistance
θ_{SA} is the heat sink base-to-ambient thermal resistance
P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained less than the value specified in "Recommended Operating Conditions(1)" on page 16. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a $T_{R\ of\ 5}$°C, a CBGA package θ_{JC} = 0.03, and a power consumption (P_D) of 5.0 watts, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 6-4.

Figure 6-4. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity



Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

T_J = 30°C + 5°C+ (0.03°C/W +1.0°C/W + 7°C/W) × 5.0 W

resulting in a die-junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature — airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

7. Power consideration

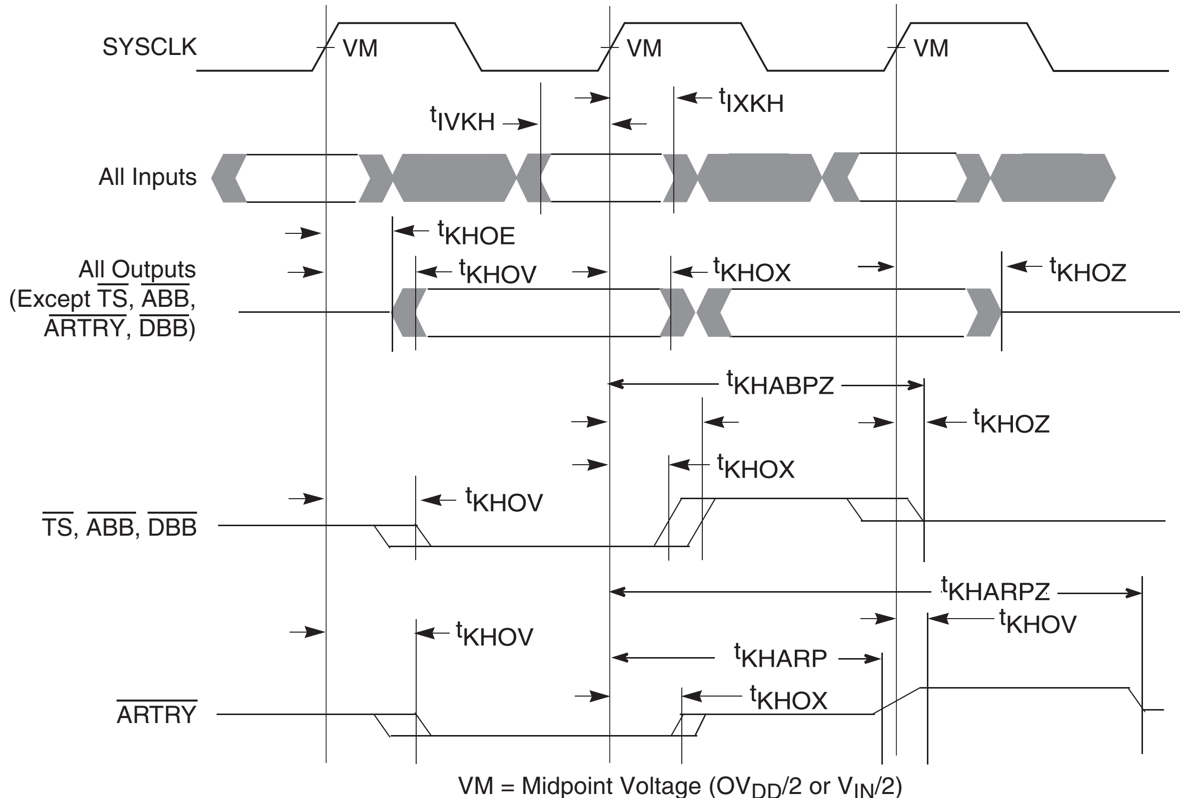
7.1 Power management

The PC755 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows:

- Full-power: This is the default power state of the PC755. The PC755 is fully powered and the internal functional units operate at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- Doze: All the functional units of the PC755 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the PC755 into the full-power state. The PC755 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC755 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input (MCP). A return to full-power state from a nap state takes only a few processor clock cycles.

Figure 8-4 provides the input/output timing diagram for the PC755.

Figure 8-4. Input/Output Timing Diagram



8.2.1.2 *L2 Clock AC Specifications*

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 8-5 on page 29 for example core and L2 frequencies at various divisors. Table 8-5 provides the potential range of L2CLK output AC timing specifications as defined in Figure 8-5 on page 30.

The minimum L2CLK frequency of Table 8-5 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 8-5 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC755 will be a function of the AC timings of the PC755, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 8-5. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

8.2.1.3 L2 Bus Input AC Specifications

Table 8-6 provides the L2 bus interface AC timing specifications for the PC755 as defined in Figure 8-6 on page 32 and Figure 8-7 on page 32 for the loading conditions described in Figure 8-8 on page 32.

Table 8-6. L2 Bus Interface AC Timing Specifications at Recommended Operating Conditions

Parameter	Symbol	All Speed Grades		Unit
		Min	Max	
L2SYNC_IN rise and Fall Time[(1)]	t_{L2CR} & t_{L2CF}	–	1.0	ns
Setup Times: Data and Parity[(2)]	t_{DVL2CH}	1.2	-	ns
Input Hold Times: Data and Parity[(2)]	t_{DXL2CH}	0	-	ns
Valid Times: [(3)(4)] All Outputs when L2CR[14-15] = 00 All Outputs when L2CR[14-15] = 01 All Outputs when L2CR[14-15] = 10 All Outputs when L2CR[14-15] = 11	t_{L2CHOV}	 - - - -	 3.1 3.2 3.3 3.7	ns
Output Hold Times: [(3)] All Outputs when L2CR[14-15] = 00 All Outputs when L2CR[14-15] = 01 All Outputs when L2CR[14-15] = 10 All Outputs when L2CR[14-15] = 11	t_{L2CHOX}	 0.5 0.7 0.9 1.1	 - - - -	ns
L2SYNC_IN to High Impedance:[(3)(5)] All Outputs when L2CR[14-15] = 00 All Outputs when L2CR[14-15] = 01 All Outputs when L2CR[14-15] = 10 All Outputs when L2CR[14-15] = 11	t_{L2CHOZ}	 - - - -	 2.4 2.6 2.8 3.0	ns

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 6-3 on page 20). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 8-1 on page 25).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14-15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14-15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev 2.8 (Rev E) were limited in performance.and did not conform to this specification. Contact your local Atmel sales office for more information.

8.2.2.1 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{TRST}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{TRST}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{TRST}$ to $\overline{HRESET}$ is not practical.

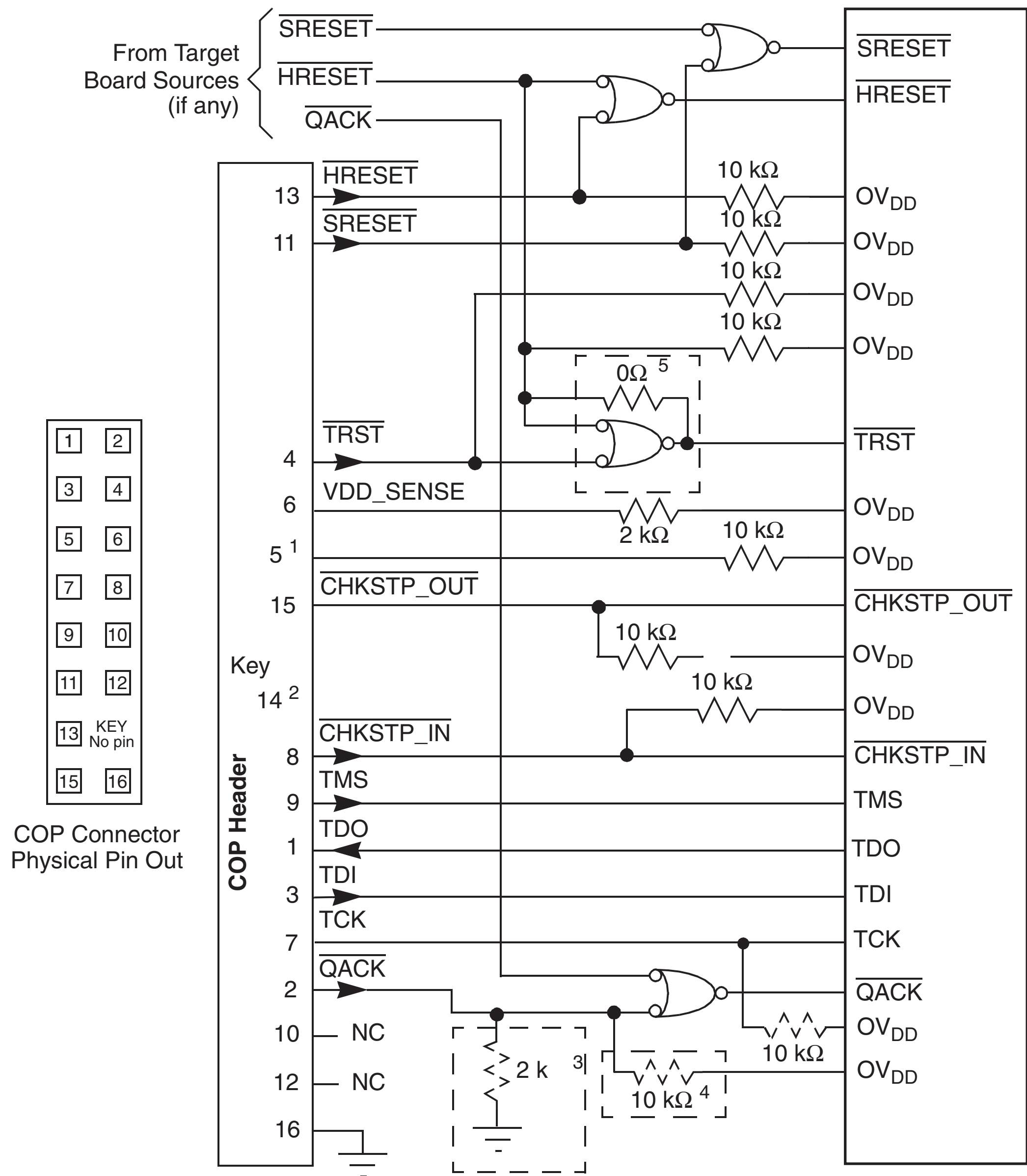
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{HRESET}$ or $\overline{TRST}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must bemerged into these signals with logic.

The arrangement shown in Figure 8-14 on page 36 allows the COP port to independently assert $\overline{HRESET}$ or $\overline{TRST}$, while ensuring that the target can drive $\overline{HRESET}$ as well. If the JTAG interface and COP header will not be used, $\overline{TRST}$ should be tied to $\overline{HRESET}$ through a 0Ω isolation resistor so that it is asserted when the systemreset signal ($\overline{HRESET}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 8-14, if this is not possible, the isolation resistor will allow future access to $\overline{TRST}$ in the case where a JTAG interfacemay need to be wired onto the system in debug situations.

The COP header shown in Figure 8-14 adds many benefits — breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface — and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

Figure 8-14. JTAG Interface Connection



Notes:
1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the PC755. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive QACK.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert QACK.
5. If the JTAG interface is implemented, connect HRESET from the target source to TRST from the COP header though an AND gate to TRST of the part. If the JTAG interface is not implemented, connect HRESET from the target source to TRST of the part through a 0Ω isolation resistor.

The COP header shown in Figure 8-15 on page 37 adds many benefits—breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

9. Preparation for Delivery

9.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

9.2 Certificate of Compliance

Atmel offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-PRF-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

9.3 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

1. Devices should be handled on benches with conductive and grounded surfaces
2. Ground test equipment, tools and operator
3. Do not handle devices by the leads
4. Store devices in conductive foam or carriers
5. Avoid use of plastic, rubber, or silk in MOS areas
6. Maintain relative humidity above 50 percent if practical
7. For CI-CGA packages, use specific tray to take care of the highest height of the package compared with the normal CBGA

9.4 Clock Relationship Choices

The PC755's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755 is shown in Figure 10-2 on page 41 for example frequencies.

Table 9-1. PC755 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0100	2x	2x	-	-	-	-	-	200 (400)
1000	3x	2x	-	-	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	-	-	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	-	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	-	225 (450)	300 (600)	338 (675)	360 (720)	-
1011	5x	2x	-	250 (500)	333 (666)	375 (750)	400 (800)	-
1001	5.5x	2x	-	275 (550)	366 5733°	-	-	-
1101	6x	2x	200 (400)	300 (600)	400 (800)	-	-	-
0101	6.5x	2x	216 (433)	325 (650)	-	-	-	-
0010	7x	2x	233 (466)	350 (700)	-	-	-	-
0001	7.5x	2x	250 (500)	375 (750)	-	-	-	-
1100	8x	2x	266 (533)	400 (800)	-	-	-	-
0110	10x	2x	333 (666)	-	-	-	-	-
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755; see "Clock AC Specifications" on page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the PC755 regardless of the SYSCLK input.

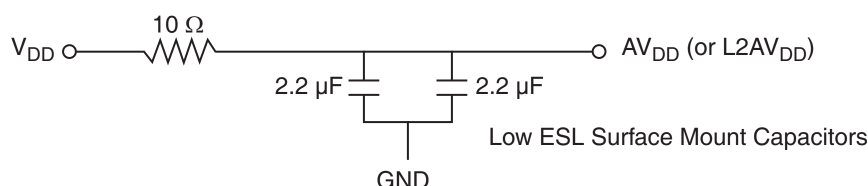
10. System Design Information

10.1 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the PC755 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 10-2 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route but is proportionately less critical.

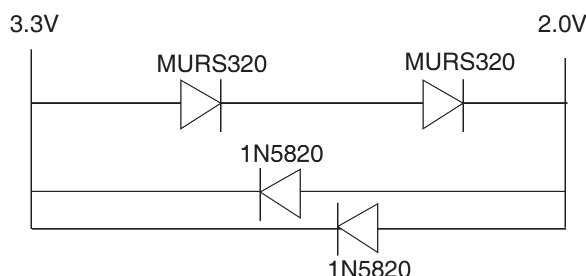
Figure 10-1. PLL Power Supply Filter Circuit



10.2 Power Supply Voltage Sequencing

The notes in Figure 10-3 on page 43 contain cautions about the sequencing of the external bus voltages and core voltage of the PC755 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the ESD (Electrostatic Discharge) protection diodes will be forward biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit of Figure 10-3 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 10-3 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

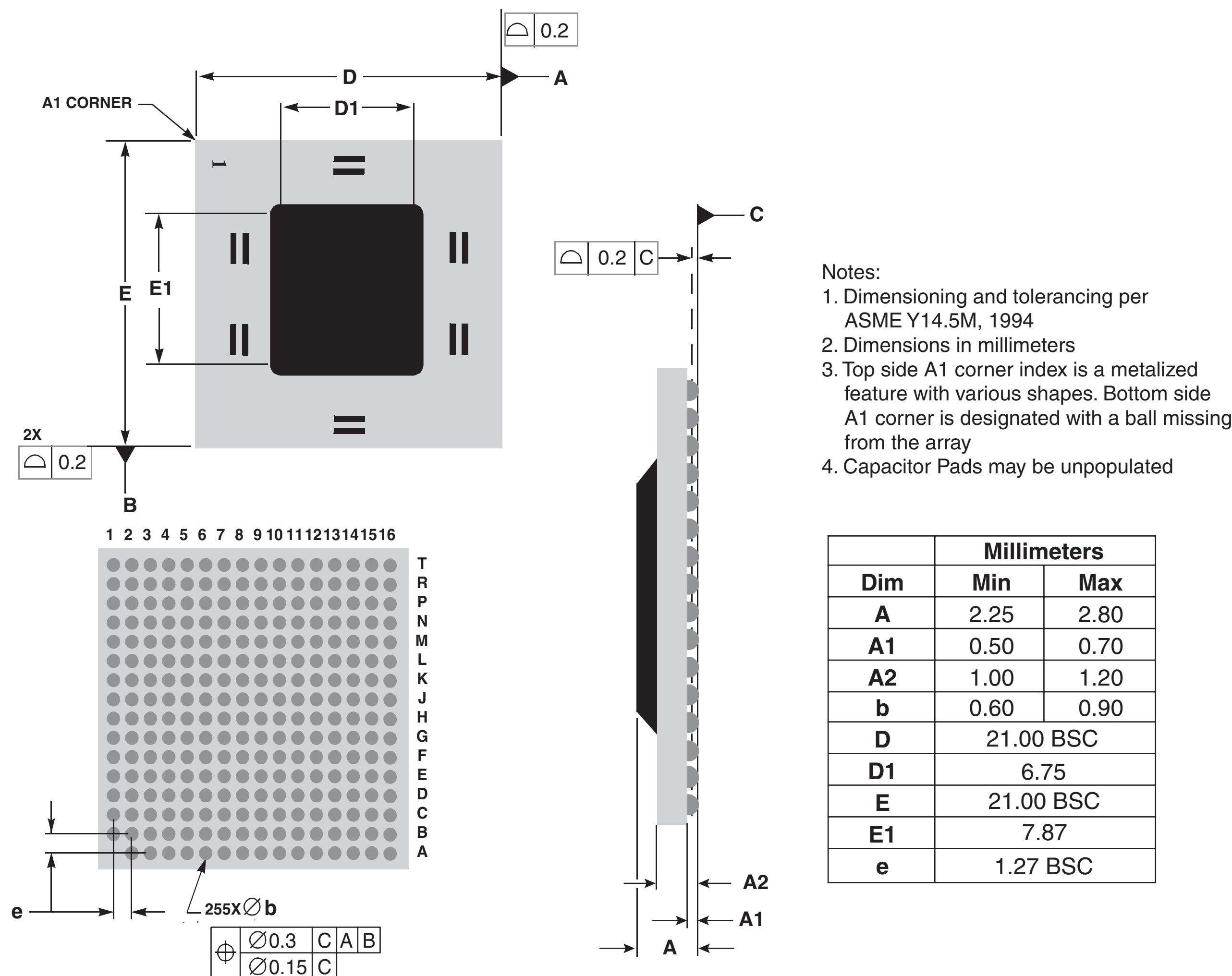
Figure 10-2. Example Voltage Sequencing Circuit



11.1.2 Mechanical Dimensions of the PC745 PBGA Package

Figure 11-2 provides the mechanical dimensions and bottom surface nomenclature of the PC745, 255 PBGA package.

Figure 11-2. Mechanical Dimensions and Bottom Surface Nomenclature of the PC745 PBGA



	Millimeters	
Dim	**Min**	**Max**
A	2.25	2.80
A1	0.50	0.70
A2	1.00	1.20
b	0.60	0.90
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2 Package Parameter for the PC755

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead plastic ball grid array (PBGA).

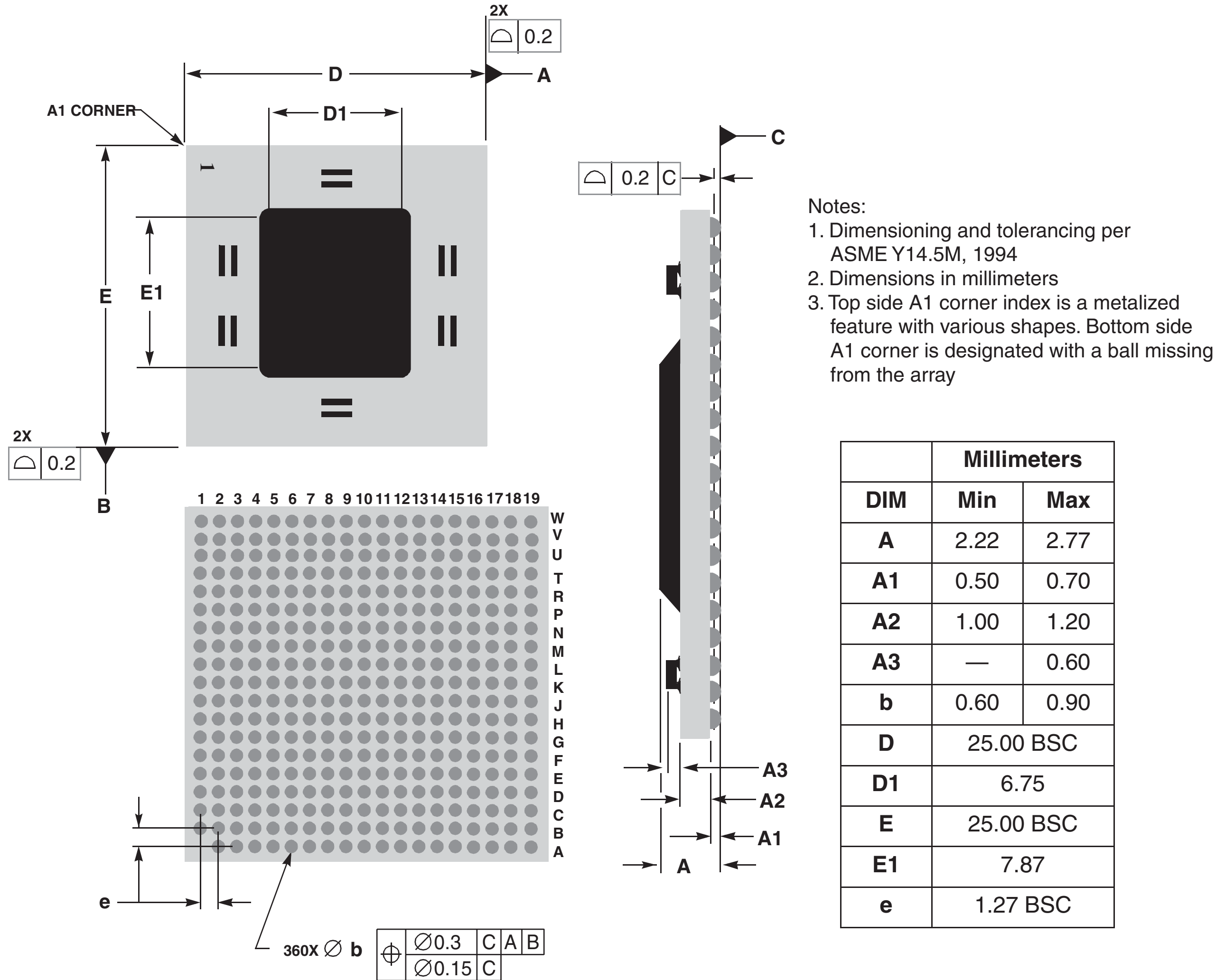
Table 11-2. Package Parameters

Parameter	HiTCE-CBGA	PBGA
Package Outline	25 mm × 25 mm	25 mm × 25 mm
Interconnects	360 (19 x 19 ball array – 1)	360 (19 x 19 ball array – 1
Pitch	1.27 mm (50 mil)	1.27 mm (50 mil)
Minimum module height	2,65 mm	2.22 mm
Maximum module height	3,2 mm	2.77 mm
Ball diameter	0,89 mm (35 mil)	0.75 mm (29.5 mil)

11.2.1 Mechanical Dimensions of the PC755 PBGA

Figure 11-3 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 PBGA package.

Figure 11-3. Mechanical Dimensions and Bottom Surface Nomenclature of the PC755 PBGA



	Millimeters	
DIM	Min	Max
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	