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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	255-BBGA Exposed Pad
Supplier Device Package	255-PBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx745bvzfu350le

1.2 General Parameters

The following list provides a summary of the general parameters of the PC755:

Technology	0.22 µm CMOS, five-layer metal, 1 layer poly
Die size	6.61 mm x 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static Packages
PC745	Surface mount 255 Plastic Ball Grid Array (PBGA) Surface mount 255 Ceramic Ball Grid Array (Hi-TCE)
PC755	Surface mount 360 Plastic Ball Grid Array (PBGA) Surface mount 360 Ceramic Ball Grid Array (CI-CGA, CBGA, HiTCE)
Core power supply	2V ± 100 mV DC (nominal; some parts support core voltages down to 1.8V; see "Recommended Operating Conditions(1)" on page 16
I/O power supply	2.5V ± 100 mV DC or 3.3V ± 165 mV DC (input thresholds are configuration pin selectable)

1.3 Features

This section summarizes features of the PC755's implementation of the PowerPC architecture. Major features of the PC755 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry Branch History Table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 6 entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes

- Fixed Point Units (FXUs) that share 32 GPRs for Integer Operands
  - Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)-shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point Unit and a 32-entry FPR File
  - Support for IEEE-754 standard single and double precision floating point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/Store Unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and Little-endian byte addressing supported
  - Misaligned Little-endian supported
  - Level 1 Cache structure
  - 32K, 32 bytes line, 8-way set associative instruction cache (iL1)
  - 32K, 32 bytes line, 8-way set associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently used (PLRU) replacement
  - Copy-back or Write Through data cache (on a page per page basis)
  - Supports all PowerPC memory coherency modes
  - Non-Blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) Cache Interface (not implemented on PC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1-Mbyte 2-way set associative L2 cache support

  - Copyback or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode.
  - 64 bytes (256K/512K) or 128 bytes (1M) sectored line size
  - Supports flow through (register-buffer) synchronous burst SRAMs, pipelined (register-register) synchronous burst SRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late-write synchronous burst SRAMs
  - L2 configurable to direct mapped SRAM interface or split cache/direct mapped or private memory
  - Core-to-L2 frequency divisors of 1, 1.5, 2, 2.5, and 3 supported
  - 64-bit data bus
  - Selectable interface voltages of 2.5V and 3.3V
  - Parity checking on both L2 address and data
- Memory Management Unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - 8 instruction BATs and 8 data BATs
  - 8 SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus Interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5V and 3.3V.
  - Parity checking on both address and data busses
- Power Management
  - Low-power design with thermal requirements very similar to PC740/750.
  - Selectable interface voltage of 1.8V/2.0V can reduce power in output buffers (compared to 3.3V)
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
- Integrated Thermal Management Assist Unit
  - One-ship thermal sensor and control logic
  - Thermal Management Interrupt for software regulation of junction temperature

6. Thermal Characteristics

6.1 Package Characteristics

Table 6-1 provides the package thermal characteristics for the PC755.

Table 6-1. Package Thermal Characteristics

Characteristic	Symbol	Value			Unit
		PC755 CBGA	PC755 PBGA	PC745 PBGA	
Junction-to-ambient thermal resistance, natural convection[1][2]	$R\theta_{JA}$	24	31	34	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board[1][3]	$R\theta_{JMA}$	17	25	26	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board[1][3]	$R\theta_{JMA}$	18	25	27	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board[1][3]	$R\theta_{JMA}$	14	21	22	°C/W
Junction-to-board thermal resistance[4]	$R\theta_{JB}$	8	17	17	°C/W
Junction-to-case thermal resistance[5]	$R\theta_{JC}$	< 0.1	< 0.1	< 0.1	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R\theta_{JC}$ for the part is less than 0.1°C/W.

Note: Refer to Section 6.1.3 "Thermal Management Information" on page 19 for more details about thermal management.

6.1.1 Package Thermal Characteristics for HiTCE

Table 6-2 provides the package thermal characteristics for the PC755, HiTCE.

Table 6-2. Package Thermal Characteristics for HiTCE Package

Characteristic	Symbol	Value		Unit
		PC755 HiTCE	PC745 HiTCE	
Junction-to-bottom of balls[1]	$R\theta_{J}$	6.8	6.5	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R\theta_{JMA}$	20.7[1][2]	20.9[1][4]	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.0	10.2[3]	°C/W

Notes:
1. Simulation, no convection air flow
2. Per JEDEC JESD51-6 with the board horizontal
3. Per JEDEC JESD51-8
4. Per JEDEC JESD51-2 with the board horizontal

6.1.2 Thermal Management Assistance

The PC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 6-4. More information on the use of this feature is given in the Freescale PC755 RISC Microprocessor User's manual.

Table 6-4. Thermal Sensor Specifications at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 16)

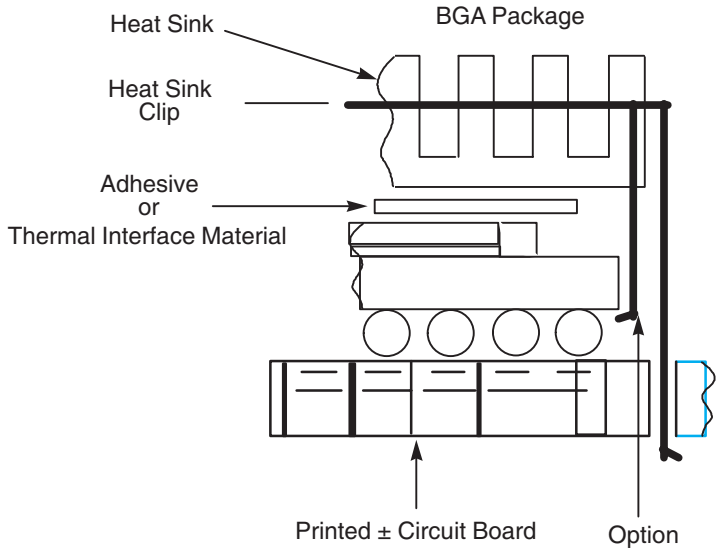
Characteristic	Min	Max	Unit
Temperature range(1)	0	127	°C
Comparator settling time(2)(3)	20	–	s
Resolution(3)	4	–	°C
Accuracy(3)	-12	+12	°C

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, "Programming the Thermal Assist Unit in the PC750 Microprocessor".
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

6.1.3 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design-the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 6-2. This spring force should not exceed 5.5 pounds of force.

Figure 6-2. Package Exploded Cross-Sectional View with Several Heat Sink Options



8.2.1 Clock AC Specifications

Table 8-2 provides the clock AC timing specifications as defined in "Absolute Maximum Ratings[1]" on page 14.

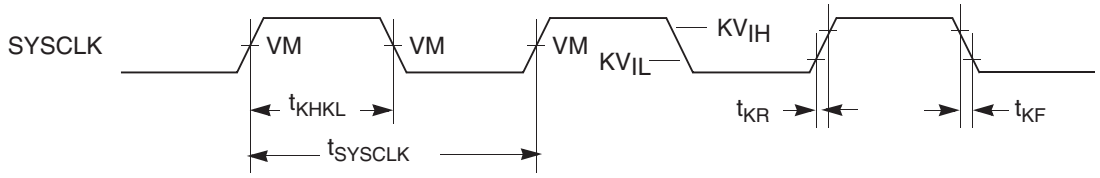
Table 8-2. Clock AC Timing Specifications at Recommended Operating Conditions (See "Recommended Operating Conditions[1]" on page 16)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit
		300 MHz		350 MHz		400 MHz		
		Min	Max	Min	Max	Min	Max	
Processor frequency[1]	f_{core}	200	300	200	350	200	400	MHz
VCO frequency[1]	f_{VCO}	400	600	400	700	400	800	MHz
SYSCLK frequency[1]	f_{SYSCLK}	25	100	25	100	25	100	MHz
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns
SYSCLK rise and fall time[2]	t_{KR} & t_{KF}	–	2	–	2	–	2	ns
	t_{KR} & t_{KF}	–	1.4	–	1.4	–	1.4	ns
SYSCLK duty cycle measured at $OV_{DD}/2$[3]	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%
SYSCLK jitter[3][4]		–	150	–	150	–	150	ps
Internal PLL relock time[3][5]		–	100	–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in Table 9-1 on page 39," for valid PLL_CFG[0-3] settings
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1v/ns is equivalent to a 2ns maximum rise/fall time measured at 0.4V and 2.4V or a rise/fall time of 1ns measured at 0.4V to 1.4V.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter – short term and long term combined and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 8-1 provides the SYSCLK input timing diagram.

Figure 8-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

8.2.1.1 *Processor Bus AC Specifications*

Table 8-3 on page 26 provides the processor bus AC timing specifications for the PC755 as defined in Figure 8-2 on page 26 and Figure 8-4 on page 28. Timing specifications for the L2 bus are provided in "L2 Clock AC Specifications" on page 28.

Table 8-3. Processor Bus Mode Selection AC Timing Specifications[1]
At V_{DD} = AV_{DD} = 2.0V 100 mV; -55 ≤T_J ≤+125°C, OV_{DD} = 3.3V 165 mV and OV_{DD} = 1.8V ± 100 mV and OV_{DD} = 2.0V 100 mV

Parameter	Symbols[2]	All Speed Grades		Unit
		Min	Max	
Mode select input setup to $\overline{\text{HRESET}}$[3][4][5][6][7]	t_{MVRH}	8	–	t_{SYSCLk}
$\overline{\text{HRESET}}$ to mode select input hold[3][4][6][7][8]	t_{MXRH}	0	–	ns

Notes:
1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (See Figure 8-2). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. THe symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going highs) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs – and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX). For additional explanation of AC timing specifications in Freescale PowerPC microprocessors, see the application note “Understanding AC Timing Specifications for PowerPC Microprocessors.”
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 8-2).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0-3]
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Figure 8-2 provides the mode select input timing diagram for the PC755.

Figure 8-2. Mode Input Timing Diagram

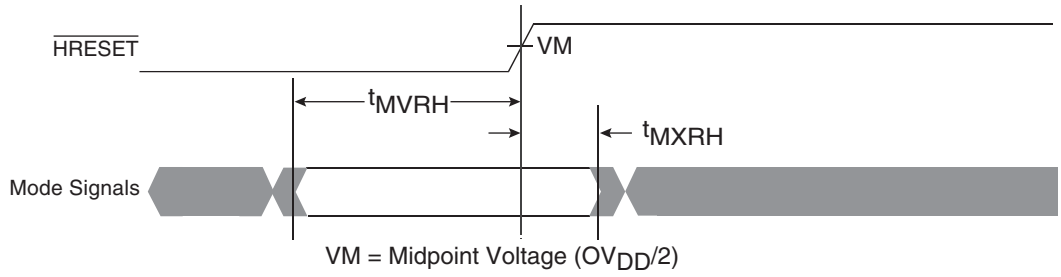


Figure 8-3 provides the AC test load for the PC755.

Figure 8-3. AC Test Load

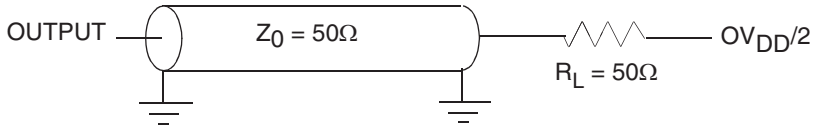
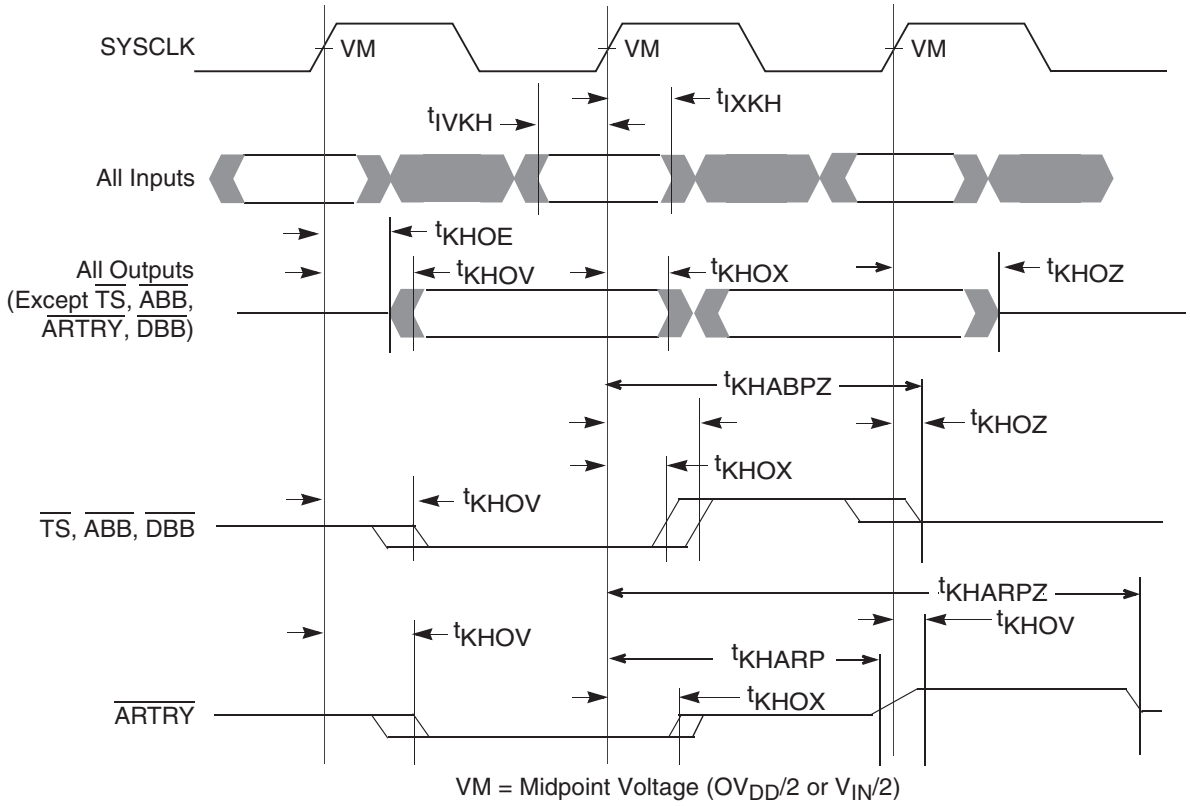


Figure 8-4 provides the input/output timing diagram for the PC755.

Figure 8-4. Input/Output Timing Diagram



8.2.1.2 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 8-5 on page 29 for example core and L2 frequencies at various divisors. Table 8-5 provides the potential range of L2CLK output AC timing specifications as defined in Figure 8-5 on page 30.

The minimum L2CLK frequency of Table 8-5 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 8-5 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC755 will be a function of the AC timings of the PC755, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 8-5. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

Table 8-7. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (Continued)

Parameter	Symbol	Min	Max	Unit
Input Setup Times:[3] - Boundary-scan data - TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 - -	 ns
Input Hold Times:[3] - Boundary-scan data - TMS, TDI	 t_{DXJH} t_{IXJH}	 15 12	 - -	 ns
Valid Times:[4] - Boundary-scan data - TDO	 t_{JLDV} t_{JLOV}	 - -	 4 4	 ns
Output Hold Times:[4] - Boundary-scan data - TDO	 t_{JLDV} t_{JLOV}	 25 12	 - -	 ns
TCK to output high impedance:[4][5] - Boundary-scan data - TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	 ns

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 8-9). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 8-9 provides the AC test load for TDO and the boundary-scan outputs of the PC755.

Figure 8-9. Alternate AC Test Load for the JTAG Interface

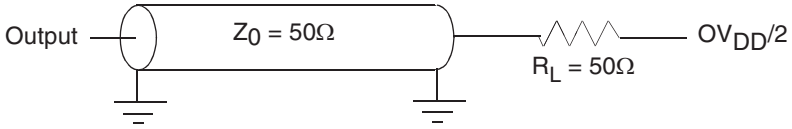
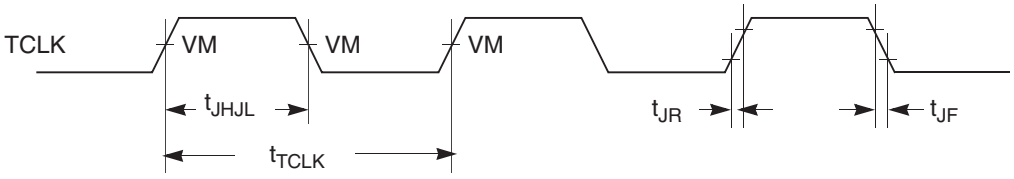


Figure 8-10 provides the JTAG clock input timing diagram.

Figure 8-10. JTAG Clock Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

8.2.2.1 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

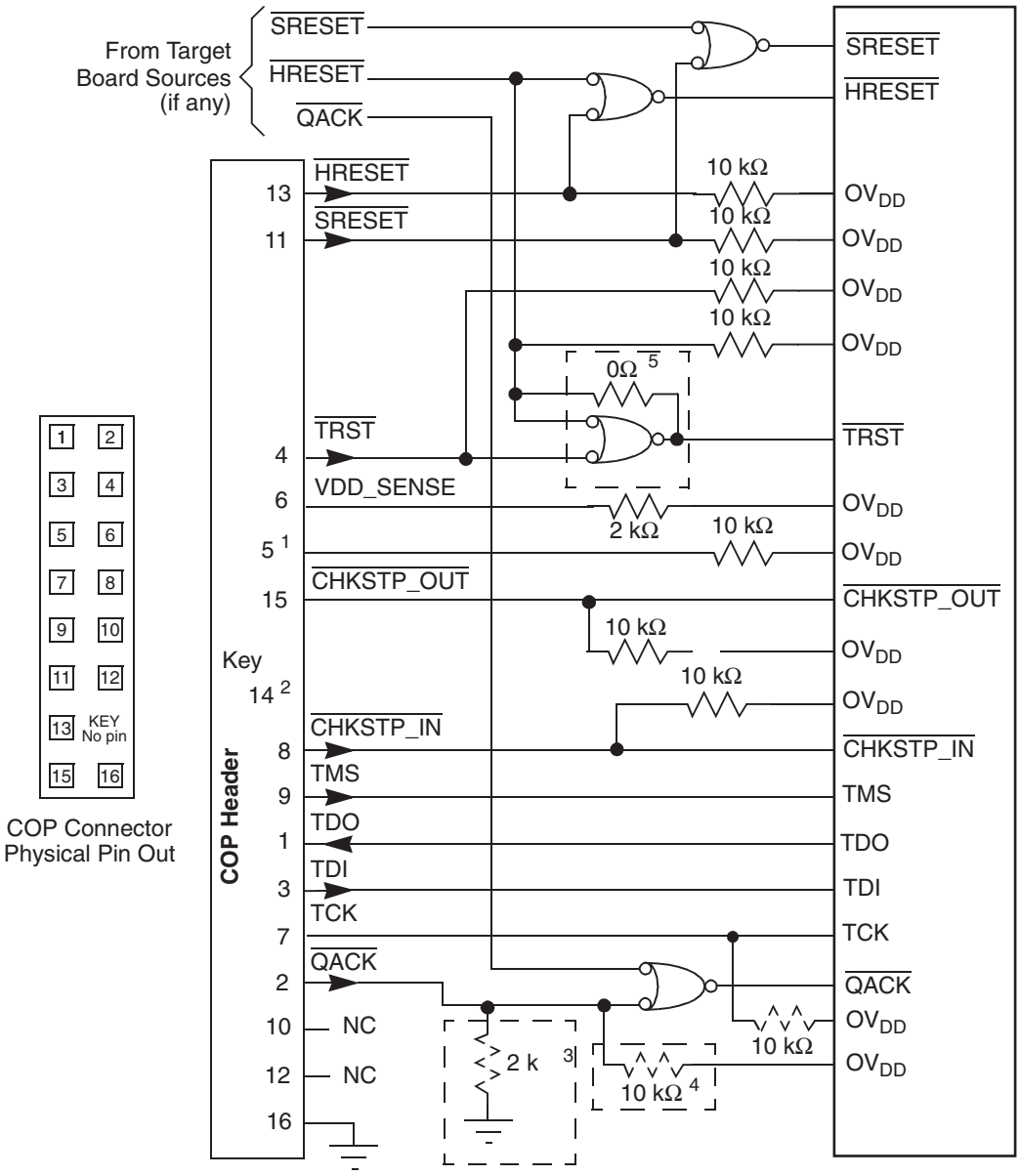
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must bemerged into these signals with logic.

The arrangement shown in Figure 8-14 on page 36 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω isolation resistor so that it is asserted when the systemreset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 8-14, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interfacemay need to be wired onto the system in debug situations.

The COP header shown in Figure 8-14 adds many benefits — breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface — and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

Figure 8-14. JTAG Interface Connection



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC755. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.

The COP header shown in Figure 8-15 on page 37 adds many benefits—breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

9.4 Clock Relationship Choices

The PC755's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755 is shown in Figure 10-2 on page 41 for example frequencies.

Table 9-1. PC755 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	**Core-to VCO Multiplier**	**Bus 33 MHz**	**Bus 50 MHz**	**Bus 66 MHz**	**Bus 75 MHz**	**Bus 80 MHz**	**Bus 100 MHz**
0100	2x	2x	-	-	-	-	-	200 (400)
1000	3x	2x	-	-	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	-	-	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	-	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	-	225 (450)	300 (600)	338 (675)	360 (720)	-
1011	5x	2x	-	250 (500)	333 (666)	375 (750)	400 (800)	-
1001	5.5x	2x	-	275 (550)	366 5733°	-	-	-
1101	6x	2x	200 (400)	300 (600)	400 (800)	-	-	-
0101	6.5x	2x	216 (433)	325 (650)	-	-	-	-
0010	7x	2x	233 (466)	350 (700)	-	-	-	-
0001	7.5x	2x	250 (500)	375 (750)	-	-	-	-
1100	8x	2x	266 (533)	400 (800)	-	-	-	-
0110	10x	2x	333 (666)	-	-	-	-	-
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755; see "Clock AC Specifications" on page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the PC755 regardless of the SYSCLK input.

The PC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the PC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the PC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC755 core, and the phase adjustment range that the L2 DLL supports. Figure 8-9 on page 33 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 9-2. Sample Core-to-L2 Frequencies

Core Frequency in MHz	1	1.5	2	2.5	3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122
375	375	250	188	150	125
400	400	266	200	160	133

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the PC755; see "L2 Clock AC Specifications" on page 28 for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

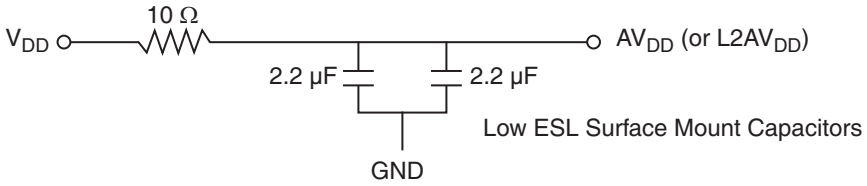
10. System Design Information

10.1 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the PC755 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 10-2 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route but is proportionately less critical.

Figure 10-1. PLL Power Supply Filter Circuit



10.2 Power Supply Voltage Sequencing

The notes in Figure 10-3 on page 43 contain cautions about the sequencing of the external bus voltages and core voltage of the PC755 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the ESD (Electrostatic Discharge) protection diodes will be forward biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit of Figure 10-3 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 10-3 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

Figure 10-2. Example Voltage Sequencing Circuit

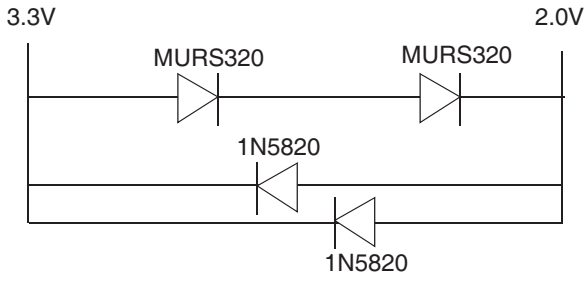


Table 10-1 summarizes the signal impedance results. The driver impedance values were characterized at 0°C, 65°C, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 10-1. Impedance Characteristics. V_{DD} = 2.0V, OV_{DD} = 3.3V, T_c = 0 - 105°C

Impedance	Processor bus	L2 bus	Symbol	Unit
RN	25-36	25-36	Z_0	W
RP	26-39	26-39	Z_0	W

10.6 Pull-up Resistor Requirements

The PC755 requires pull-up resistors (1 kΩ – 5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the processor or other bus masters. These pins are $\overline{TS}$, $\overline{ABB}$, $\overline{AACK}$, $\overline{ARTRY}$, $\overline{DBB}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{TEA}$, and $\overline{DBDIS}$. $\overline{DRTRY}$ should also be connected to a pull-up resistor (1 kΩ – 5 kΩ) if it will be used by the system; otherwise, this signal should be connected to $\overline{HRESET}$ to select NO-DRTRY mode.

Three test pins also require pull-up resistors (100Ω – 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ – 5 kΩ) if it is used by the system.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the processor must continually monitor these signals for snooping, this float condition may cause additional power draw by the input receivers on the processor or by other receivers in the system. These signals can be pulled up through weak (10 kΩ) pull-up resistors by the system or may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw, but address bus pull-up resistors are not necessary for proper device operation. The snooped address and transfer attribute inputs are:
A[0:31], AP[0:3], TT[0:4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

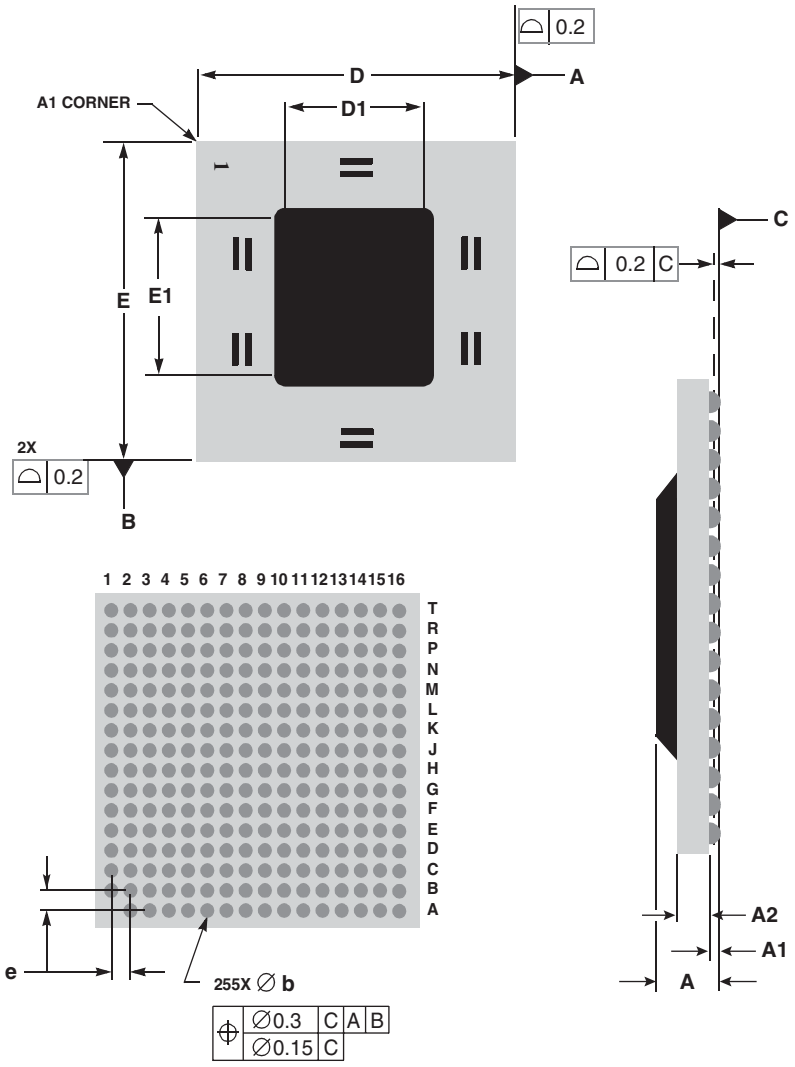
If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

11.1.1 Mechanical Dimensions of the PC745 HiTCE Package

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature of the PC745, 255 HiTCE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature of the PC745 HiTCE



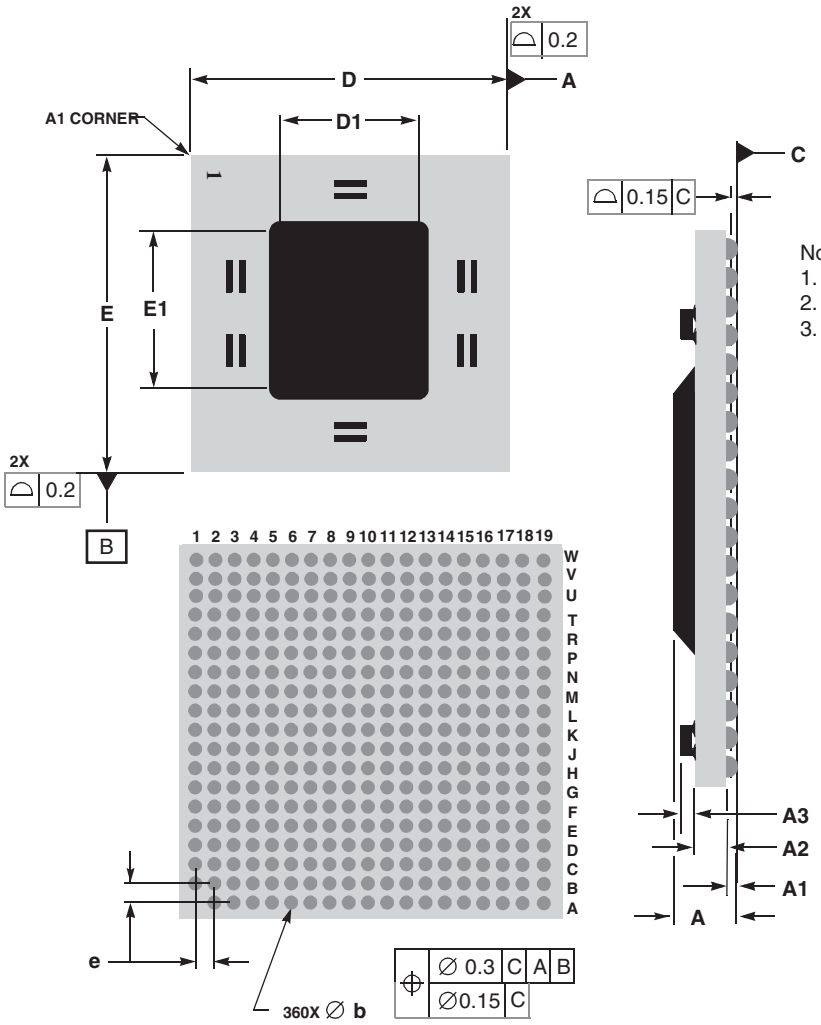
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array
4. Capacitor Pads may be unpopulated

	Millimeters	
Dim	**Min**	**Max**
A	2.42	3.08
A1	0.8	1.0
A2	0.90	1.14
b	0.82	0.93
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.3 Mechanical Dimensions of the PC755 HiTCE Package

Figure 11-5 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 HiTCE package.

Figure 11-5. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (HiTCE)



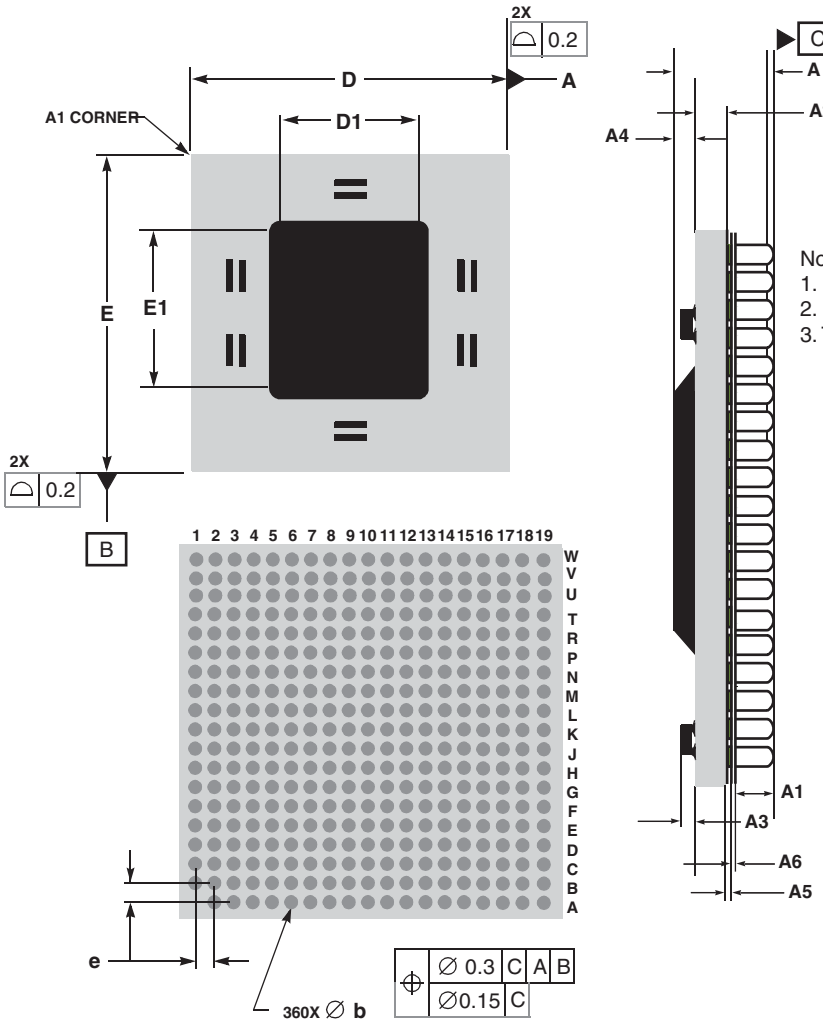
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.24
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.4 Mechanical Dimensions of the PC755 CI-CGA Package

Figure 11-6 provides the mechanical dimensions and bottom surface nomenclature of PC755, 360 CI-CGA package.

Figure 11-6. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (CI-CGA)



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	4.08 BSC	
A1	1.545	1.695
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.9
A5	0.14 BSC	
A6	0.25	0.35
b	0.79	0.990
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

13. Definitions

13.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnity Atmel for any damages resulting from such improper use or sale.

13.2 Differences with Commercial Part

	Commercial part	Military part
Temperature range	T_J = 0 to 105° C	T_J = -55°C to 125°C

14. Document Revision History

Table 14-1 provides a revision history for this hardware specification.

Table 14-1. Revision History

Revision Number	Date	Substantive Change(s)
2138G	04/2006	Increased power specification for 350 MHz full-power mode in Table 7-1 on page 23. Updated ordering information to new Template.
2138F	05/2005	Added HiTCE package for PowerPC 745 Removed phrase "for the ceramic ball grid array (CBGA) package" from Section 6.1.3 on page 19; this information applies to devices in all packages Figure 8-14 on page 36: updated COP Connector Diagram to recommend a weak pull-up resistor on TCK
2138E	10/2004	Product specification release subsequent to product qualification Motorola changed to Freescale
2138D	06/2003	Preliminary β-site

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