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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	360-BBGA Exposed Pad
Supplier Device Package	360-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx755bvzfu300le

Screening

This product is manufactured in full compliance with:

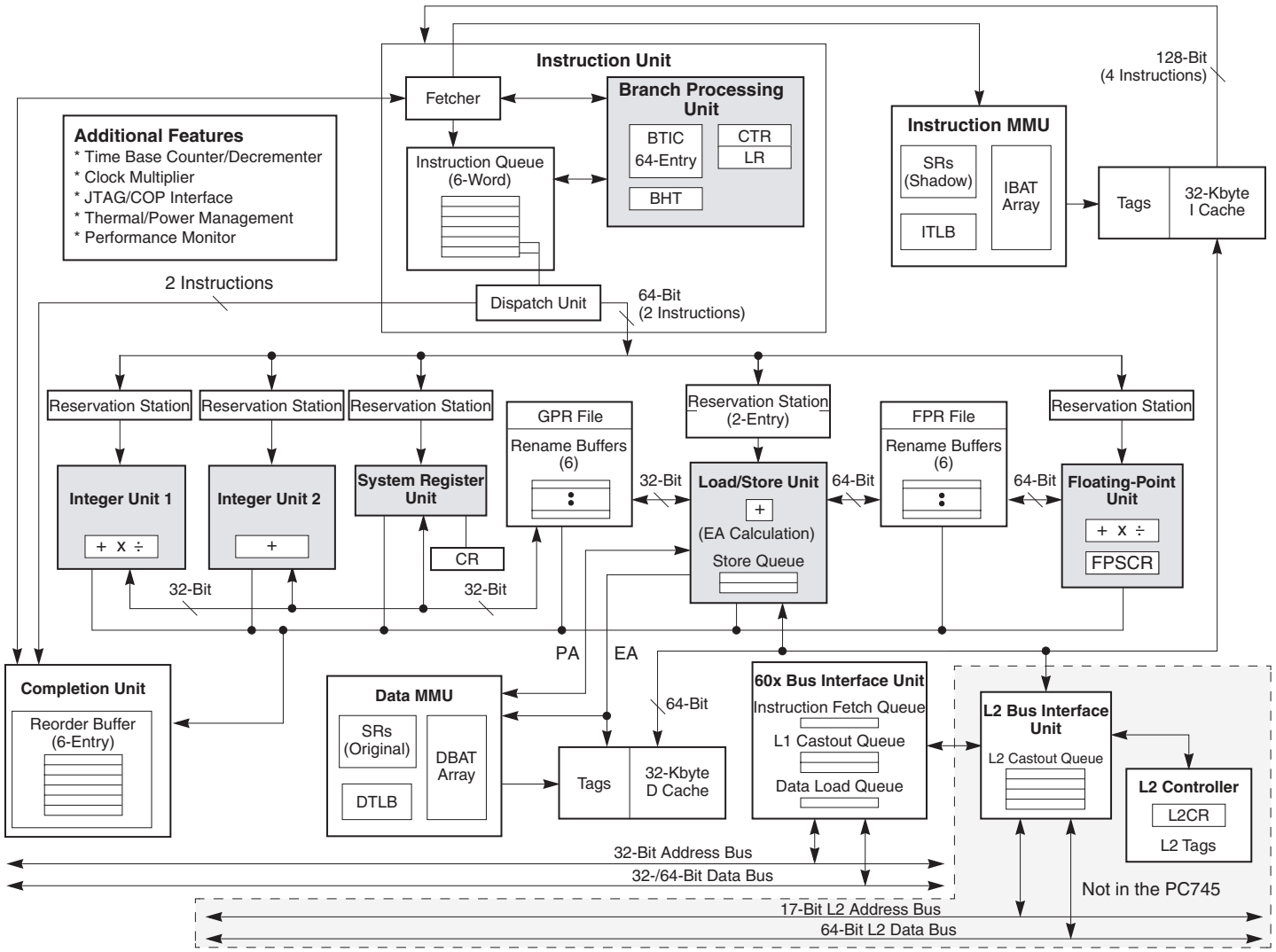
- HiTCE CBGA according to Atmel standards
- CBGA + CI-CGA + FC-PBGA up screenings based upon Atmel standards
- Full military temperature ranges (T_J = -55°C, +125°C)
- Industrial temperature ranges (T_J = -40°C, +110°C)

1. General Description

1.1 Simplified Block Diagram

The PC755 is targeted for low power systems and supports power management features such as doze, nap, sleep, and dynamic power management. The PC755 consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus.

Figure 1-1. PC755 Block Diagram



1.2 General Parameters

The following list provides a summary of the general parameters of the PC755:

Technology	0.22 µm CMOS, five-layer metal, 1 layer poly
Die size	6.61 mm x 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static Packages
PC745	Surface mount 255 Plastic Ball Grid Array (PBGA) Surface mount 255 Ceramic Ball Grid Array (Hi-TCE)
PC755	Surface mount 360 Plastic Ball Grid Array (PBGA) Surface mount 360 Ceramic Ball Grid Array (CI-CGA, CBGA, HiTCE)
Core power supply	2V ± 100 mV DC (nominal; some parts support core voltages down to 1.8V; see "Recommended Operating Conditions(1)" on page 16
I/O power supply	2.5V ± 100 mV DC or 3.3V ± 165 mV DC (input thresholds are configuration pin selectable)

1.3 Features

This section summarizes features of the PC755's implementation of the PowerPC architecture. Major features of the PC755 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry Branch History Table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 6 entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes

- Fixed Point Units (FXUs) that share 32 GPRs for Integer Operands
  - Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)-shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point Unit and a 32-entry FPR File
  - Support for IEEE-754 standard single and double precision floating point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/Store Unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and Little-endian byte addressing supported
  - Misaligned Little-endian supported
  - Level 1 Cache structure
  - 32K, 32 bytes line, 8-way set associative instruction cache (iL1)
  - 32K, 32 bytes line, 8-way set associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently used (PLRU) replacement
  - Copy-back or Write Through data cache (on a page per page basis)
  - Supports all PowerPC memory coherency modes
  - Non-Blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) Cache Interface (not implemented on PC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1-Mbyte 2-way set associative L2 cache support

2. Pin Assignments

Figure 2-1 (in part A) shows the pinout of the PC745, 255PBGA and HiTCE CBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Figure 2-1. Pinout of the PC745, 255 PBGA and HiTCE CBGA Packages as Viewed from the Top Surface

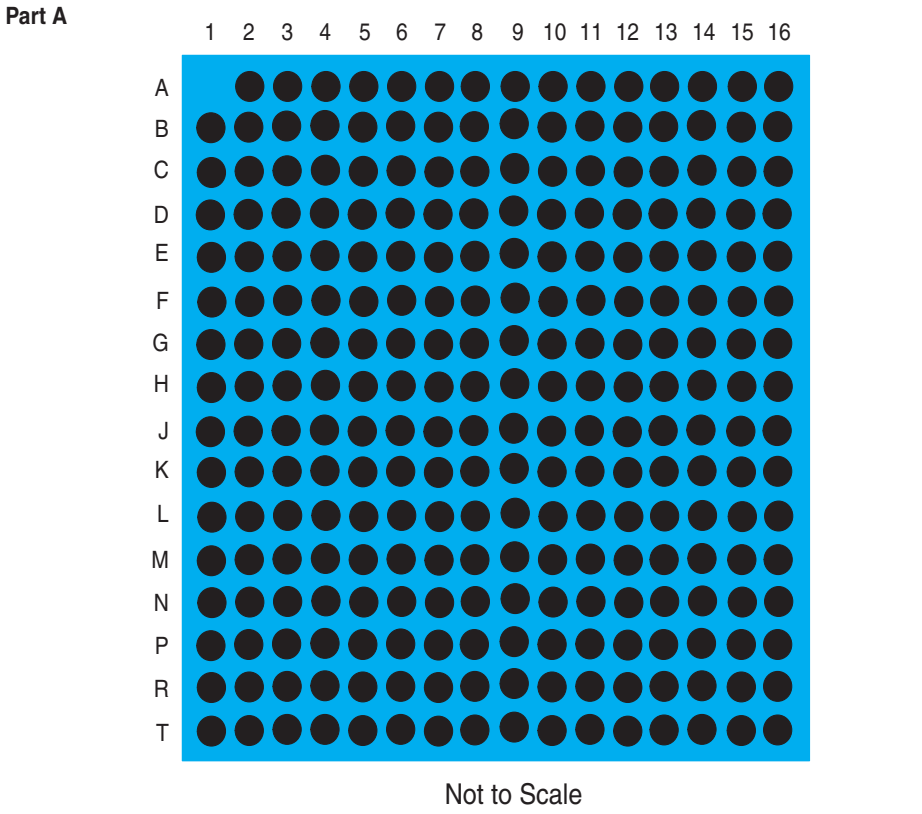
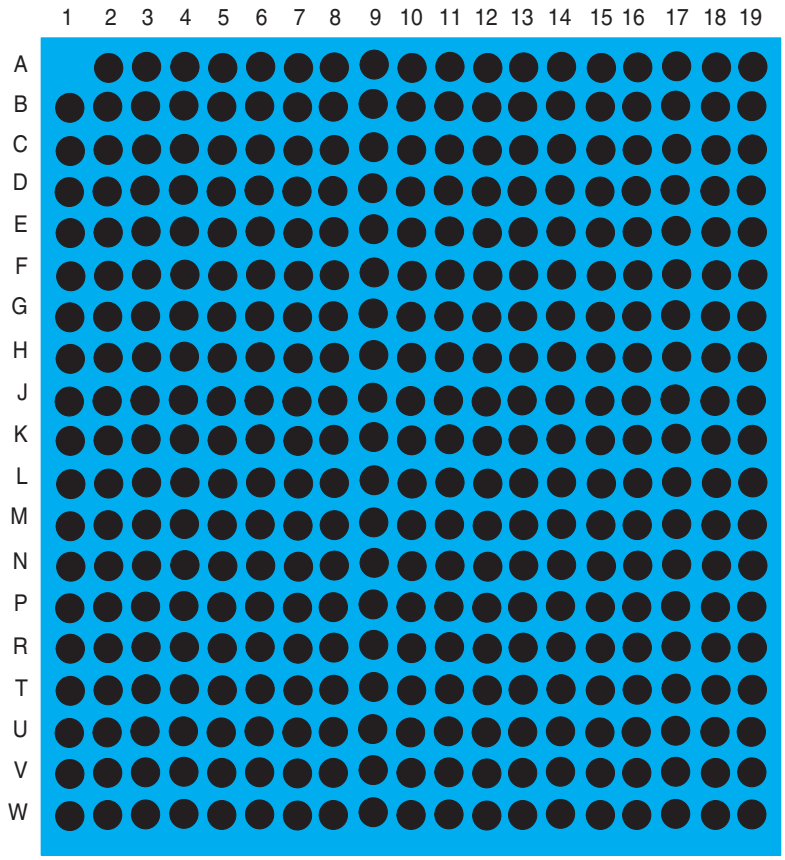


Figure 2-2 (in part A) shows the pinout of the PC755, 360 PBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Figure 2-2. Pinout of the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages as Viewed from the Top Surface

Part A



Not to Scale

Part B

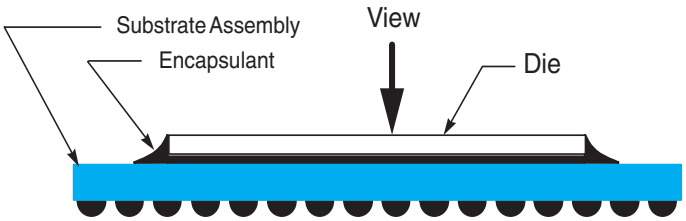


Table 2-2 provides the pinout listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8]

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	–	–
$\overline{\text{AACK}}$	N3	Low	Input	–	–
$\overline{\text{ABB}}$	L7	Low	I/O	–	–
AP[0-3]	C4, C5, C6, C7	High	I/O	–	–
$\overline{\text{ARTRY}}$	L6	Low	I/O	–	–
AVDD	A8	-	-	2V	2V
$\overline{\text{BG}}$	H1	Low	Input	–	–
$\overline{\text{BR}}$	E7	Low	Output	–	–
BVSEL[3][5][6]	W1	High	Input	GND	3.3V
$\overline{\text{CI}}$	C2	Low	Output	–	–
CKSTP_IN	B8	Low	Input	–	–
CKSTP_OUT	D7	Low	Output	–	–
CLK_OUT	E3	–	Output	–	–
$\overline{\text{DBB}}$	K5	Low	I/O	–	–
$\overline{\text{DBDIS}}$	G1	Low	Input	–	–
$\overline{\text{DBG}}$	K1	Low	Input	–	–
$\overline{\text{DBWO}}$	D1	Low	Input	–	–
DH[0-31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	–	–
DL[0-31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	–	–
DP[0-7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	–	–
$\overline{\text{DRTRY}}$	H6	Low	Input	–	–
$\overline{\text{GBL}}$	B1	Low	I/O	–	–
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	–	–	GND	GND
$\overline{\text{HRESET}}$	B6	Low	Input	–	–
$\overline{\text{INT}}$	C11	Low	Input	–	–
L1_TSTCLK[2]	F8	High	Input	–	–
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	–	–

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
L2AVDD	L13	–	–	2V	2V
$\overline{\text{L2CE}}$	P17	Low	Output	–	–
L2CLKOUTA	N15	–	Output	–	–
L2CLKOUTB	L16	–	Output	–	–
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	–	–
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	–	–
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	–	–	1.8V/2V	3.3V
L2SYNC_IN	L14	–	Input	–	–
L2SYNC_OUT	M14	–	Output	–	–
L2_TSTCLK[2]	F7	High	Input	–	–
L2VSEL[1][3][5][6]	A19	High	Input	GND	3.3V
$\overline{\text{L2WE}}$	N16	Low	Output	–	–
L2ZZ	G17	High	Output	–	–
$\overline{\text{LSSD\_MODE}}$[2]	F9	Low	Input	–	–
$\overline{\text{MCP}}$	B11	Low	Input	–	–
NC (No-Connect)	B3, B4, B5, W19, K9, K11[4], K19[4]	–	–	–	–
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	–	–	1.8V/2V	3.3V
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input	–	–
$\overline{\text{QACK}}$	B2	Low	Input	–	–
$\overline{\text{QREQ}}$	J3	Low	Output	–	–
$\overline{\text{RSRV}}$	D3	Low	Output	–	–
$\overline{\text{SMI}}$	A12	Low	Input	–	–
$\overline{\text{SRESET}}$	E10	Low	Input	–	–
SYSCLK	H9	–	Input	–	–
$\overline{\text{TA}}$	F1	Low	Input	–	–
TBEN	A2	High	Input	–	–
$\overline{\text{TBST}}$	A11	Low	I/O	–	–
TCK	B10	High	Input	–	–
TDI[6]	B7	High	Input	–	–
TDO	D9	High	Output	–	–

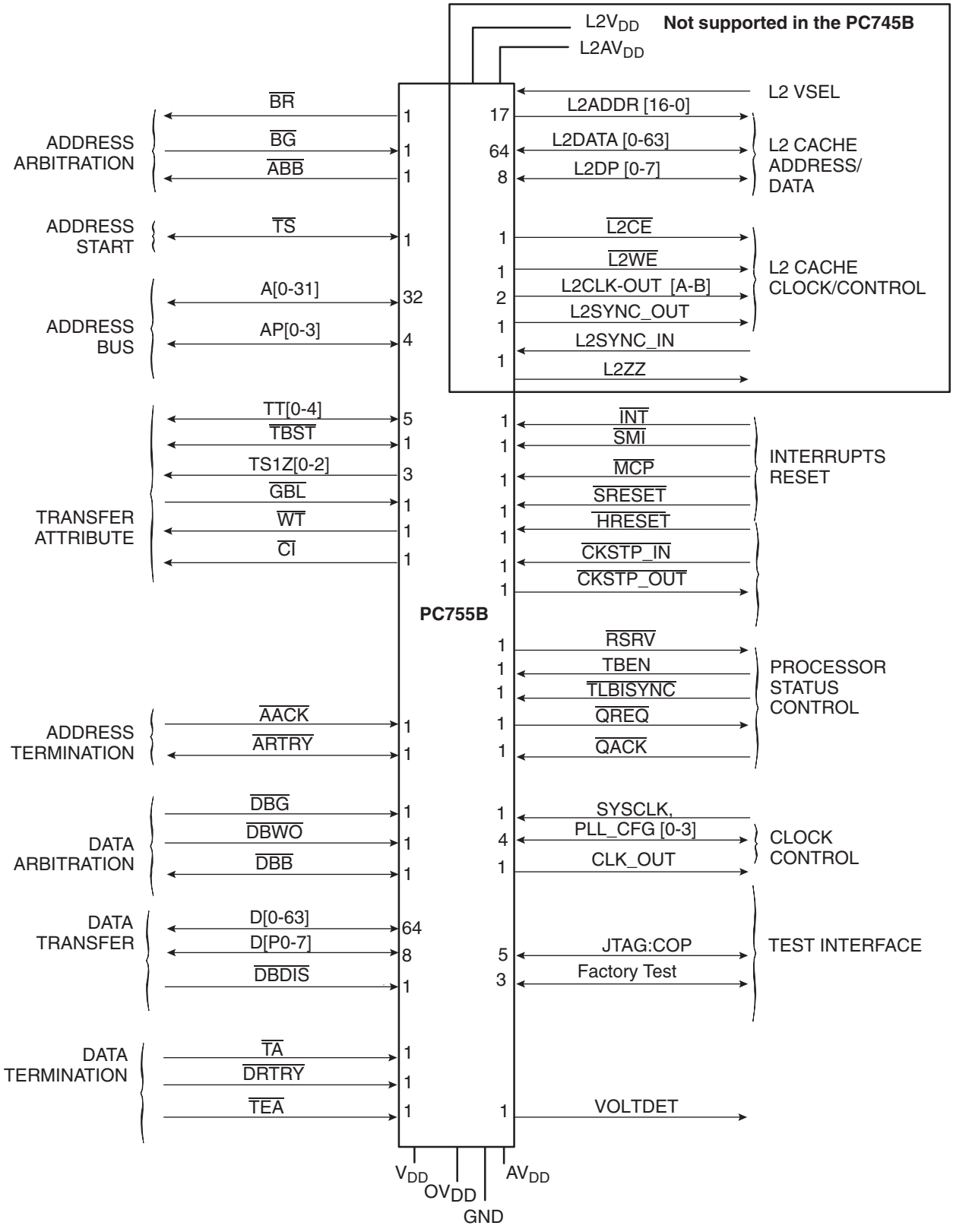
Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
$\overline{\text{TEA}}$	J1	Low	Input	–	–
$\overline{\text{TLBISYNC}}$	A3	Low	Input	–	–
TMS[6]	C8	High	Input	–	–
$\overline{\text{TRST}}$[6]	A10	Low	Input	–	–
$\overline{\text{TS}}$	K7	Low	I/O	–	–
TSIZ[0-2]	A9, B9, C9	High	Output	–	–
TT[0-4]	C10, D11, B12, C12, F11	High	I/O	–	–
$\overline{\text{WT}}$	C3	Low	Output	–	–
VDD	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	–	–	2V	2V
VOLTDET[7]	K13	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0-16], L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 5-1 on page 15 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see "Recommended Operating Conditions[1]" on page 16.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of 9 existing no-connects in PC750's 360-BGA package.
6. Internal pull up on die.
7. Internally tied to $L2OV_{DD}$ in the PC755 360-BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.
8. This is different from the PC745 255-BGA package.

3. Signal Description

Figure 3-1. PC755 Microprocessor Signal Groups



4. Detailed Specifications

This specification describes the specific requirements for the microprocessor PC755, in compliance with Atmel Grenoble standard screening.

5. Applicable Documents

1) MIL-STD-883: Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

Depending on the package, the terminal connections is shown in Table 2-1 on page 8, Table 2-2 on page 10 and Figure 3-1 on page 13.

5.1.2 Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage[4]		V_{DD}	-0.3 to 2.5	V
PLL supply voltage[4]		AV_{DD}	-0.3 to 2.5	V
L2 DLL supply voltage[4]		$L2AV_{DD}$	-0.3 to 2.5	V
Processor bus supply voltage[3]		OV_{DD}	-0.3 to 3.6	V
L2 bus supply voltage[3]		$L2OV_{DD}$	-0.3 to 3.6	V
Input voltage	Processor bus[2][5]	V_{IN}	-0.3 to OV_{DD} + 0.3V	V
	L2 Bus[2][5]	V_{IN}	-0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{IN}	-0.3 to 3.6	V
Storage temperature range		T_{STG}	-55/+150	°C

Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions[1]" on page 16. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3V for up to 20 ms, or by 2.5V for up to 40 ms. Excursions beyond 3.3V or 40 ms are not supported.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0V for up to 20 ms, or by 0.7V for up to 40 ms. Excursions beyond 1.0V or 40 ms are not supported.
5. This is a DC specifications only. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5-1 on page 15.

8. Electrical Characteristics

8.1 Static Characteristics

Table 8-1. DC Electrical Specifications at Recommended Operating Conditions (see "Recommended Operating Conditions[1]" on page 16)

Characteristic	Nominal bus Voltage[1]	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSLCK)[2][3]	2.5	V_{IH}	1.6	(L2)OV_{DD} + 0.3	V
	3.3	V_{IH}	2	(L2)OV_{DD} + 0.3	V
Input low voltage (all inputs except SYSLCK)[2]	2.5	V_{IL}	-0.3	0.6	V
	3.3	V_{IL}	-0.3	0.8	V
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V
SYSCLK input low voltage	2.5	KV_{IL}	-0.3	0.4	V
	3.3	KV_{IL}	-0.3	0.4	V
Input leakage current, [2][3] V_{IN} = $L2OV_{DD}$/OV_{DD}		I_{in}	–	10	µA
Hi-Z (off-state) leakage current, [2][3][5] V_{IN} = $L2OV_{DD}$/OV_{DD}		I_{TSI}	–	10	µA
Output high voltage, I_{OH} = -6 mA	2.5	V_{OH}	1.7	–	V
	3.3	V_{OH}	2.4	–	V
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	–	0.45	V
	3.3	V_{OL}	–	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz [3][4]		C_{in}	–	5	pF

Notes:
1. Nominal voltages; See "Recommended Operating Conditions[1]" on page 16.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).

8.2 Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in "Clock AC Specifications" on page 25 and tested for conformance to the AC specifications for that frequency. These specifications are for 275, 300, 333 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0-3] signals. Parts are sold by maximum processor core frequency.

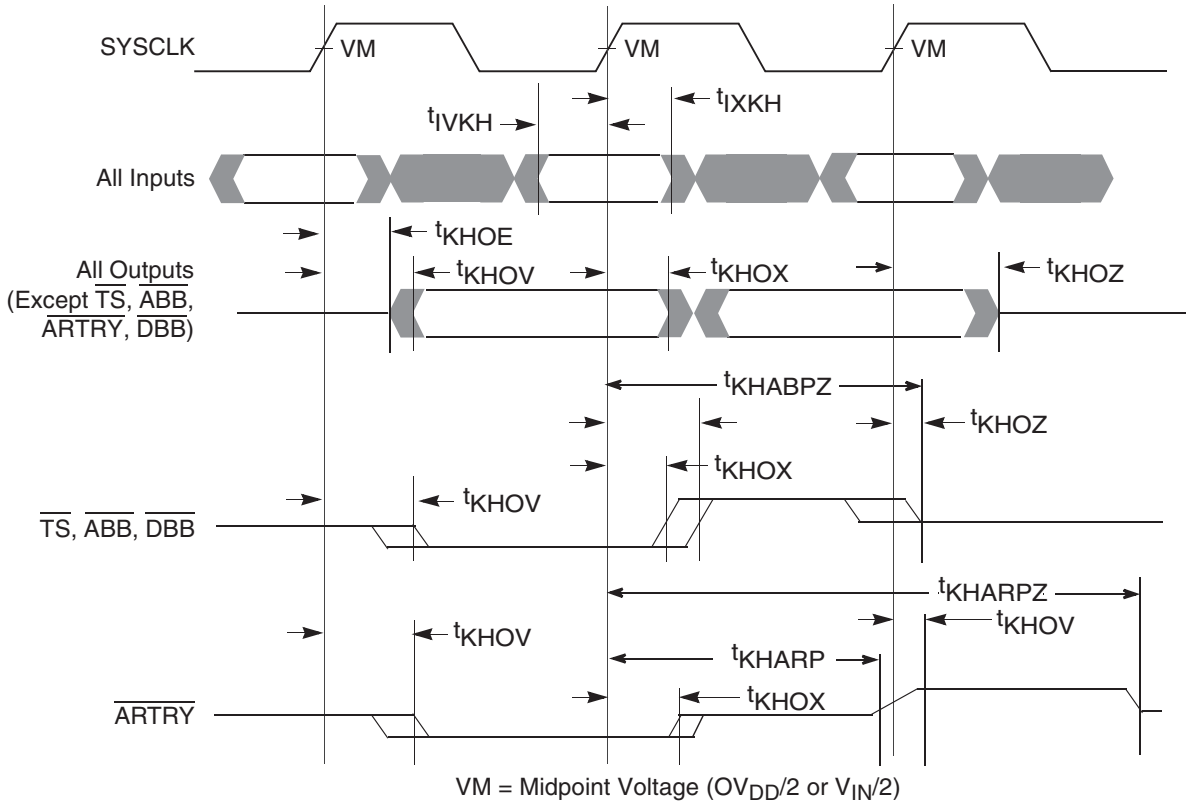
Table 8-4. Processor Bus AC Timing Specifications[1] at Recommended Operating Conditions

Parameter	Symbols	All Speed Grades		Unit
		Min	Max	
Setup Times: All Inputs	t_{IVKH}	2.5	–	ns
Input Hold Times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.6	–	ns
Input Hold Times: All Inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.2	–	ns
Valid Times: All Outputs	t_{KHOV}	–	4.1	ns
Output Hold Times: All Outputs	t_{KHOX}	1	–	ns
SYSCLK to Output Enable[2]	t_{KHOE}	0.5	–	ns
SYSCLK to Output High Impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)[2]	t_{KHOZ}	–	6	ns
SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ High Impedance After Precharge[2][3][4]	t_{KHABPZ}	–	1	t_{SYSCLK}
Maximum Delay to $\overline{\text{ARTRY}}$ Precharge[2][3][5]	t_{KHARP}	–	1	t_{SYSCLK}
SYSCLK to $\overline{\text{ARTRY}}$ High Impedance After Precharge[2][3][5]	t_{KHARPZ}	–	2	t_{SYSCLK}

Notes:
1. Revisions prior to Rev 2.8 (Rev E) were limited in performance and did not conform to this specification. Contact your local Freescale sales office for more information.
2. Guaranteed by design and characterization.
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6-1 on page 18. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 x t_{SYSCLK}, i.e. less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following AACK will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; i.e., it should be high-Z as shown in Figure 6-1 on page 18 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.

Figure 8-4 provides the input/output timing diagram for the PC755.

Figure 8-4. Input/Output Timing Diagram



8.2.1.2 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 8-5 on page 29 for example core and L2 frequencies at various divisors. Table 8-5 provides the potential range of L2CLK output AC timing specifications as defined in Figure 8-5 on page 30.

The minimum L2CLK frequency of Table 8-5 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 8-5 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC755 will be a function of the AC timings of the PC755, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 8-5. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

8.2.1.3 L2 Bus Input AC Specifications

Table 8-6 provides the L2 bus interface AC timing specifications for the PC755 as defined in Figure 8-6 on page 32 and Figure 8-7 on page 32 for the loading conditions described in Figure 8-8 on page 32.

Table 8-6. L2 Bus Interface AC Timing Specifications at Recommended Operating Conditions

Parameter	Symbol	All Speed Grades		Unit
		Min	Max	
L2SYNC_IN rise and Fall Time(1)	t_{L2CR} & t_{L2CF}	–	1.0	ns
Setup Times: Data and Parity(2)	t_{DVL2CH}	1.2	-	ns
Input Hold Times: Data and Parity(2)	t_{DXL2CH}	0	-	ns
Valid Times: (3)(4)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOV}	-	3.1	ns
All Outputs when L2CR[14-15] = 01		-	3.2	
All Outputs when L2CR[14-15] = 10		-	3.3	
All Outputs when L2CR[14-15] = 11		-	3.7	
Output Hold Times: (3)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOX}	0.5	-	ns
All Outputs when L2CR[14-15] = 01		0.7	-	
All Outputs when L2CR[14-15] = 10		0.9	-	
All Outputs when L2CR[14-15] = 11		1.1	-	
L2SYNC_IN to High Impedance:(3)(5)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOZ}	-	2.4	ns
All Outputs when L2CR[14-15] = 01		-	2.6	
All Outputs when L2CR[14-15] = 10		-	2.8	
All Outputs when L2CR[14-15] = 11		-	3.0	

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 6-3 on page 20). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 8-1 on page 25).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14-15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14-15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev 2.8 (Rev E) were limited in performance.and did not conform to this specification. Contact your local Atmel sales office for more information.

9.4 Clock Relationship Choices

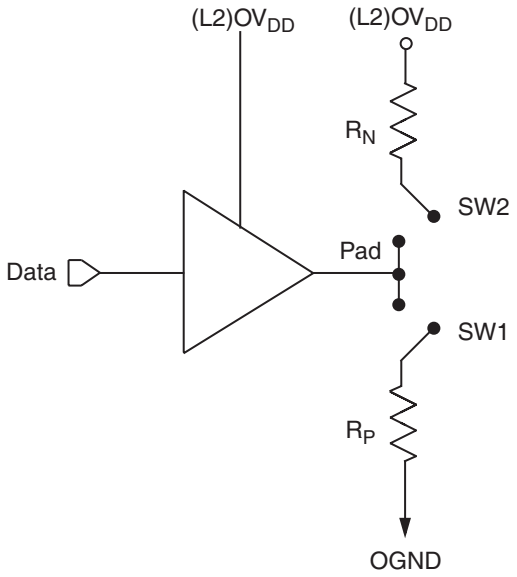
The PC755's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755 is shown in Figure 10-2 on page 41 for example frequencies.

Table 9-1. PC755 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	**Core-to VCO Multiplier**	**Bus 33 MHz**	**Bus 50 MHz**	**Bus 66 MHz**	**Bus 75 MHz**	**Bus 80 MHz**	**Bus 100 MHz**
0100	2x	2x	-	-	-	-	-	200 (400)
1000	3x	2x	-	-	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	-	-	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	-	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	-	225 (450)	300 (600)	338 (675)	360 (720)	-
1011	5x	2x	-	250 (500)	333 (666)	375 (750)	400 (800)	-
1001	5.5x	2x	-	275 (550)	366 5733°	-	-	-
1101	6x	2x	200 (400)	300 (600)	400 (800)	-	-	-
0101	6.5x	2x	216 (433)	325 (650)	-	-	-	-
0010	7x	2x	233 (466)	350 (700)	-	-	-	-
0001	7.5x	2x	250 (500)	375 (750)	-	-	-	-
1100	8x	2x	266 (533)	400 (800)	-	-	-	-
0110	10x	2x	333 (666)	-	-	-	-	-
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755; see "Clock AC Specifications" on page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the PC755 regardless of the SYSCLK input.

Figure 10-3. Driver Impedance Measurement Circuit

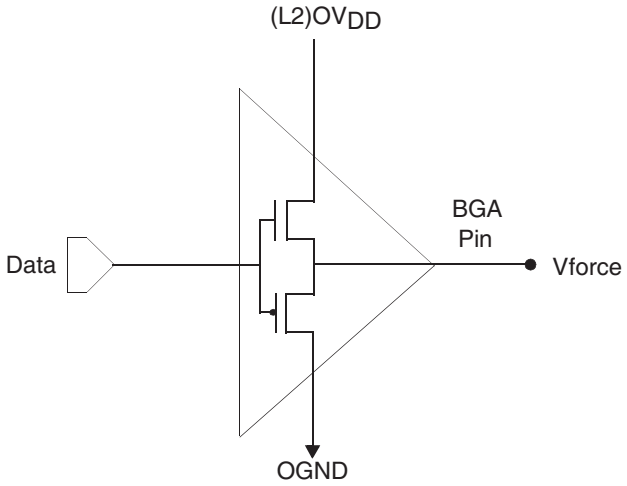


Alternately, the following is another method to determine the output impedance of the PC755. A voltage source, V_{force}, is connected to the output of the PC755 as in Figure 10-4. Data is held low, the voltage source is set to a value that is equal to (L2)OV_{DD}/2 and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to (L2)OV_{DD}/2, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, (L2)OV_{DD}/2, by the current sank by the pull-up when the data is high and V_{force} is equal to (L2)OV_{DD}/2. This method can be employed with either empirical data from a test set up or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 10-4 describes the alternate driver impedance measurement circuit.

Figure 10-4. Alternate Driver Impedance Measurement Circuit



11. Package Mechanical Data

The following sections provide the package parameters and mechanical dimensions for the PC745, 255 PBGA package as well as the PC755, 360 CBGA and PBGA packages. While both the PC755 plastic and the ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, please contact your local Atmel sales office.

11.1 Package Parameters for the PC745

The package parameters are as provided in the following list. The package type is 21 × 21 mm, 255-lead plastic ball grid array (PBGA).

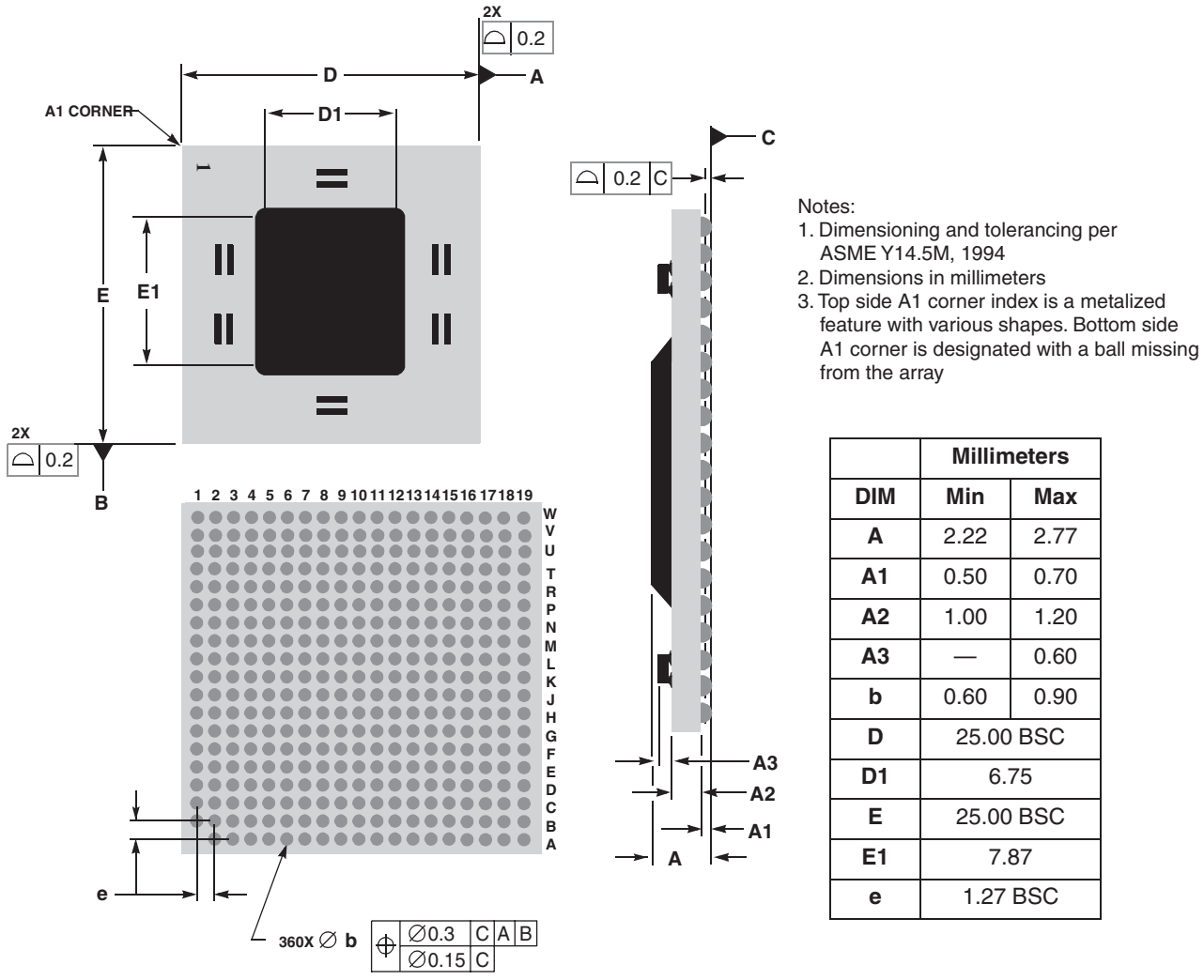
Table 11-1. Package Parameters

Parameter	HiTCE	PBGA
Package outline	21 × 21 mm	21 × 21 mm
Interconnects	255 (16 × 16 ball array – 1)	255 (16 × 16 ball array – 1)
Pitch	1.27 mm (50 mil)	1.27 mm (50 mil)
Minimum module height	2.42	2.25 mm
Maximum module height	3.08	2.80 mm
Ball diameter (typical)	0.89 mm (35 mil)	0.75 mm (29.5 mil)

11.2.1 Mechanical Dimensions of the PC755 PBGA

Figure 11-3 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 PBGA package.

Figure 11-3. Mechanical Dimensions and Bottom Surface Nomenclature of the PC755 PBGA



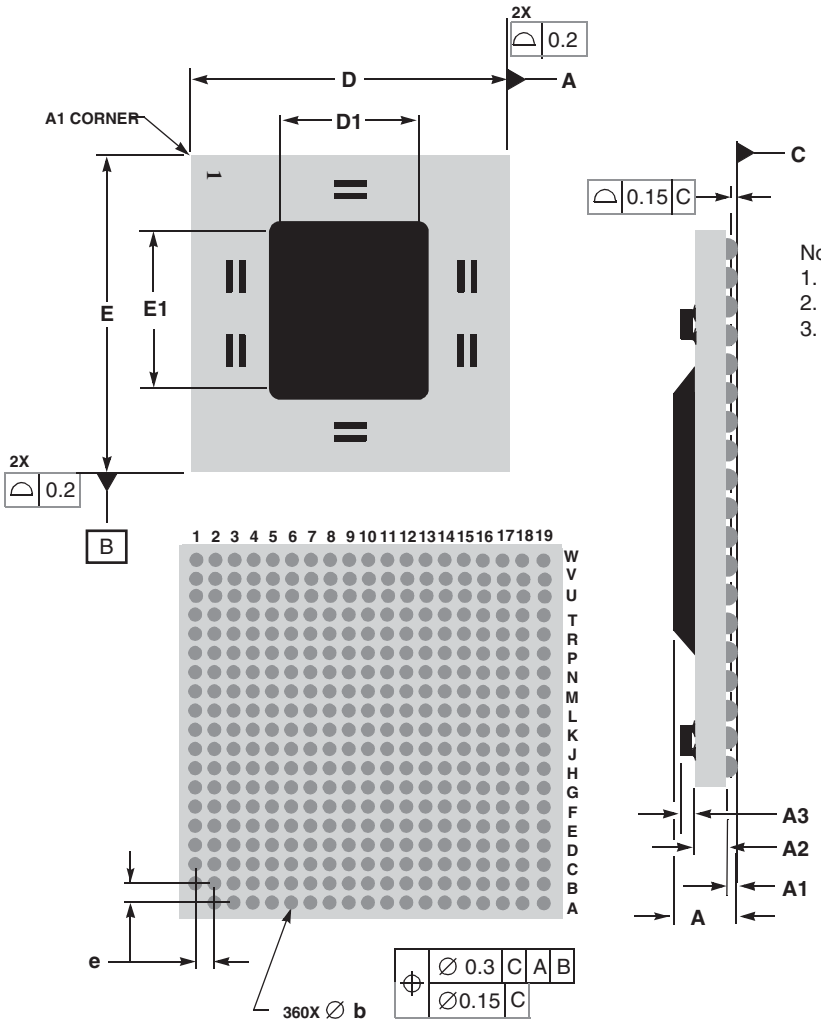
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.3 Mechanical Dimensions of the PC755 HiTCE Package

Figure 11-5 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 HiTCE package.

Figure 11-5. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (HiTCE)



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.24
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

13. Definitions

13.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnity Atmel for any damages resulting from such improper use or sale.

13.2 Differences with Commercial Part

	Commercial part	Military part
Temperature range	T_J = 0 to 105° C	T_J = -55°C to 125°C

14. Document Revision History

Table 14-1 provides a revision history for this hardware specification.

Table 14-1. Revision History

Revision Number	Date	Substantive Change(s)
2138G	04/2006	Increased power specification for 350 MHz full-power mode in Table 7-1 on page 23. Updated ordering information to new Template.
2138F	05/2005	Added HiTCE package for PowerPC 745 Removed phrase "for the ceramic ball grid array (CBGA) package" from Section 6.1.3 on page 19; this information applies to devices in all packages Figure 8-14 on page 36: updated COP Connector Diagram to recommend a weak pull-up resistor on TCK
2138E	10/2004	Product specification release subsequent to product qualification Motorola changed to Freescale
2138D	06/2003	Preliminary β-site