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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	360-BBGA Exposed Pad
Supplier Device Package	360-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx755bvzfu350le

  - Copyback or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode.
  - 64 bytes (256K/512K) or 128 bytes (1M) sectored line size
  - Supports flow through (register-buffer) synchronous burst SRAMs, pipelined (register-register) synchronous burst SRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late-write synchronous burst SRAMs
  - L2 configurable to direct mapped SRAM interface or split cache/direct mapped or private memory
  - Core-to-L2 frequency divisors of 1, 1.5, 2, 2.5, and 3 supported
  - 64-bit data bus
  - Selectable interface voltages of 2.5V and 3.3V
  - Parity checking on both L2 address and data
- Memory Management Unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - 8 instruction BATs and 8 data BATs
  - 8 SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus Interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5V and 3.3V.
  - Parity checking on both address and data busses
- Power Management
  - Low-power design with thermal requirements very similar to PC740/750.
  - Selectable interface voltage of 1.8V/2.0V can reduce power in output buffers (compared to 3.3V)
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
- Integrated Thermal Management Assist Unit
  - One-ship thermal sensor and control logic
  - Thermal Management Interrupt for software regulation of junction temperature

Table 2-2 provides the pinout listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8]

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	–	–
$\overline{\text{AACK}}$	N3	Low	Input	–	–
$\overline{\text{ABB}}$	L7	Low	I/O	–	–
AP[0-3]	C4, C5, C6, C7	High	I/O	–	–
$\overline{\text{ARTRY}}$	L6	Low	I/O	–	–
AVDD	A8	-	-	2V	2V
$\overline{\text{BG}}$	H1	Low	Input	–	–
$\overline{\text{BR}}$	E7	Low	Output	–	–
BVSEL[3][5][6]	W1	High	Input	GND	3.3V
$\overline{\text{CI}}$	C2	Low	Output	–	–
CKSTP_IN	B8	Low	Input	–	–
CKSTP_OUT	D7	Low	Output	–	–
CLK_OUT	E3	–	Output	–	–
$\overline{\text{DBB}}$	K5	Low	I/O	–	–
$\overline{\text{DBDIS}}$	G1	Low	Input	–	–
$\overline{\text{DBG}}$	K1	Low	Input	–	–
$\overline{\text{DBWO}}$	D1	Low	Input	–	–
DH[0-31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	–	–
DL[0-31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	–	–
DP[0-7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	–	–
$\overline{\text{DRTRY}}$	H6	Low	Input	–	–
$\overline{\text{GBL}}$	B1	Low	I/O	–	–
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	–	–	GND	GND
$\overline{\text{HRESET}}$	B6	Low	Input	–	–
$\overline{\text{INT}}$	C11	Low	Input	–	–
L1_TSTCLK[2]	F8	High	Input	–	–
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	–	–

4. Detailed Specifications

This specification describes the specific requirements for the microprocessor PC755, in compliance with Atmel Grenoble standard screening.

5. Applicable Documents

1) MIL-STD-883: Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

Depending on the package, the terminal connections is shown in Table 2-1 on page 8, Table 2-2 on page 10 and Figure 3-1 on page 13.

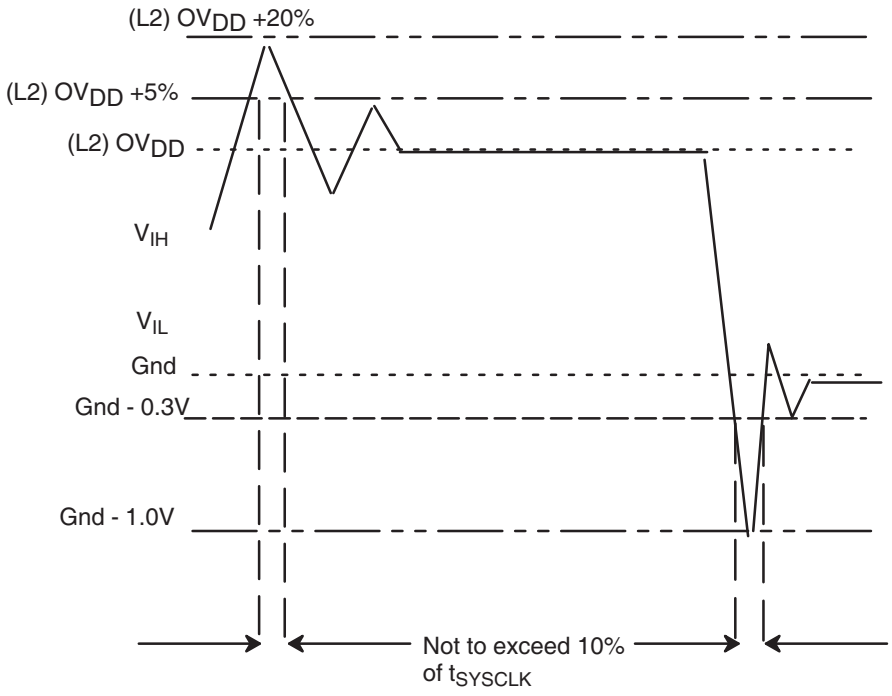
5.1.2 Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage[4]		V_{DD}	-0.3 to 2.5	V
PLL supply voltage[4]		AV_{DD}	-0.3 to 2.5	V
L2 DLL supply voltage[4]		$L2AV_{DD}$	-0.3 to 2.5	V
Processor bus supply voltage[3]		OV_{DD}	-0.3 to 3.6	V
L2 bus supply voltage[3]		$L2OV_{DD}$	-0.3 to 3.6	V
Input voltage	Processor bus[2][5]	V_{IN}	-0.3 to OV_{DD} + 0.3V	V
	L2 Bus[2][5]	V_{IN}	-0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{IN}	-0.3 to 3.6	V
Storage temperature range		T_{STG}	-55/+150	°C

Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions[1]" on page 16. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3V for up to 20 ms, or by 2.5V for up to 40 ms. Excursions beyond 3.3V or 40 ms are not supported.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0V for up to 20 ms, or by 0.7V for up to 40 ms. Excursions beyond 1.0V or 40 ms are not supported.
5. This is a DC specifications only. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5-1 on page 15.

Figure 5-1 shows the allowable undershoot and overshoot voltage on the PC755 and PC745.

Figure 5-1. Overshoot/Undershoot Voltage



The PC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC755 core voltage must always be provided at nominal 2.0V (see "Recommended Operating Conditions(1)" on page 16 for actual recommended core voltage). Voltage to the L2 I/Os and Processor Interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 5-1. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 5-1 describes the input threshold voltage setting.

Table 5-1. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5V/3.3V	1	2.5V/3.3V

Notes: 1. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, contact your local Atmel sales office.

5.1.3 Recommended Operating Conditions[1]

Characteristic		Symbol	Recommended Value				Unit
			300 MHz, 350 MHz		400 MHz		
			Min	Max	Min	Max	
Core supply voltage[3]		V_{DD}	1.80	2.10	1.90	2.10	V
PLL supply voltage[3]		AV_{DD}	1.80	2.10	1.90	2.10	V
L2 DLL supply voltage[3]		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V
Processor bus supply voltage[2][4][5]	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V
			3.135	3.465	3.135	3.465	V
L2 bus supply voltage[2][4][5]	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V
			3.135	3.465	3.135	3.465	V
Input voltage	Processor bus	V_{IN}	GND	OV_{DD}	GND	OV_{DD}	V
	L2 Bus	V_{IN}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V
	JTAG Signals	V_{IN}	GND	OV_{DD}	GND	OV_{DD}	V
Die-junction temperature	Military temperature range	T_J	-55	125	-55	125	°C
	Industrial temperature	T_J	-40	110	-40	110	°C

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support.
3. 2.0V nominal.
4. 2.5V nominal.
5. 3.3V nominal.

Table 6-3. Package Thermal Characteristics for CI-CGA

Characteristic	Symbol	Value	Unit
		PC755 CI-CGA	
Junction to board thermal resistance	$R\theta_{JB}$	8.42	°C/W

The board designer can choose between several types of heat sinks to place on the PC755. There are several commercially-available heat sinks for the PC755 provided by the following vendors.

For the exposed-die packaging technology, shown in "Recommended Operating Conditions(1)" on page 16, the intrinsic conduction thermal resistance paths are as follows:

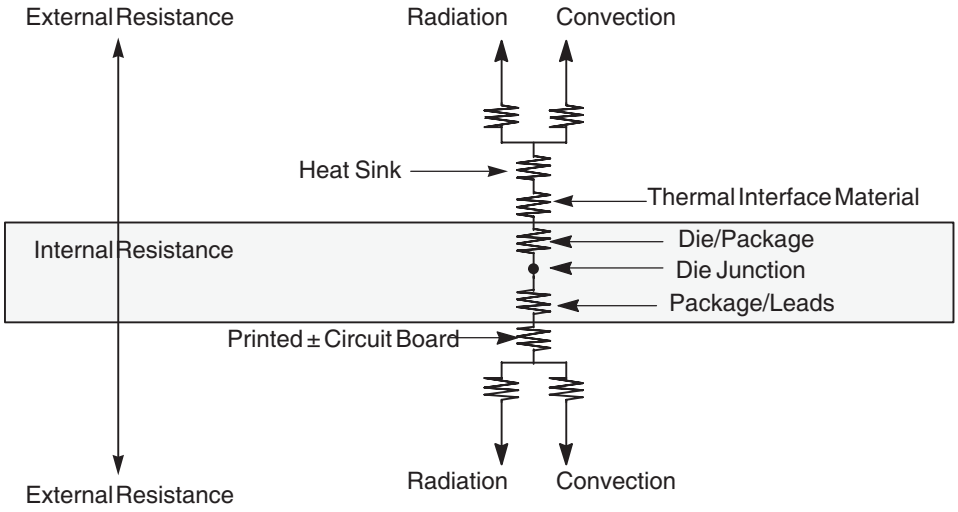
- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 6-1 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Figure 6-1. C4 Package with Head Sink Mounted to a Printed-circuit Board



Note the internal versus external package resistance.

6.1.2 Thermal Management Assistance

The PC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 6-4. More information on the use of this feature is given in the Freescale PC755 RISC Microprocessor User's manual.

Table 6-4. Thermal Sensor Specifications at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 16)

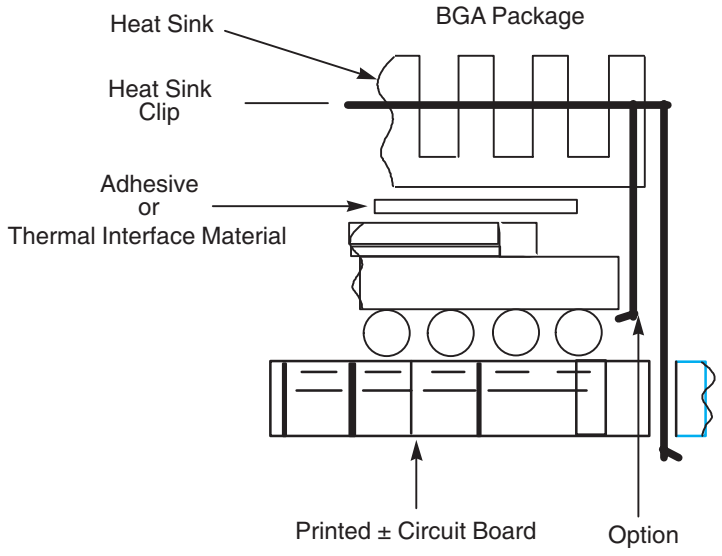
Characteristic	Min	Max	Unit
Temperature range(1)	0	127	°C
Comparator settling time(2)(3)	20	–	s
Resolution(3)	4	–	°C
Accuracy(3)	-12	+12	°C

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, "Programming the Thermal Assist Unit in the PC750 Microprocessor".
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

6.1.3 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design-the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 6-2. This spring force should not exceed 5.5 pounds of force.

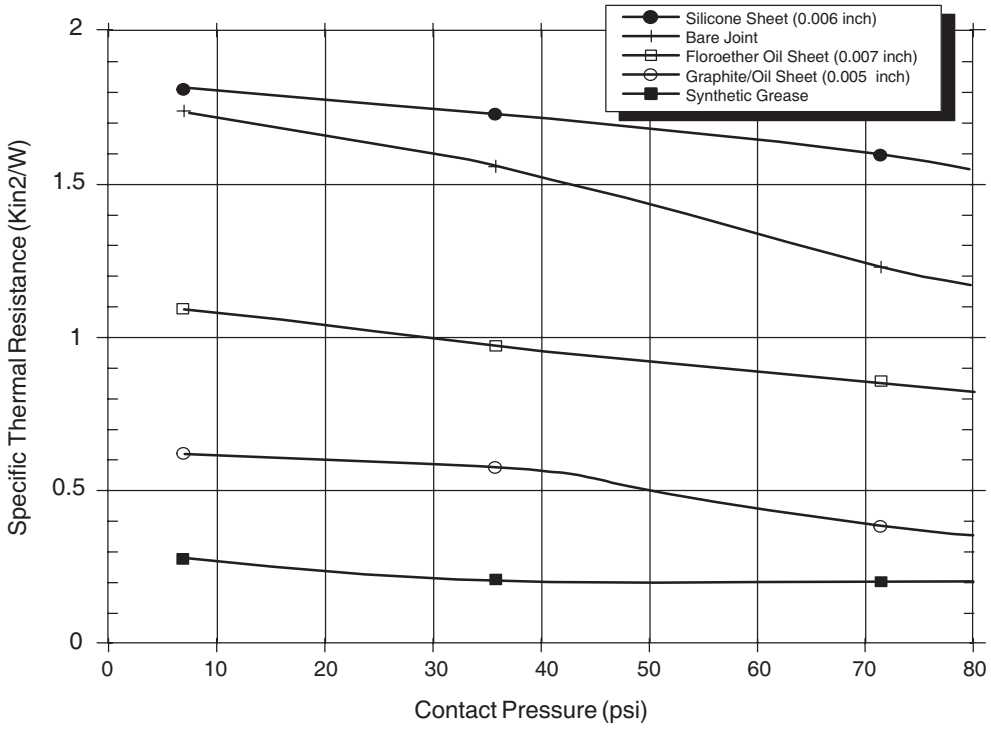
Figure 6-2. Package Exploded Cross-Sectional View with Several Heat Sink Options



Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6.1.4 Adhesives and Thermal Interface Materials

Figure 6-3. Thermal Performance of Select Thermal Interface Material



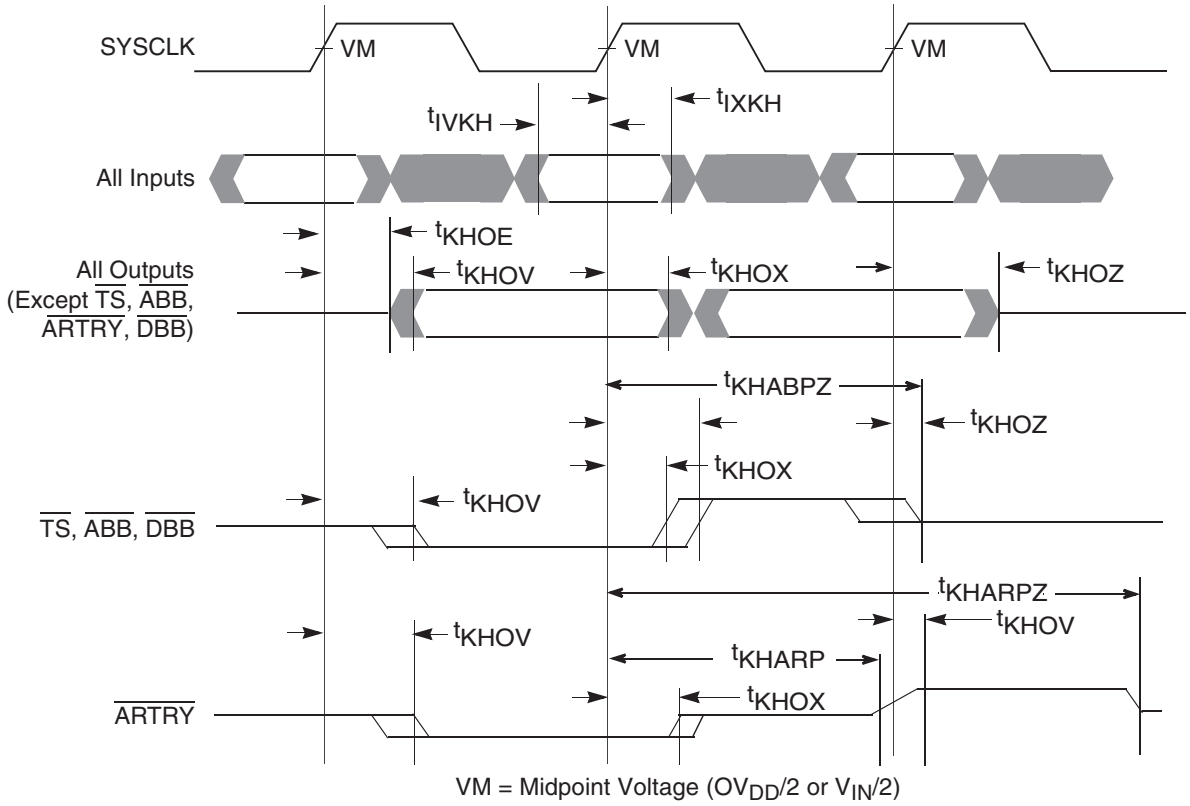
A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-3 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 6-2 on page 19). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

Figure 8-4 provides the input/output timing diagram for the PC755.

Figure 8-4. Input/Output Timing Diagram



8.2.1.2 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 8-5 on page 29 for example core and L2 frequencies at various divisors. Table 8-5 provides the potential range of L2CLK output AC timing specifications as defined in Figure 8-5 on page 30.

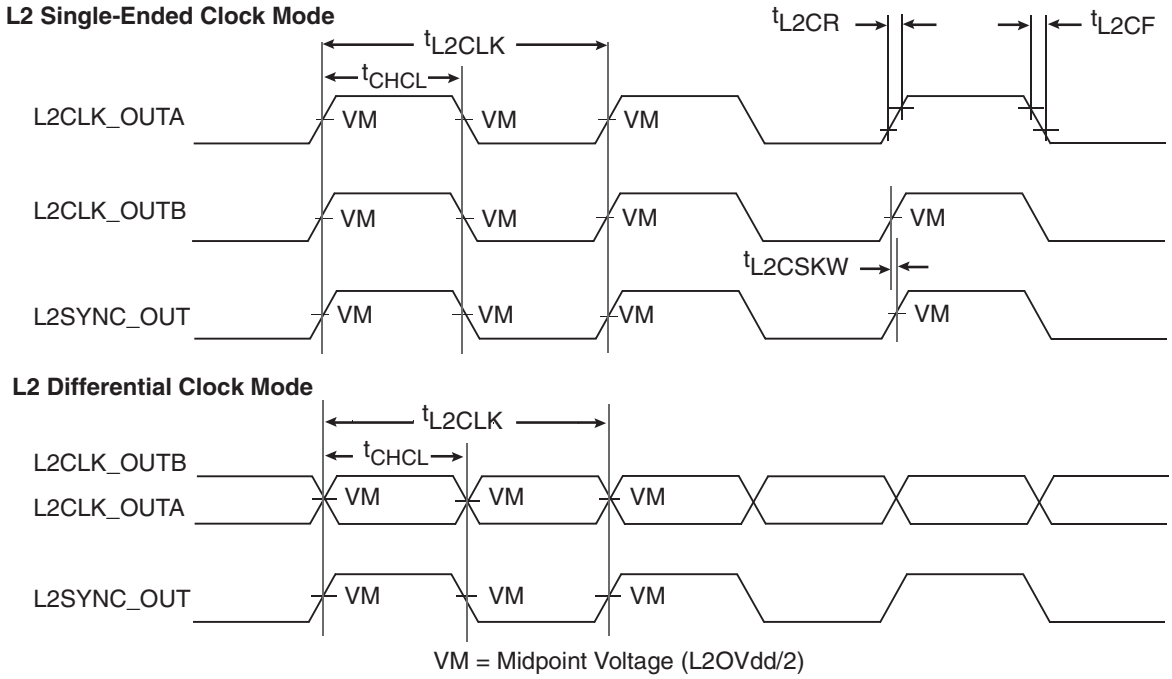
The minimum L2CLK frequency of Table 8-5 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 8-5 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC755 will be a function of the AC timings of the PC755, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 8-5. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

The L2CLK_OUT timing diagram is shown in Figure 8-5.

Figure 8-5. L2CLK_OUT Output Timing Diagram



8.2.1.3 L2 Bus Input AC Specifications

Table 8-6 provides the L2 bus interface AC timing specifications for the PC755 as defined in Figure 8-6 on page 32 and Figure 8-7 on page 32 for the loading conditions described in Figure 8-8 on page 32.

Table 8-6. L2 Bus Interface AC Timing Specifications at Recommended Operating Conditions

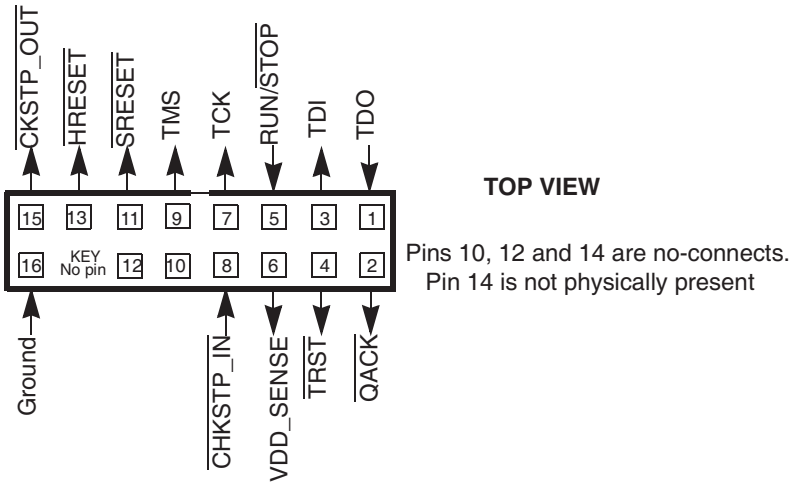
Parameter	Symbol	All Speed Grades		Unit
		Min	Max	
L2SYNC_IN rise and Fall Time(1)	t_{L2CR} & t_{L2CF}	–	1.0	ns
Setup Times: Data and Parity(2)	t_{DVL2CH}	1.2	-	ns
Input Hold Times: Data and Parity(2)	t_{DXL2CH}	0	-	ns
Valid Times: (3)(4)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOV}	-	3.1	ns
All Outputs when L2CR[14-15] = 01		-	3.2	
All Outputs when L2CR[14-15] = 10		-	3.3	
All Outputs when L2CR[14-15] = 11		-	3.7	
Output Hold Times: (3)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOX}	0.5	-	ns
All Outputs when L2CR[14-15] = 01		0.7	-	
All Outputs when L2CR[14-15] = 10		0.9	-	
All Outputs when L2CR[14-15] = 11		1.1	-	
L2SYNC_IN to High Impedance:(3)(5)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOZ}	-	2.4	ns
All Outputs when L2CR[14-15] = 01		-	2.6	
All Outputs when L2CR[14-15] = 10		-	2.8	
All Outputs when L2CR[14-15] = 11		-	3.0	

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 6-3 on page 20). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 8-1 on page 25).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14-15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14-15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev 2.8 (Rev E) were limited in performance.and did not conform to this specification. Contact your local Atmel sales office for more information.

The COP interface has a standard header for connection to the target system, based on the 0.025” square-post 0.100” centered header assembly (often called a “Berg” header). The connector typically has pin 14 removed as a connector key.

Figure 8-15 shows the COP connector diagram.

Figure 8-15. COP Connector Diagram



There is no standardized way to number the COP header shown in Figure 8-15; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin one (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 8-15 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Table 8-7 on page 32 is usually hooked up to the PCI bridge chip in a system and is an input to the PC755 informing it that it can go into the quiescent state. Under normal operation this occurs during a low power mode selection. In order for COP to work the PC755 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. To preserve correct power down operation, $\overline{\text{QACK}}$ should be merged so that it also can be driven by the PCI bridge.

9. Preparation for Delivery

9.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

9.2 Certificate of Compliance

Atmel offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-PRF-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

9.3 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

1. Devices should be handled on benches with conductive and grounded surfaces
2. Ground test equipment, tools and operator
3. Do not handle devices by the leads
4. Store devices in conductive foam or carriers
5. Avoid use of plastic, rubber, or silk in MOS areas
6. Maintain relative humidity above 50 percent if practical
7. For CI-CGA packages, use specific tray to take care of the highest height of the package compared with the normal CBGA

9.4 Clock Relationship Choices

The PC755's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755 is shown in Figure 10-2 on page 41 for example frequencies.

Table 9-1. PC755 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	**Core-to VCO Multiplier**	**Bus 33 MHz**	**Bus 50 MHz**	**Bus 66 MHz**	**Bus 75 MHz**	**Bus 80 MHz**	**Bus 100 MHz**
0100	2x	2x	-	-	-	-	-	200 (400)
1000	3x	2x	-	-	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	-	-	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	-	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	-	225 (450)	300 (600)	338 (675)	360 (720)	-
1011	5x	2x	-	250 (500)	333 (666)	375 (750)	400 (800)	-
1001	5.5x	2x	-	275 (550)	366 5733°	-	-	-
1101	6x	2x	200 (400)	300 (600)	400 (800)	-	-	-
0101	6.5x	2x	216 (433)	325 (650)	-	-	-	-
0010	7x	2x	233 (466)	350 (700)	-	-	-	-
0001	7.5x	2x	250 (500)	375 (750)	-	-	-	-
1100	8x	2x	266 (533)	400 (800)	-	-	-	-
0110	10x	2x	333 (666)	-	-	-	-	-
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755; see "Clock AC Specifications" on page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the PC755 regardless of the SYSCLK input.

The PC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the PC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the PC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC755 core, and the phase adjustment range that the L2 DLL supports. Figure 8-9 on page 33 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 9-2. Sample Core-to-L2 Frequencies

Core Frequency in MHz	1	1.5	2	2.5	3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122
375	375	250	188	150	125
400	400	266	200	160	133

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the PC755; see "L2 Clock AC Specifications" on page 28 for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

10.3 Decoupling Recommendations

Due to the PC755's dynamic power management feature, large address and data buses, and high operating frequencies, the PC755 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC755 system, and the PC755 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the PC755. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$ and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV vplanes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors – 100-330 µF (AVX TPS tantalum or Sanyo OSCON).

10.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the PC755.

10.5 Output Buffer DC Impedance

The PC755 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to $(L2)OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $(L2)OV_{DD}/2$ (See Figure 10-4 on page 43).

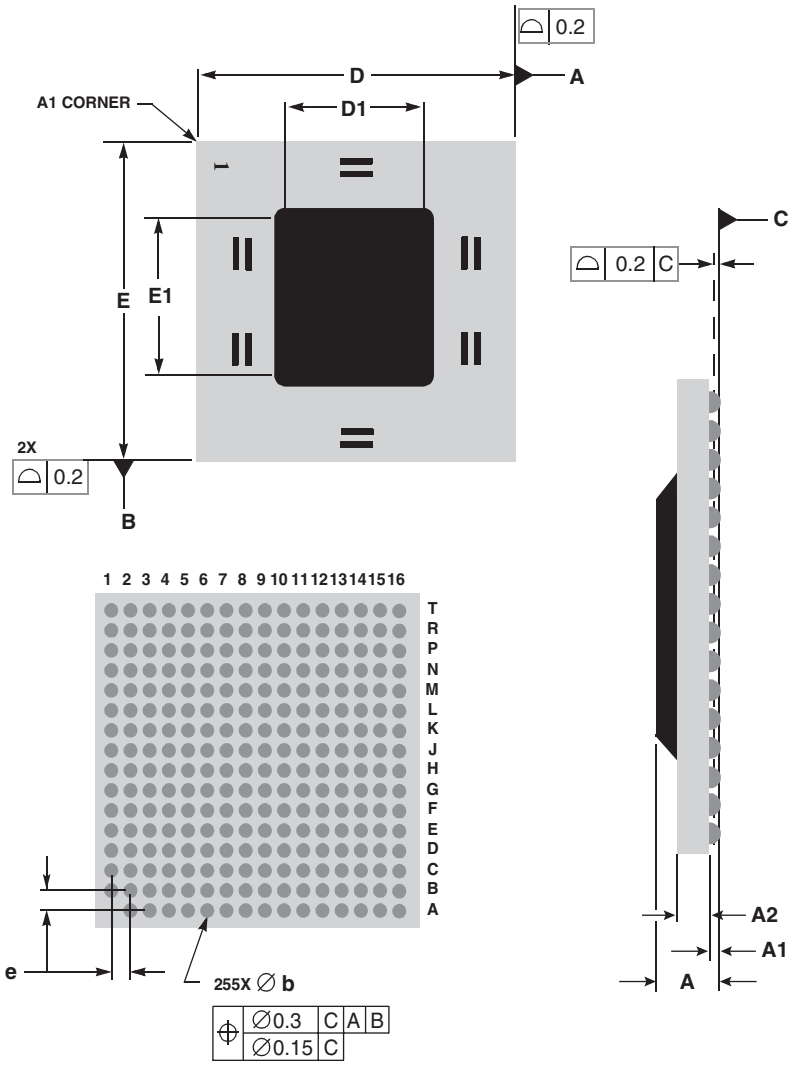
The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices.

NO TAG describes the driver impedance measurement circuit described above.

11.1.1 Mechanical Dimensions of the PC745 HiTCE Package

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature of the PC745, 255 HiTCE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature of the PC745 HiTCE



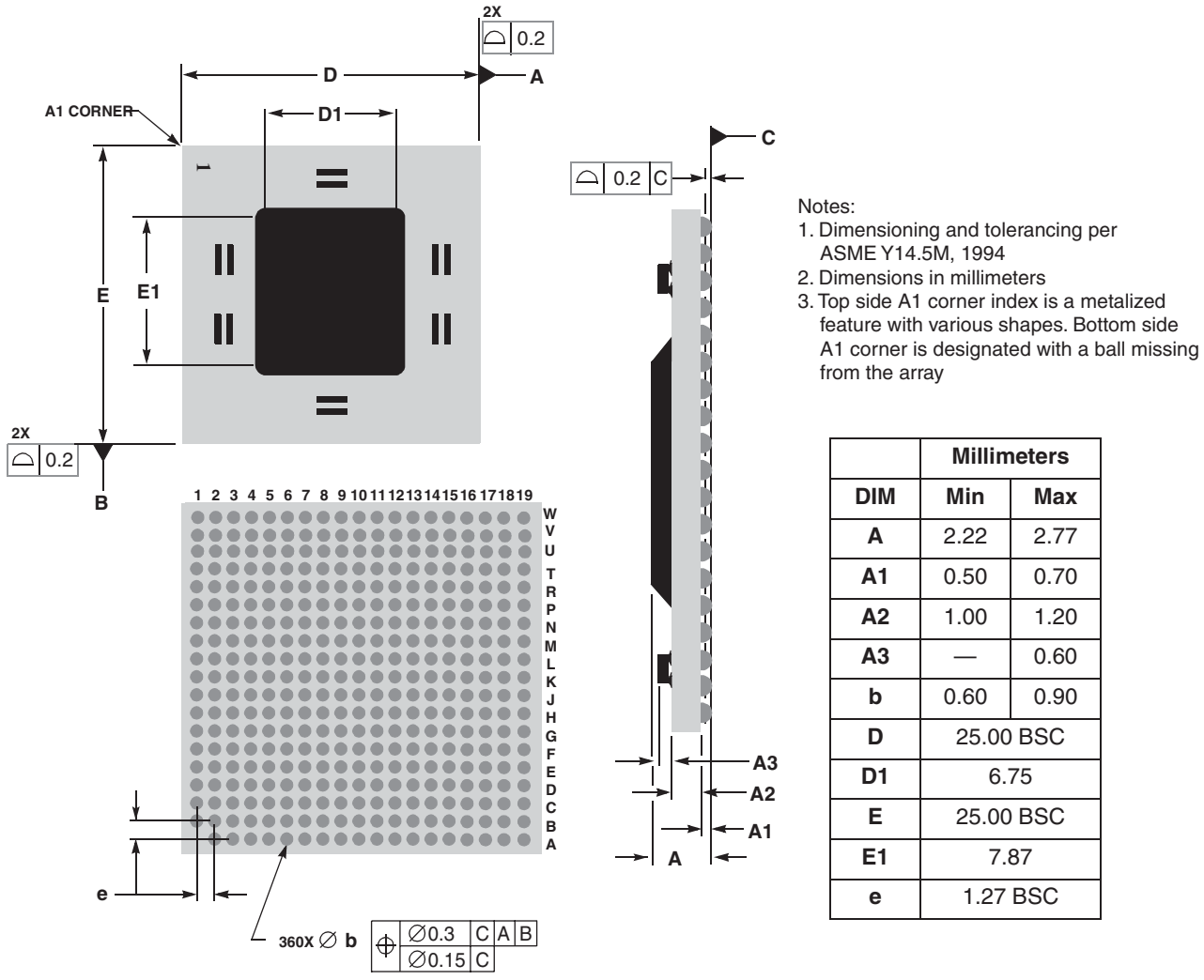
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array
4. Capacitor Pads may be unpopulated

	Millimeters	
Dim	**Min**	**Max**
A	2.42	3.08
A1	0.8	1.0
A2	0.90	1.14
b	0.82	0.93
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.1 Mechanical Dimensions of the PC755 PBGA

Figure 11-3 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 PBGA package.

Figure 11-3. Mechanical Dimensions and Bottom Surface Nomenclature of the PC755 PBGA



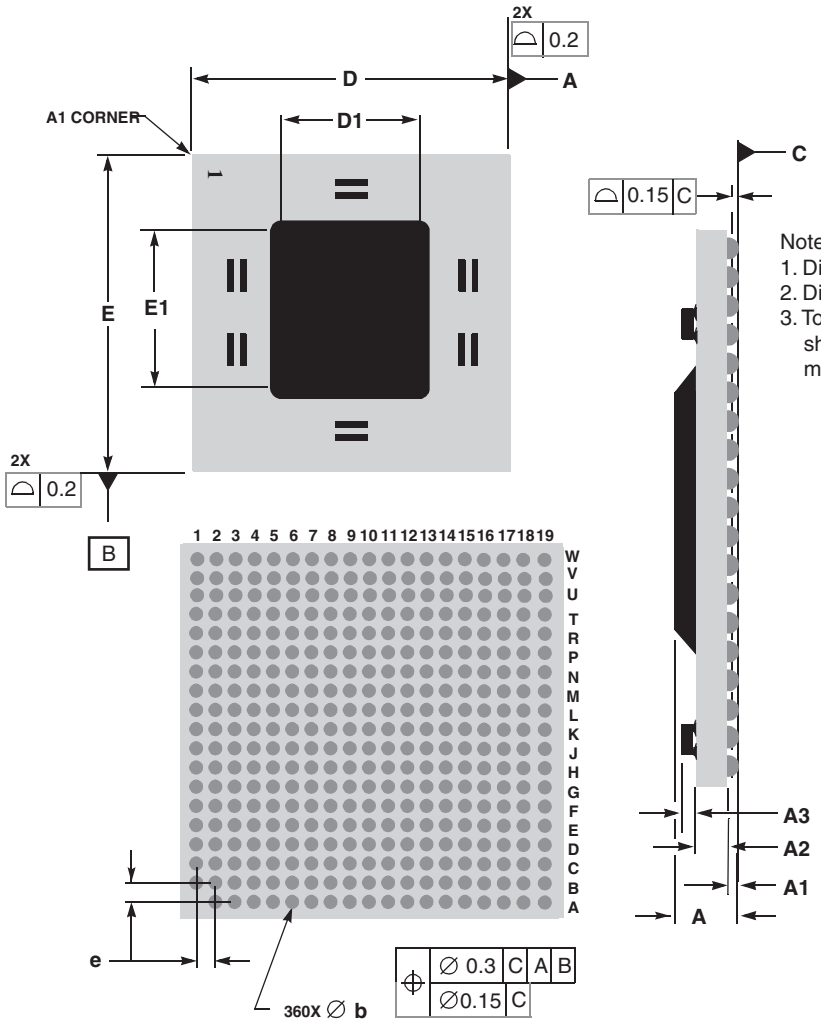
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.2 Mechanical Dimensions of the PC755 CBGA Package

Figure 11-4 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 CBGA package.

Figure 11-4. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (CBGA)



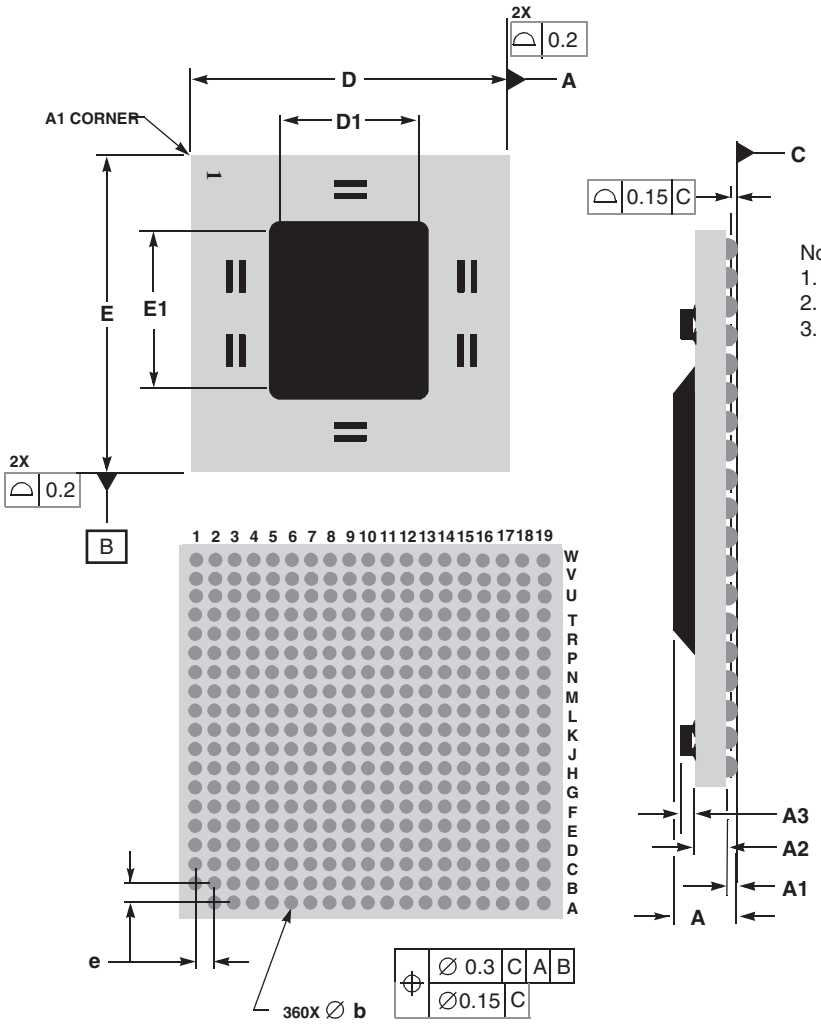
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.20
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.3 Mechanical Dimensions of the PC755 HiTCE Package

Figure 11-5 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 HiTCE package.

Figure 11-5. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (HiTCE)



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.24
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	