Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	360-BBGA Exposed Pad
Supplier Device Package	360-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx755cvzfu400le

1.2 General Parameters

The following list provides a summary of the general parameters of the PC755:

Technology	0.22 µm CMOS, five-layer metal, 1 layer poly
Die size	6.61 mm x 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static Packages
PC745	Surface mount 255 Plastic Ball Grid Array (PBGA) Surface mount 255 Ceramic Ball Grid Array (Hi-TCE)
PC755	Surface mount 360 Plastic Ball Grid Array (PBGA) Surface mount 360 Ceramic Ball Grid Array (CI-CGA, CBGA, HiTCE)
Core power supply	2V ± 100 mV DC (nominal; some parts support core voltages down to 1.8V; see "Recommended Operating Conditions(1)" on page 16
I/O power supply	2.5V ± 100 mV DC or 3.3V ± 165 mV DC (input thresholds are configuration pin selectable)

1.3 Features

This section summarizes features of the PC755's implementation of the PowerPC architecture. Major features of the PC755 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry Branch History Table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 6 entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes

2.1 Pinout Listings

Table 2-1 provides the pinout listing for the PC745, 255 PBGA package.

Table 2-1. Pinout Listing for the PC745, 255 PBGA and HiTCE CBGA Packages

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	–	–
AACK	L2	Low	Input	–	–
ABB	K4	Low	I/O	–	–
AP[0-3]	C1, B4, B3, B2	High	I/O	–	–
ARTRY	J4	Low	I/O	–	–
AVDD	A10	–	–	2V	2V
BG	L1	Low	Input	–	–
BR	B6	Low	Output	–	–
BVSEL[3][4][5]	B1	High	Input	GND	3.3V
CI	E1	Low	Output	–	–
CKSTP_IN	D8	Low	Input	–	–
CKSTP_OUT	A6	Low	Output	–	–
CLK_OUT	D7	–	Output	–	–
DBB	J14	Low	I/O	–	–
DBG	N1	Low	Input	–	–
DBDIS	H15	Low	Input	–	–
DBWO	G4	Low	Input	–	–
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	–	–
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	–	–
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	–	–
DRTRY	G16	Low	Input	–	–
GBL	F1	Low	I/O	–	–
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12				
$\overline{\text{HRESET}}$	A7	Low	Input	–	–
INT	B15	Low	Input	–	–
L1_TSTCLK[2]	D11	High	Input	–	–
L2_TSTCLK[2]	D12	High	Input	–	–
LSSD_MODE[2]	B10	Low	Input	–	––

Table 2-2 provides the pinout listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8]

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	–	–
$\overline{\text{AACK}}$	N3	Low	Input	–	–
$\overline{\text{ABB}}$	L7	Low	I/O	–	–
AP[0-3]	C4, C5, C6, C7	High	I/O	–	–
$\overline{\text{ARTRY}}$	L6	Low	I/O	–	–
AVDD	A8	-	-	2V	2V
$\overline{\text{BG}}$	H1	Low	Input	–	–
$\overline{\text{BR}}$	E7	Low	Output	–	–
BVSEL[3][5][6]	W1	High	Input	GND	3.3V
$\overline{\text{CI}}$	C2	Low	Output	–	–
CKSTP_IN	B8	Low	Input	–	–
CKSTP_OUT	D7	Low	Output	–	–
CLK_OUT	E3	–	Output	–	–
$\overline{\text{DBB}}$	K5	Low	I/O	–	–
$\overline{\text{DBDIS}}$	G1	Low	Input	–	–
$\overline{\text{DBG}}$	K1	Low	Input	–	–
$\overline{\text{DBWO}}$	D1	Low	Input	–	–
DH[0-31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	–	–
DL[0-31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	–	–
DP[0-7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	–	–
$\overline{\text{DRTRY}}$	H6	Low	Input	–	–
$\overline{\text{GBL}}$	B1	Low	I/O	–	–
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	–	–	GND	GND
$\overline{\text{HRESET}}$	B6	Low	Input	–	–
$\overline{\text{INT}}$	C11	Low	Input	–	–
L1_TSTCLK[2]	F8	High	Input	–	–
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	–	–

Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
L2AVDD	L13	–	–	2V	2V
$\overline{\text{L2CE}}$	P17	Low	Output	–	–
L2CLKOUTA	N15	–	Output	–	–
L2CLKOUTB	L16	–	Output	–	–
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	–	–
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	–	–
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	–	–	1.8V/2V	3.3V
L2SYNC_IN	L14	–	Input	–	–
L2SYNC_OUT	M14	–	Output	–	–
L2_TSTCLK[2]	F7	High	Input	–	–
L2VSEL[1][3][5][6]	A19	High	Input	GND	3.3V
$\overline{\text{L2WE}}$	N16	Low	Output	–	–
L2ZZ	G17	High	Output	–	–
$\overline{\text{LSSD\_MODE}}$[2]	F9	Low	Input	–	–
$\overline{\text{MCP}}$	B11	Low	Input	–	–
NC (No-Connect)	B3, B4, B5, W19, K9, K11[4], K19[4]	–	–	–	–
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	–	–	1.8V/2V	3.3V
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input	–	–
$\overline{\text{QACK}}$	B2	Low	Input	–	–
$\overline{\text{QREQ}}$	J3	Low	Output	–	–
$\overline{\text{RSRV}}$	D3	Low	Output	–	–
$\overline{\text{SMI}}$	A12	Low	Input	–	–
$\overline{\text{SRESET}}$	E10	Low	Input	–	–
SYSCLK	H9	–	Input	–	–
$\overline{\text{TA}}$	F1	Low	Input	–	–
TBEN	A2	High	Input	–	–
$\overline{\text{TBST}}$	A11	Low	I/O	–	–
TCK	B10	High	Input	–	–
TDI[6]	B7	High	Input	–	–
TDO	D9	High	Output	–	–

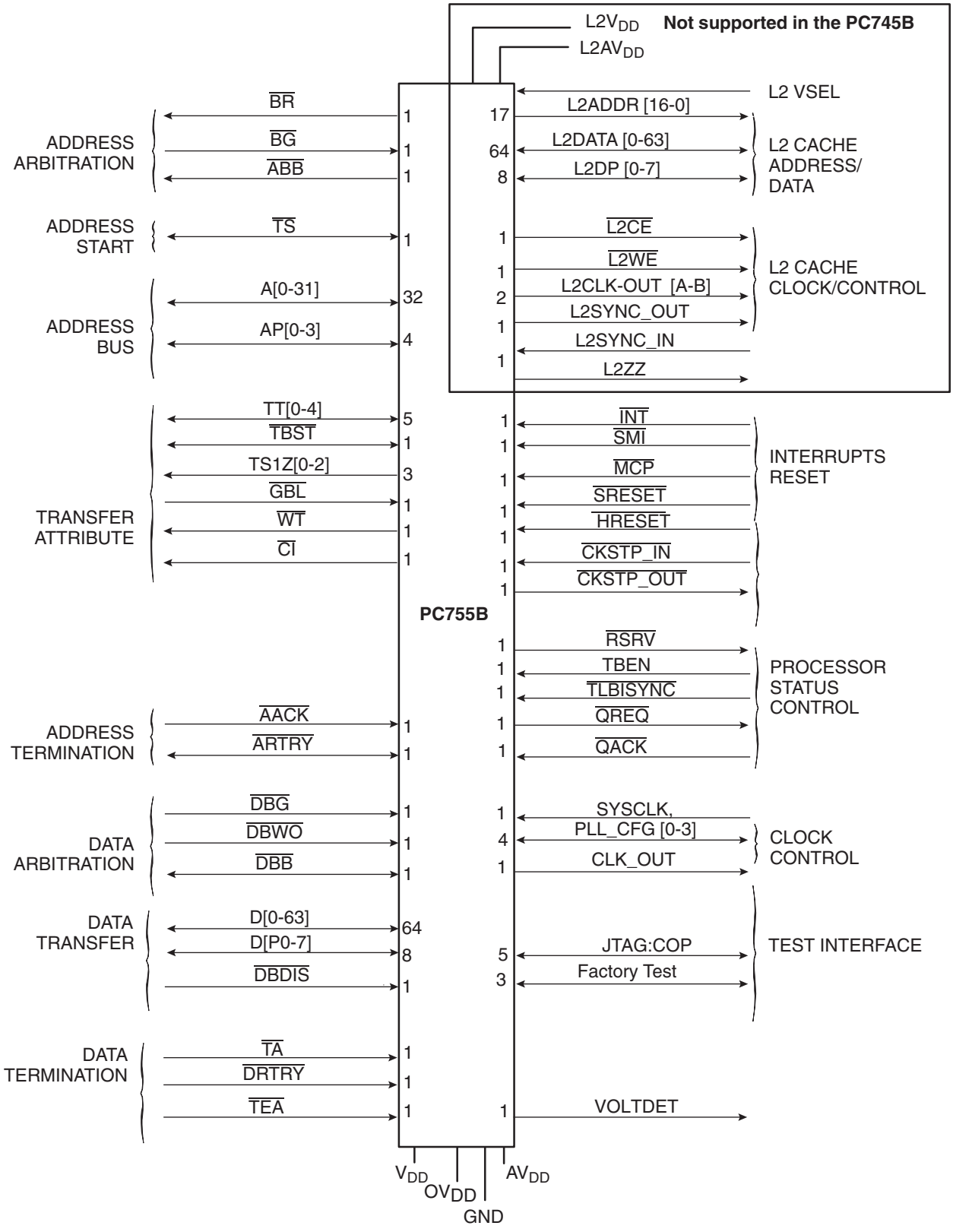
Table 2-2. Pinout Listing for the PC755, 360 PBGA, CBGA, HiTCE CBGA and CI-CGA Packages[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
$\overline{\text{TEA}}$	J1	Low	Input	–	–
$\overline{\text{TLBISYNC}}$	A3	Low	Input	–	–
TMS[6]	C8	High	Input	–	–
$\overline{\text{TRST}}$[6]	A10	Low	Input	–	–
$\overline{\text{TS}}$	K7	Low	I/O	–	–
TSIZ[0-2]	A9, B9, C9	High	Output	–	–
TT[0-4]	C10, D11, B12, C12, F11	High	I/O	–	–
$\overline{\text{WT}}$	C3	Low	Output	–	–
VDD	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	–	–	2V	2V
VOLTDET[7]	K13	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0-16], L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 5-1 on page 15 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see "Recommended Operating Conditions[1]" on page 16.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of 9 existing no-connects in PC750's 360-BGA package.
6. Internal pull up on die.
7. Internally tied to $L2OV_{DD}$ in the PC755 360-BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.
8. This is different from the PC745 255-BGA package.

3. Signal Description

Figure 3-1. PC755 Microprocessor Signal Groups



4. Detailed Specifications

This specification describes the specific requirements for the microprocessor PC755, in compliance with Atmel Grenoble standard screening.

5. Applicable Documents

1) MIL-STD-883: Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

Depending on the package, the terminal connections is shown in Table 2-1 on page 8, Table 2-2 on page 10 and Figure 3-1 on page 13.

5.1.2 Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage[4]		V_{DD}	-0.3 to 2.5	V
PLL supply voltage[4]		AV_{DD}	-0.3 to 2.5	V
L2 DLL supply voltage[4]		$L2AV_{DD}$	-0.3 to 2.5	V
Processor bus supply voltage[3]		OV_{DD}	-0.3 to 3.6	V
L2 bus supply voltage[3]		$L2OV_{DD}$	-0.3 to 3.6	V
Input voltage	Processor bus[2][5]	V_{IN}	-0.3 to OV_{DD} + 0.3V	V
	L2 Bus[2][5]	V_{IN}	-0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{IN}	-0.3 to 3.6	V
Storage temperature range		T_{STG}	-55/+150	°C

Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions[1]" on page 16. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3V for up to 20 ms, or by 2.5V for up to 40 ms. Excursions beyond 3.3V or 40 ms are not supported.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0V for up to 20 ms, or by 0.7V for up to 40 ms. Excursions beyond 1.0V or 40 ms are not supported.
5. This is a DC specifications only. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5-1 on page 15.

6.1.2 Thermal Management Assistance

The PC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 6-4. More information on the use of this feature is given in the Freescale PC755 RISC Microprocessor User's manual.

Table 6-4. Thermal Sensor Specifications at Recommended Operating Conditions (see "Recommended Operating Conditions(1)" on page 16)

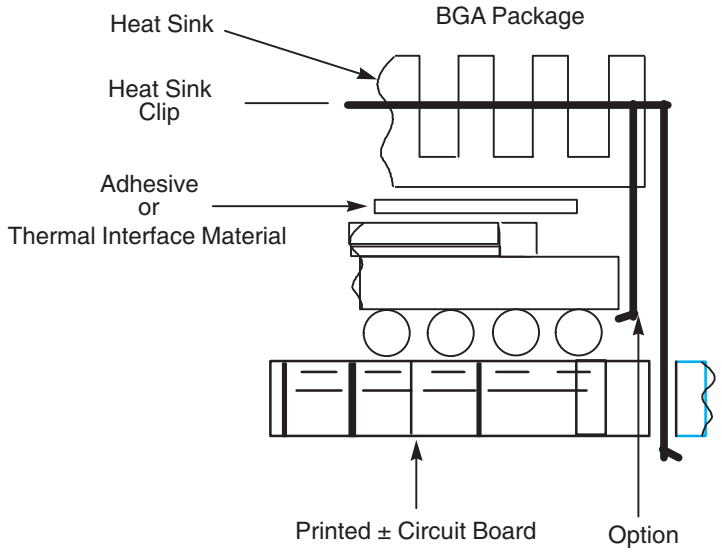
Characteristic	Min	Max	Unit
Temperature range(1)	0	127	°C
Comparator settling time(2)(3)	20	–	s
Resolution(3)	4	–	°C
Accuracy(3)	-12	+12	°C

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, "Programming the Thermal Assist Unit in the PC750 Microprocessor".
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

6.1.3 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design-the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 6-2. This spring force should not exceed 5.5 pounds of force.

Figure 6-2. Package Exploded Cross-Sectional View with Several Heat Sink Options



6.1.5 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

Where:

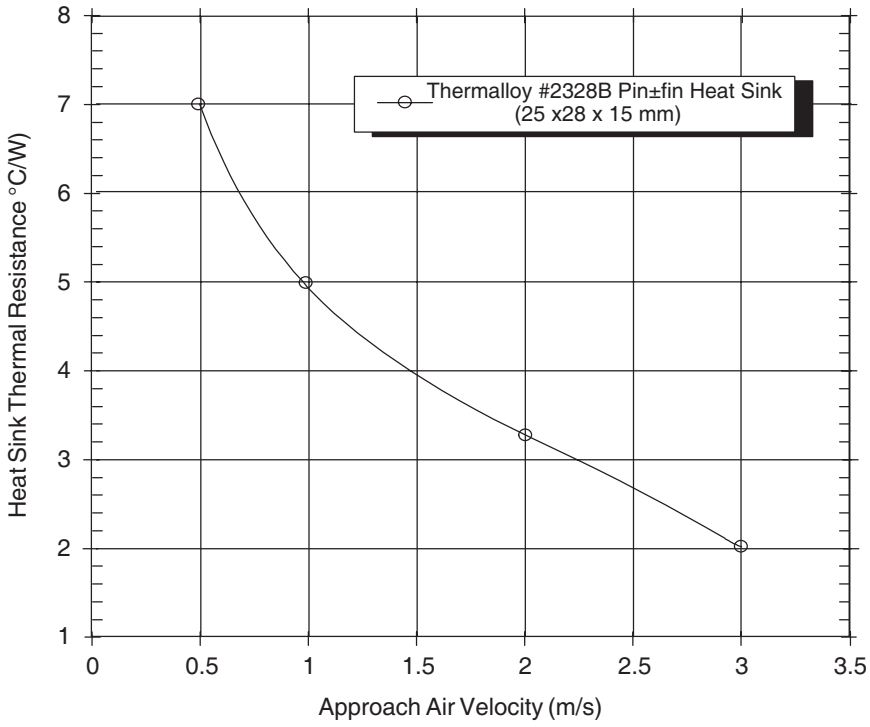
T_J is the die-junction temperature
T_A is the inlet cabinet ambient temperature
T_R is the air temperature rise within the computer cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the adhesive or interface material thermal resistance
θ_{SA} is the heat sink base-to-ambient thermal resistance
P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained less than the value specified in "Recommended Operating Conditions(1)" on page 16. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a $T_{R\ of\ 5}$°C, a CBGA package θ_{JC} = 0.03, and a power consumption (P_D) of 5.0 watts, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 6-4.

Figure 6-4. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity



Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W$

resulting in a die-junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature — airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

7. Power consideration

7.1 Power management

The PC755 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows:

- Full-power: This is the default power state of the PC755. The PC755 is fully powered and the internal functional units operate at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- Doze: All the functional units of the PC755 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the PC755 into the full-power state. The PC755 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC755 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input (MCP). A return to full-power state from a nap state takes only a few processor clock cycles.

Table 8-3. Processor Bus Mode Selection AC Timing Specifications[1]
At V_{DD} = AV_{DD} = 2.0V 100 mV; -55 ≤T_J ≤+125°C, OV_{DD} = 3.3V 165 mV and OV_{DD} = 1.8V ± 100 mV and OV_{DD} = 2.0V 100 mV

Parameter	Symbols[2]	All Speed Grades		Unit
		Min	Max	
Mode select input setup to $\overline{\text{HRESET}}$[3][4][5][6][7]	t_{MVRH}	8	–	t_{SYSCLk}
$\overline{\text{HRESET}}$ to mode select input hold[3][4][6][7][8]	t_{MXRH}	0	–	ns

Notes:
1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (See Figure 8-2). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. THe symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going highs) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs – and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX). For additional explanation of AC timing specifications in Freescale PowerPC microprocessors, see the application note “Understanding AC Timing Specifications for PowerPC Microprocessors.”
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 8-2).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0-3]
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Figure 8-2 provides the mode select input timing diagram for the PC755.

Figure 8-2. Mode Input Timing Diagram

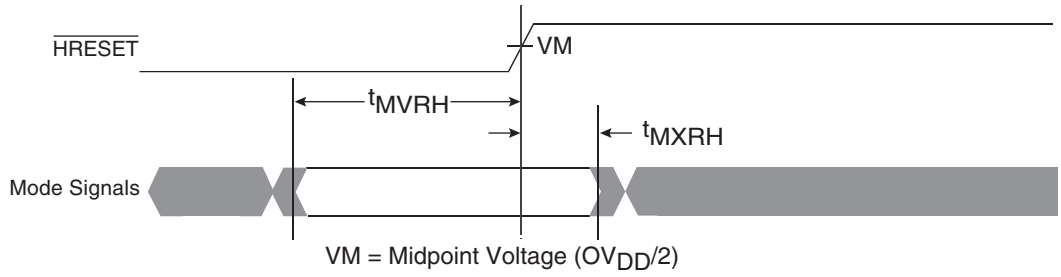


Figure 8-3 provides the AC test load for the PC755.

Figure 8-3. AC Test Load

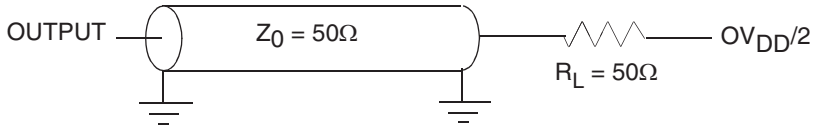


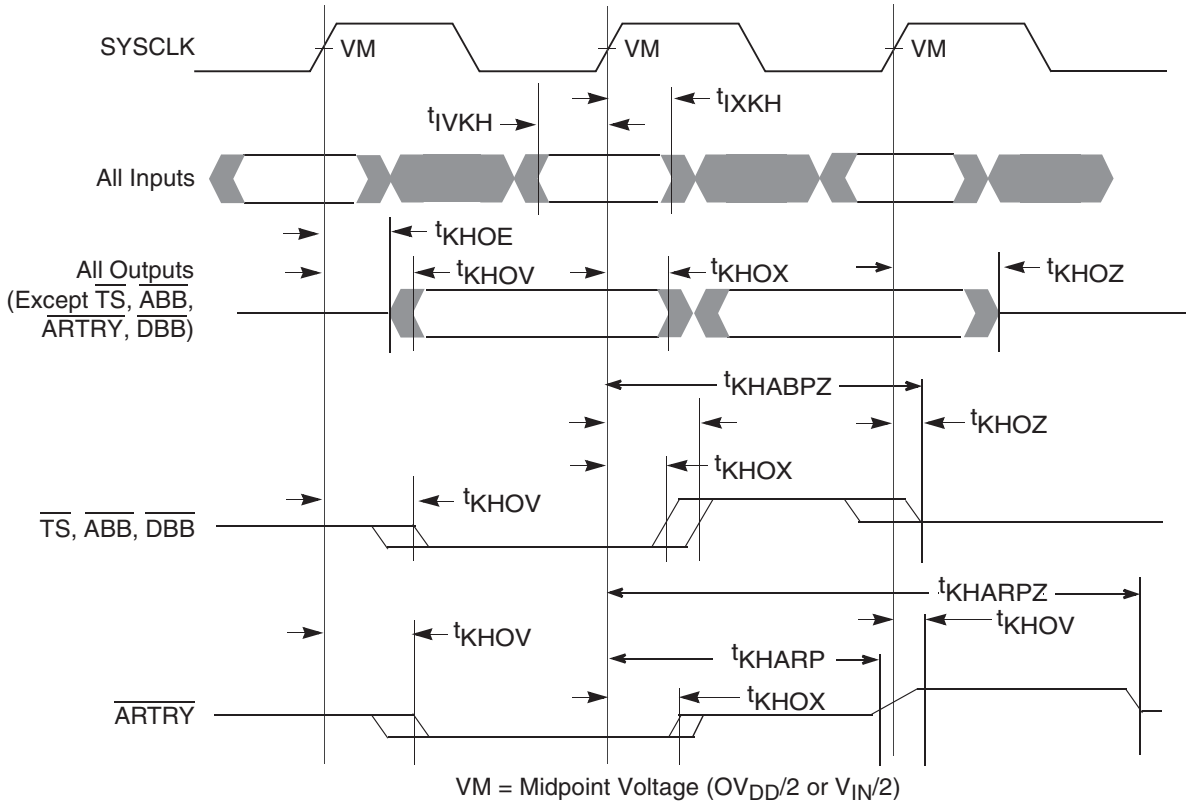
Table 8-4. Processor Bus AC Timing Specifications[1] at Recommended Operating Conditions

Parameter	Symbols	All Speed Grades		Unit
		Min	Max	
Setup Times: All Inputs	t_{IVKH}	2.5	–	ns
Input Hold Times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.6	–	ns
Input Hold Times: All Inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.2	–	ns
Valid Times: All Outputs	t_{KHOV}	–	4.1	ns
Output Hold Times: All Outputs	t_{KHOX}	1	–	ns
SYSCLK to Output Enable[2]	t_{KHOE}	0.5	–	ns
SYSCLK to Output High Impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)[2]	t_{KHOZ}	–	6	ns
SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ High Impedance After Precharge[2][3][4]	t_{KHABPZ}	–	1	t_{SYSCLK}
Maximum Delay to $\overline{\text{ARTRY}}$ Precharge[2][3][5]	t_{KHARP}	–	1	t_{SYSCLK}
SYSCLK to $\overline{\text{ARTRY}}$ High Impedance After Precharge[2][3][5]	t_{KHARPZ}	–	2	t_{SYSCLK}

Notes:
1. Revisions prior to Rev 2.8 (Rev E) were limited in performance and did not conform to this specification. Contact your local Freescale sales office for more information.
2. Guaranteed by design and characterization.
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6-1 on page 18. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 x t_{SYSCLK}, i.e. less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following AACK will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; i.e., it should be high-Z as shown in Figure 6-1 on page 18 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.

Figure 8-4 provides the input/output timing diagram for the PC755.

Figure 8-4. Input/Output Timing Diagram



8.2.1.2 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 8-5 on page 29 for example core and L2 frequencies at various divisors. Table 8-5 provides the potential range of L2CLK output AC timing specifications as defined in Figure 8-5 on page 30.

The minimum L2CLK frequency of Table 8-5 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 8-5 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC755 will be a function of the AC timings of the PC755, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 8-5. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

8.2.1.3 L2 Bus Input AC Specifications

Table 8-6 provides the L2 bus interface AC timing specifications for the PC755 as defined in Figure 8-6 on page 32 and Figure 8-7 on page 32 for the loading conditions described in Figure 8-8 on page 32.

Table 8-6. L2 Bus Interface AC Timing Specifications at Recommended Operating Conditions

Parameter	Symbol	All Speed Grades		Unit
		Min	Max	
L2SYNC_IN rise and Fall Time(1)	t_{L2CR} & t_{L2CF}	–	1.0	ns
Setup Times: Data and Parity(2)	t_{DVL2CH}	1.2	-	ns
Input Hold Times: Data and Parity(2)	t_{DXL2CH}	0	-	ns
Valid Times: (3)(4)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOV}	-	3.1	ns
All Outputs when L2CR[14-15] = 01		-	3.2	
All Outputs when L2CR[14-15] = 10		-	3.3	
All Outputs when L2CR[14-15] = 11		-	3.7	
Output Hold Times: (3)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOX}	0.5	-	ns
All Outputs when L2CR[14-15] = 01		0.7	-	
All Outputs when L2CR[14-15] = 10		0.9	-	
All Outputs when L2CR[14-15] = 11		1.1	-	
L2SYNC_IN to High Impedance:(3)(5)				
All Outputs when L2CR[14-15] = 00	t_{L2CHOZ}	-	2.4	ns
All Outputs when L2CR[14-15] = 01		-	2.6	
All Outputs when L2CR[14-15] = 10		-	2.8	
All Outputs when L2CR[14-15] = 11		-	3.0	

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 6-3 on page 20). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 8-1 on page 25).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14-15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14-15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev 2.8 (Rev E) were limited in performance.and did not conform to this specification. Contact your local Atmel sales office for more information.

Table 10-1 summarizes the signal impedance results. The driver impedance values were characterized at 0°C, 65°C, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 10-1. Impedance Characteristics. V_{DD} = 2.0V, OV_{DD} = 3.3V, T_c = 0 - 105°C

Impedance	Processor bus	L2 bus	Symbol	Unit
RN	25-36	25-36	Z_0	W
RP	26-39	26-39	Z_0	W

10.6 Pull-up Resistor Requirements

The PC755 requires pull-up resistors (1 kΩ – 5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the processor or other bus masters. These pins are $\overline{TS}$, $\overline{ABB}$, $\overline{AACK}$, $\overline{ARTRY}$, $\overline{DBB}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{TEA}$, and $\overline{DBDIS}$. $\overline{DRTRY}$ should also be connected to a pull-up resistor (1 kΩ – 5 kΩ) if it will be used by the system; otherwise, this signal should be connected to $\overline{HRESET}$ to select NO-DRTRY mode.

Three test pins also require pull-up resistors (100Ω – 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ – 5 kΩ) if it is used by the system.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the processor must continually monitor these signals for snooping, this float condition may cause additional power draw by the input receivers on the processor or by other receivers in the system. These signals can be pulled up through weak (10 kΩ) pull-up resistors by the system or may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw, but address bus pull-up resistors are not necessary for proper device operation. The snooped address and transfer attribute inputs are:
A[0:31], AP[0:3], TT[0:4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

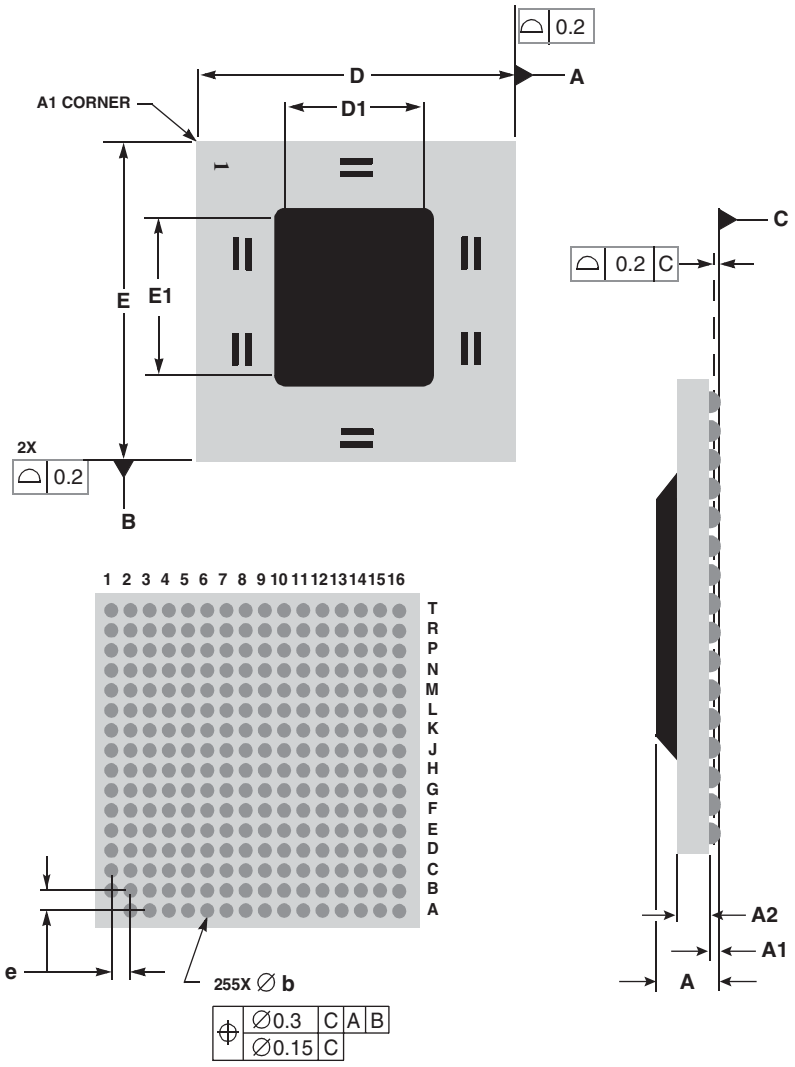
If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

11.1.1 Mechanical Dimensions of the PC745 HiTCE Package

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature of the PC745, 255 HiTCE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature of the PC745 HiTCE



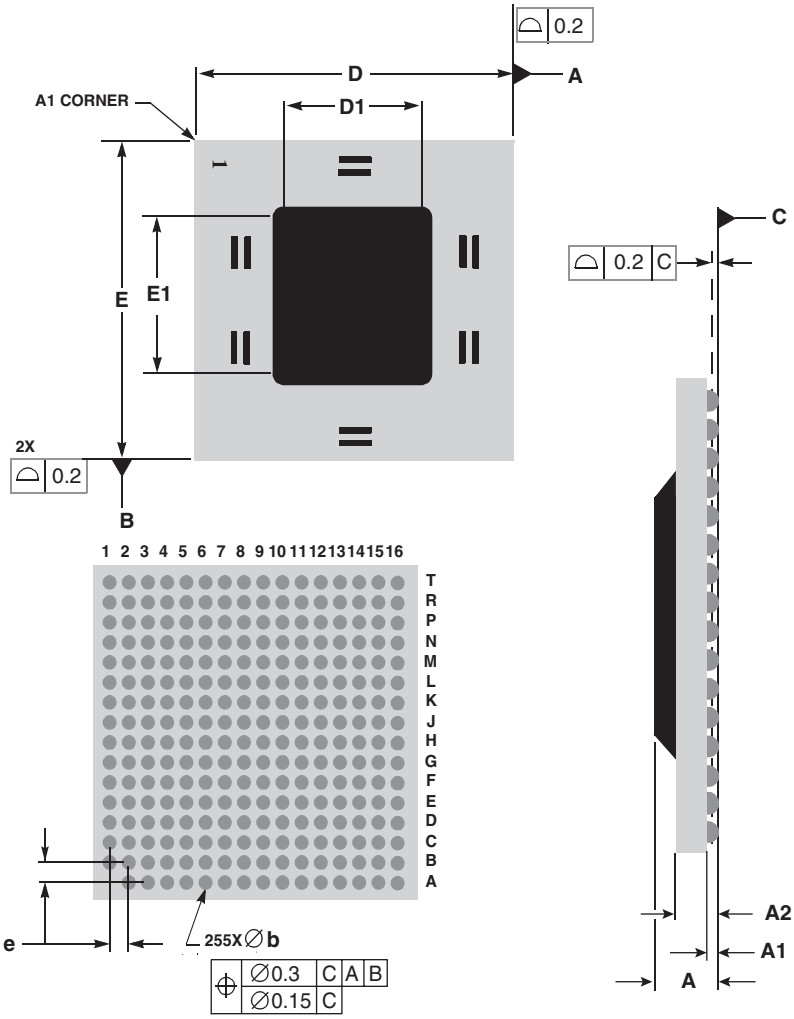
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array
4. Capacitor Pads may be unpopulated

	Millimeters	
Dim	**Min**	**Max**
A	2.42	3.08
A1	0.8	1.0
A2	0.90	1.14
b	0.82	0.93
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

11.1.2 Mechanical Dimensions of the PC745 PBGA Package

Figure 11-2 provides the mechanical dimensions and bottom surface nomenclature of the PC745, 255 PBGA package.

Figure 11-2. Mechanical Dimensions and Bottom Surface Nomenclature of the PC745 PBGA



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array
4. Capacitor Pads may be unpopulated

	Millimeters	
Dim	**Min**	**Max**
A	2.25	2.80
A1	0.50	0.70
A2	1.00	1.20
b	0.60	0.90
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2 Package Parameter for the PC755

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead plastic ball grid array (PBGA).

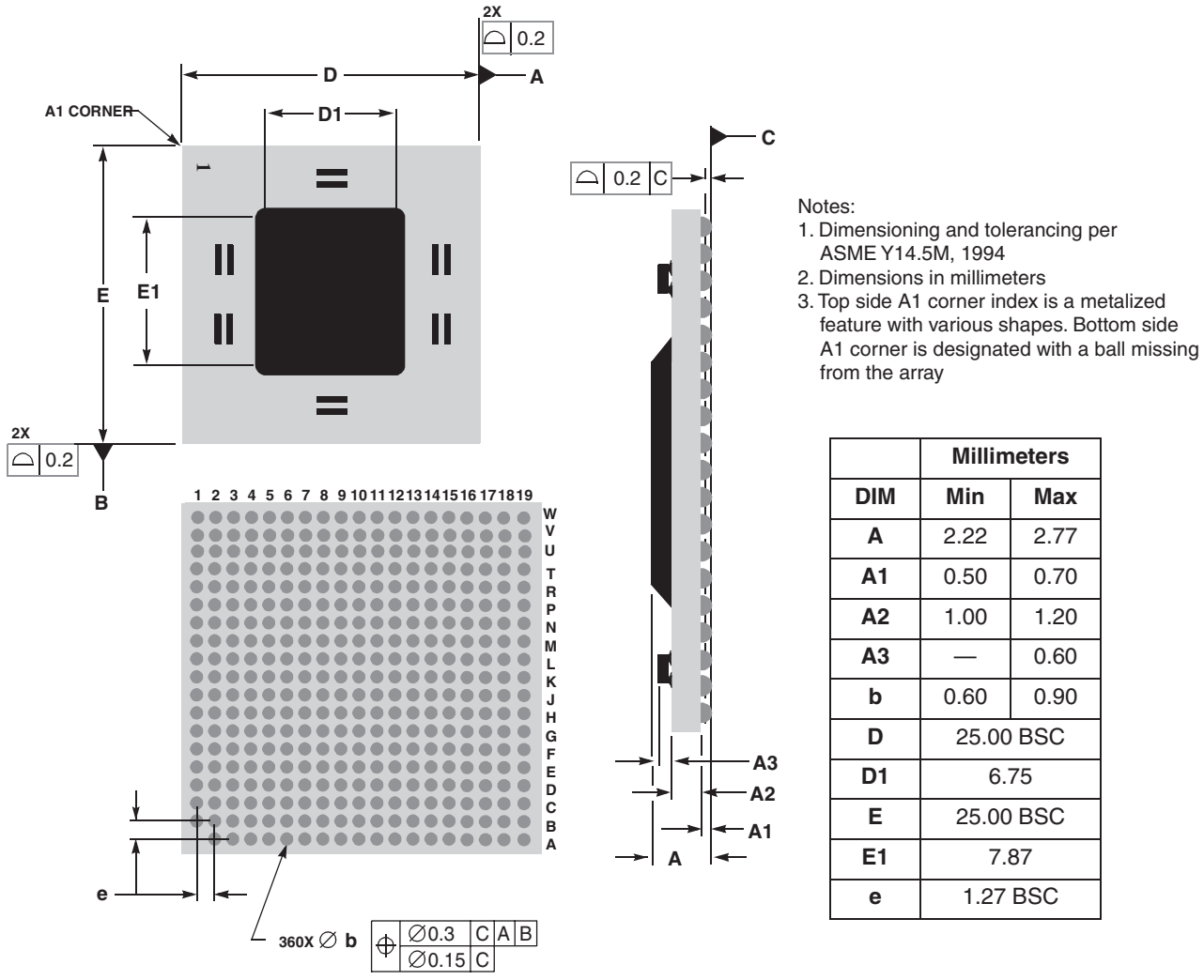
Table 11-2. Package Parameters

Parameter	HiTCE-CBGA	PBGA
Package Outline	25 mm × 25 mm	25 mm × 25 mm
Interconnects	360 (19 x 19 ball array – 1)	360 (19 x 19 ball array – 1
Pitch	1.27 mm (50 mil)	1.27 mm (50 mil)
Minimum module height	2,65 mm	2.22 mm
Maximum module height	3,2 mm	2.77 mm
Ball diameter	0,89 mm (35 mil)	0.75 mm (29.5 mil)

11.2.1 Mechanical Dimensions of the PC755 PBGA

Figure 11-3 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 PBGA package.

Figure 11-3. Mechanical Dimensions and Bottom Surface Nomenclature of the PC755 PBGA



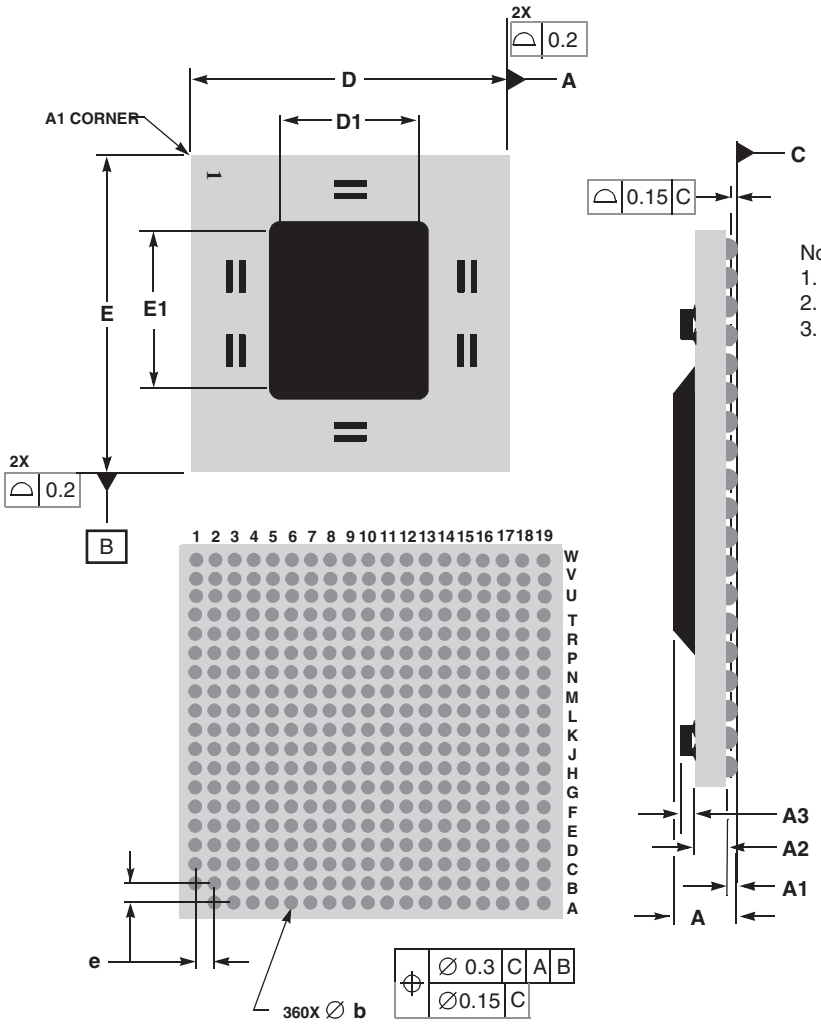
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

11.2.3 Mechanical Dimensions of the PC755 HiTCE Package

Figure 11-5 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 HiTCE package.

Figure 11-5. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (HiTCE)



Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.24
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

13. Definitions

13.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnity Atmel for any damages resulting from such improper use or sale.

13.2 Differences with Commercial Part

	Commercial part	Military part
Temperature range	T_J = 0 to 105° C	T_J = -55°C to 125°C

14. Document Revision History

Table 14-1 provides a revision history for this hardware specification.

Table 14-1. Revision History

Revision Number	Date	Substantive Change(s)
2138G	04/2006	Increased power specification for 350 MHz full-power mode in Table 7-1 on page 23. Updated ordering information to new Template.
2138F	05/2005	Added HiTCE package for PowerPC 745 Removed phrase "for the ceramic ball grid array (CBGA) package" from Section 6.1.3 on page 19; this information applies to devices in all packages Figure 8-14 on page 36: updated COP Connector Diagram to recommend a weak pull-up resistor on TCK
2138E	10/2004	Product specification release subsequent to product qualification Motorola changed to Freescale
2138D	06/2003	Preliminary β-site