Intel - EP4CE10E22C8 Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	645
Number of Logic Elements/Cells	10320
Total RAM Bits	423936
Number of I/O	91
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce10e22c8

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2. Logic Elements and Logic Array Blocks in Cyclone IV Devices

CYIV-51002-1.0

This chapter contains feature definitions for logic elements (LEs) and logic array blocks (LABs). Details are provided on how LEs work, how LABs contain groups of LEs, and how LABs interface with the other blocks in Cyclone[®] IV devices.

Logic Elements

Logic elements (LEs) are the smallest units of logic in the Cyclone IV device architecture. LEs are compact and provide advanced features with efficient logic usage. Each LE has the following features:

- A four-input look-up table (LUT), which can implement any function of four variables
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive the following interconnects:
 - Local
 - Row
 - Column
 - Register chain
 - Direct link
- Register packing support
- Register feedback support



Arithmetic Mode

Arithmetic mode is ideal for implementing adders, counters, accumulators, and comparators. An LE in arithmetic mode implements a 2-bit full adder and basic carry chain (Figure 2–3). LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output. Register feedback and register packing are supported when LEs are used in arithmetic mode.

Figure 2–3 shows LEs in arithmetic mode.





The Quartus II Compiler automatically creates carry chain logic during design processing. You can also manually create the carry chain logic during design entry. Parameterized functions, such as LPM functions, automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 LEs by automatically linking LABs in the same column. For enhanced fitting, a long carry chain runs vertically, which allows fast horizontal connections to M9K memory blocks or embedded multipliers through direct link interconnects. For example, if a design has a long carry chain in an LAB column next to a column of M9K memory blocks, any LE output can feed an adjacent M9K memory block through the direct link interconnect. If the carry chains run horizontally, any LAB which is not next to the column of M9K memory blocks uses other row or column interconnects to drive a M9K memory block. A carry chain continues as far as a full column.

Power-Up Conditions and Memory Initialization

The M9K memory block outputs of Cyclone IV devices power up to zero (cleared) regardless of whether the output registers are used or bypassed. All M9K memory blocks support initialization using a **.mif**. You can create **.mif**s in the Quartus II software and specify their use using the RAM MegaWizard Plug-In Manager when instantiating memory in your design. Even if memory is pre-initialized (for example, using a **.mif**), it still powers up with its outputs cleared. Only the subsequent read after power up outputs the pre-initialized values.

To For more information about **.mif**s, refer to the *RAM Megafunction User Guide* and the *Quartus II Handbook*.

Power Management

The M9K memory block clock enables of Cyclone IV devices allow you to control clocking of each M9K memory block to reduce AC power consumption. Use the rden signal to ensure that read operations only occur when necessary. If your design does not require read-during-write, reduce power consumption by deasserting the rden signal during write operations or any period when there are no memory operations. The Quartus II software automatically powers down any unused M9K memory blocks to save static power.

Document Revision History

Table 3–6 shows the revision history for this chapter.

Table 3-6.	Document	Revision	History
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Date	Version	Changes
November 2011	1.1	Updated the "Byte Enable Support" section.
November 2009	1.0	Initial release.

If you do not use dedicated clock pins to feed the GCLKs, you can use them as general-purpose input pins to feed the logic array. However, when using them as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Constitution For more information about how to connect the clock and PLL pins, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

Clock Control Block

The clock control block drives the GCLKs. Clock control blocks are located on each side of the device, close to the dedicated clock input pins. GCLKs are optimized for minimum clock skew and delay.

Table 5–4 lists the sources that can feed the clock control block, which in turn feeds the GCLKs.

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as synchronous and asynchronous clears, presets, or clock enables onto given GCLKs.
Dual-purpose clock (DPCLK and CDPCLK) I/O input	DPCLK and CDPCLK I/O pins are bidirectional dual function pins that are used for high fan-out control signals, such as protocol signals, TRDY and IRDY signals for PCI, via the GCLK. Clock control blocks that have inputs driven by dual-purpose clock I/O pins are not able to drive PLL inputs.
PLL outputs	PLL counter outputs can drive the GCLK.
Internal logic	You can drive the GCLK through logic array routing to enable internal logic elements (LEs) to drive a high fan-out, low-skew signal path. Clock control blocks that have inputs driven by internal logic are not able to drive PLL inputs.

Table 5-4. Clock Control Block Inputs

In Cyclone IV devices, dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each GCLK. The output from the clock control block in turn feeds the corresponding GCLK. The GCLK can drive the PLL input if the clock control block inputs are outputs of another PLL or dedicated clock input pins. There are five or six clock control blocks on each side of the device periphery—depending on device density; providing up to 30 clock control blocks in each Cyclone IV GX device. The maximum number of clock control blocks per Cyclone IV E device is 20. For the clock control block locations, refer to Figure 5–2 on page 5–12, Figure 5–3 on page 5–13, and Figure 5–4 on page 5–14.

The clock control blocks on the left side of the Cyclone IV GX device do not support any clock inputs.

The control block has two functions:

- Dynamic GCLK clock source selection (not applicable for DPCLK, CDPCLK, and internal logic input)
- GCLK network power down (dynamic enable and disable)



Figure 5–3. Clock Networks and Clock Control Block Locations in EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 Devices ^{(1), (2)}

Notes to Figure 5-3:

- (1) The clock networks and clock control block locations in this figure apply to only the EP4CGX30 device in F484 package and all EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices.
- (2) PLL_1, PLL_2, PLL_3, and PLL_4 are general purpose PLLs while PLL_5, PLL_6, PLL_7, and PLL_8 are multipurpose PLLs.
- (3) There are 6 clock control blocks on the top, right and bottom sides of the device and 12 clock control blocks on the left side of the device.
- (4) REFCLK[0,1]p/n and REFCLK[4,5]p/n can only drive the general purpose PLLs and multipurpose PLLs on the left side of the device. These clock pins do not have access to the clock control blocks and GCLK networks. The REFCLK[4,5]p/n pins are not available in devices in F484 package.
- (5) Not available for EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices in F484 package.
- (6) Dedicated clock pins can feed into this PLL. However, these paths are not fully compensated.

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–5 and Figure 6–6.



Figure 6–5. Cyclone IV Devices HSTL I/O Standard Termination

Figure 6–6. Cyclone IV Devices SSTL I/O Standard Termination



Figure 6–9 shows the overview of Cyclone IV E I/O banks.

Figure 6–9. Cyclone IV E I/O Banks (1), (2)



Notes to Figure 6-9:

- (1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.
- (2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.
- (3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
- (4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.
- (6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 3, 4, 7, and 8.
- (7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses true LVDS input buffer.



Figure 8–26. JTAG Configuration of Multiple Devices Using a Download Cable (1.2, 1.5, and 1.8-V V_{CCIO} Powering the JTAG Pins)

Notes to Figure 8-26:

- (1) Connect these pull-up resistors to the V_{CCI0} supply of the bank in which the pin resides.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.
- (3) In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) Power up the V_{CC} of the ByteBlaster II or USB-Blaster cable with supply from V_{CCI0}. The ByteBlaster II and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the ByteBlaster II Download Cable User Guide and the USB-Blaster Download Cable User Guide.
- (6) Resistor value can vary from 1 k Ω to 10 k Ω .
 - IF a non-Cyclone IV device is cascaded in the JTAG-chain, TDO of the non-Cyclone IV device driving into TDI of the Cyclone IV device must fit the maximum overshoot outlined in Equation 8–1 on page 8–5.

The CONF_DONE and nSTATUS signals are shared in multi-device AS, AP, PS, and FPP configuration chains to ensure that the devices enter user mode at the same time after configuration is complete. When the CONF_DONE and nSTATUS signals are shared among all the devices, you must configure every device when JTAG configuration is performed.

If you only use JTAG configuration, Altera recommends that you connect the circuitry as shown in Figure 8–25 or Figure 8–26, in which each of the CONF_DONE and nSTATUS signals are isolated so that each device can enter user mode individually.

After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, ensure that the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multi-device configuration chain, the nCEO of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured. You can place other Altera devices that have JTAG support in the same JTAG chain for device programming and configuration.

Table 8–21 lists the optional configuration pins. If you do not enable these optional configuration pins in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Pin Name	User Mode	Pin Type	Description
	N/A if option is on		Optional user-supplied clock input synchronizes the initialization of one or more devices. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
CLKUSR	I/O if option is off.	Input	In AS configuration for Cyclone IV GX devices, you can use this pin as an external clock source to generate the DCLK by changing the clock source option in the Quartus II software in the Configuration tab of the Device and Pin Options dialog box.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Status pin is used to indicate when the device has initialized and is in user-mode. When nCONFIG is low, the INIT_DONE pin is tri-stated and pulled high due to an external 10-k Ω pull-up resistor during the beginning of configuration. After the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to- high transition. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
			The functionality of this pin changes if the Enable OCT_DONE option is enabled in the Quartus II software. This option controls whether the INIT_DONE signal is gated by the OCT_DONE signal, which indicates the power-up on-chip termination (OCT) calibration is complete. If this option is turned off, the INIT_DONE signal is not gated by the OCT_DONE signal.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. You can enable this pin by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.

Table 8–21. Optional Configuration Pins

Figure 8–32 shows the transitions between the factory configuration and application configuration in remote update mode.





After power up or a configuration error, the factory configuration logic writes the remote system upgrade control register to specify the address of the application configuration to be loaded. The factory configuration also specifies whether or not to enable the user watchdog timer for the application configuration and, if enabled, specifies the timer setting.

Only valid application configurations designed for remote update mode include the logic to reset the timer in user mode. For more information about the user watchdog timer, refer to the "User Watchdog Timer" on page 8–79.

If there is an error while loading the application configuration, the remote system upgrade status register is written by the dedicated remote system upgrade circuitry of the Cyclone IV device to specify the cause of the reconfiguration.

The following actions cause the remote system upgrade status register to be written:

- nSTATUS driven low externally
- Internal cyclical redundancy check (CRC) error
- User watchdog timer time-out
- A configuration reset (logic array nCONFIG signal or external nCONFIG pin assertion)

The Cyclone IV device automatically loads the factory configuration when an error occurs. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for reconfiguration. Then the factory configuration takes the appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

The byte ordering block operates in either word-alignment-based byte ordering or user-controlled byte ordering modes.

In word-alignment-based byte ordering mode, the byte ordering block starts looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary when it detects a rising edge on the rx_syncstatus signal. Whenever the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if the pad byte insertion is necessary. If the byte ordering block detects another rising edge on the rx_syncstatus signal from the word aligner, it deasserts the rx_byteorderalignstatus signal and repeats the byte ordering operation.

In user-controlled byte ordering mode, the byte ordering operation is user-triggered using rx_enabyteord port. A rising edge on rx_enabyteord port triggers the byte ordering block to start looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary. When the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if a pad byte insertion is necessary.

RX Phase Compensation FIFO

The RX phase compensation FIFO compensates for the phase difference between the parallel receiver clock and the FPGA fabric interface clock, when interfacing the receiver channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP blocks). The FIFO is four words deep, with latency between two to three parallel clock cycles.

Figure 1–24 shows the RX phase compensation FIFO block diagram.



Figure 1–24. RX Phase Compensation FIFO Block Diagram

Note to Figure 1-24:

(1) Parameter x refers to the transceiver channel width, where 8, 10, 16, or 20 bits are supported.

The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in the Deterministic Latency functional mode. For more information, refer to "Deterministic Latency Mode" on page 1–73. For more information about FIFO clocking, refer to "FPGA Fabric-Transceiver Interface Clocking" on page 1–43.

Miscellaneous Receiver PCS Feature

The receiver PCS supports the following additional feature:

Output bit-flip—reverses the bit order at a byte level at the output of the receiver phase compensation FIFO. For example, if the 16-bit parallel receiver data at the output of the receiver phase compensation FIFO is '10111100 10101101' (16'hBCAD), enabling this option reverses the data on rx_dataout port to '00111101 10110101' (16'h3DB5).

In configuration with rate match FIFO, the transmitter datapath clocking is identical to Transmitter Only operation as shown in Figure 1–38. In each bonded receiver channel, the CDR unit recovers the clock from serial received data and generates the high- and low-speed recovered clock for each bonded channel. The high-speed recovered clock feeds the channel's deserializer, and low-speed recovered clock is forwarded to receiver PCS. The individual low-speed recovered clock feeds to the following blocks in the receiver PCS:

- word aligner
- write clock of rate match FIFO

The common bonded low-speed clock that is used in all bonded transmitter PCS datapaths feeds the following blocks in each bonded receiver PCS:

- read clock of rate match FIFO
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the common bonded low-speed clock frequency is halved before feeding to the write clock of RX phase compensation FIFO. The common bonded low-speed clock is available in FPGA fabric as coreclkout port, which can be used in FPGA fabric to send transmitter data and control signals, and capture receiver data and status signals from the bonded channels.

FPGA Fabric-Transceiver Interface Clocking

The FPGA fabric-transceiver interface clocks consists of clock signals from the FPGA fabric to the transceiver blocks, and from the transceiver blocks to the FPGA fabric. These clock resources use the global clock networks (GCLK) in the FPGA core.

For information about the GCLK resources in the Cyclone IV GX devices, refer to *Clock Networks and PLLs in Cyclone IV Devices* chapter.

Table 1–11 lists the FPGA fabric-transceiver interface clocks.

Table 1–11. FPGA Fabric-Transceiver Interface Clocks (Part 1 of 2)

Clock Name	Clock Description	Interface Direction
tx_clkout	Phase compensation FIFO clock	Transceiver to FPGA fabric
rx_clkout	Phase compensation FIFO clock	Transceiver to FPGA fabric
coreclkout	Phase compensation FIFO clock	Transceiver to FPGA fabric
fixed_clk	125MHz receiver detect clock in PIPE mode	FPGA fabric to transceiver
reconfig_clk (1), (2)	Transceiver dynamic reconfiguration and offset cancellation clock	FPGA fabric to transceiver

Figure 1–45 and Figure 1–46 show the supported transceiver configurations in Basic mode with the 8-bit and 10-bit PMA-PCS interface width respectively.



Figure 1–45. Supported Transceiver Configurations in Basic Mode with the 8-bit PMA-PCS Interface Width

- The busy signal remains low for the first reconfig_clk clock cycle. It then gets asserted from the second reconfig_clk clock cycle. Subsequent deassertion of the busy signal indicates the completion of the offset cancellation process. This busy signal is required in transceiver reset sequences except for transmitter only channel configurations. Refer to the reset sequences shown in Figure 2–2 and the associated references listed in the notes for the figure.
- Altera strongly recommends adhering to these reset sequences for proper operation of the Cyclone IV GX transceiver.

Figure 2–2 shows the transceiver reset sequences for Cyclone IV GX devices.





Notes to Figure 2-2:

- (1) Refer to the Timing Diagram in Figure 2-10.
- (2) Refer to the Timing Diagram in Figure 2–3.
- (3) Refer to the Timing Diagram in Figure 2–4.
- (4) Refer to the Timing Diagram in Figure 2–5.
- (5) Refer to the Timing Diagram in Figure 2–6.
- (6) Refer to the Timing Diagram in Figure 2–7.
- (7) Refer to the Timing Diagram in Figure 2–8.
- (8) Refer to the Timing Diagram in Figure 2–9.

Port Name	Input/ Output		Description				
		This is an optional pre-emphasis write control for the transmit buffer. Depending on what value you set at this input, the controller dynamically writes the value to the pre-emphasis control register of the transmit buffer.					
		The width of this signal is fixed to 5 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Use same control signal for all the channels option in the Analog controls screen. Otherwise, the width of this signal is 5 bits per channel.					
		tx_preemp[40]	Corresponding ALTGX instance settings	Corresponding pre- emphasis setting (mA)			
		00000	0	Disabled			
		00001	1	0.5			
tx preemp[40] (1)	Input	00101	5	1.0			
		01001	9	1.5			
		01101	13	2.0			
		10000	16	2.375			
		10001	17	2.5			
		10010	18	2.625			
		10011	19	2.75			
		10100	20	2.875			
		10101	21	3.0			
		All other values $=> N_{i}$	Ά				
		This is an optional wr the PMA.	ite control to write an equalization cont	rol value for the receive side of			
		The width of this signal is fixed to 4 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Us same control signal for all the channels option in the Analog controls screen. Otherv the width of this signal is 4 bits per channel.					
rx_eqctrl[30] ⁽¹⁾	Input	<pre>rx_eqctrl[30]</pre>	Corresponding ALTGX instance setting	ngs			
		0001	Low				
		0101	Medium Low				
		0100	Medium High				
		0111	High				
		All other values $=> N_{i}$	Ά				

Table 3–2. Dynamic Reconfiguration Controller Port List (ALTGX_RECONFIG Instance) (Part 5 of 7)

PMA Control Ports Used in a Read Transaction

- tx_vodctrl_out is 3 bits per channel
- tx_preemp_out is 5 bits per channel
- rx eqdcgain out is 2 bits per channel
- rx_eqctrl_out is 4 bits per channel

For example, assume the number of channels controlled by the dynamic reconfiguration controller is two, tx_vodctrl_out is 6 bits wide.

Write Transaction

The value you set at the selected PMA control ports is written to all the transceiver channels connected to the ALTGX_RECONFIG instance.

For example, assume you have enabled tx_vodctrl in the ALTGX_RECONFIG MegaWizard Plug-In Manager to reconfigure the V_{OD} of the transceiver channels. To complete a write transaction to reconfigure the V_{OD}, perform the following steps:

- 1. Before you initiate a write transaction, set the selected PMA control ports to the desired settings (for example, tx_vodctrl = 3'b001).
- 2. Set the rx_tx_duplex_sel port to **2'b10** so that only the transmit PMA controls are written to the transceiver channel.
- 3. Ensure that the busy signal is low before you start a write transaction.
- 4. Assert the write_all signal for one reconfig_clk clock cycle. This initiates the write transaction.
- 5. The busy output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy writing the PMA control values. When the write transaction has completed, the busy signal goes low.

Figure 3–6 shows the write transaction for Method 2.

Figure 3–6. Write Transaction Waveform—Use the same control signal for all the channels Option



Note to Figure 3-6:

(1) In this waveform example, you want to write to only the transmitter portion of the channel.

Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Cyclone IV Device Datasheet Revised: December 2016 Part Number: CYIV-53001-2.1 Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

Symbol/	Conditions	C6			C7, 17			C8			llnit
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
PCIe Transmit Jitter Gene	ration ⁽³⁾										
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	— — 0.25		0.25	_	_	0.25	_	_	0.25	UI
PCIe Receiver Jitter Tole	rance ⁽³⁾										
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6		> 0.6			UI	
GIGE Transmit Jitter Gene	ration ⁽⁴⁾										
Deterministic jitter	Pattern – CBPAT	_		0 14			0 14			0 14	111
(peak-to-peak)				0.14			0.14			0.14	01
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279		—	0.279	_	—	0.279	UI
GIGE Receiver Jitter Tole	rance ⁽⁴⁾										
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4		> 0.4		ļ	UI	
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66		> 0.66			> 0.66			UI	

Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices (1), (2)

Notes to Table 1-23:

(1) Dedicated refclk pins were used to drive the input reference clocks.

(2) The jitter numbers specified are valid for the stated conditions only.

(3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.

(4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

 Table 1–24.
 Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)

Device		Performance								
Device	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	17	18L ⁽¹⁾	A7	Unit	
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz	
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz	
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz	
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz	
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz	
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz	