Intel - EP4CE10E22I7 Datasheet





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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	645
Number of Logic Elements/Cells	10320
Total RAM Bits	423936
Number of I/O	91
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce10e22i7

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In addition to the three general routing outputs, LEs in an LAB have register chain outputs, which allows registers in the same LAB to cascade together. The register chain output allows the LUTs to be used for combinational functions and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources.

LE Operating Modes

Cyclone IV LEs operate in the following modes:

- Normal mode
- Arithmetic mode

The Quartus[®] II software automatically chooses the appropriate mode for common functions, such as counters, adders, subtractors, and arithmetic functions, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions. You can also create special-purpose functions that specify which LE operating mode to use for optimal performance, if required.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (Figure 2–2). The Quartus II Compiler automatically selects the carry-in (cin) or the data3 signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

Figure 2–2 shows LEs in normal mode.





2–3

LAB Interconnects

The LAB local interconnect is driven by column and row interconnects and LE outputs in the same LAB. Neighboring LABs, phase-locked loops (PLLs), M9K RAM blocks, and embedded multipliers from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive up to 48 LEs through fast local and direct link interconnects.

Figure 2–5 shows the direct link connection.



Figure 2–5. Cyclone IV Device Direct Link Connection

LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include:

- Two clocks
- Two clock enables
- Two asynchronous clears
- One synchronous clear
- One synchronous load

You can use up to eight control signals at a time. Register packing and synchronous load cannot be used simultaneously.

Each LAB can have up to four non-global control signals. You can use additional LAB control signals as long as they are global signals.

Synchronous clear and load signals are useful for implementing counters and other functions. The synchronous clear and synchronous load signals are LAB-wide signals that affect all registers in the LAB.

3. Memory Blocks in Cyclone IV Devices

Cyclone[®] IV devices feature embedded memory structures to address the on-chip memory needs of Altera[®] Cyclone IV device designs. The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

This chapter contains the following sections:

- "Memory Modes" on page 3–7
- "Clocking Modes" on page 3–14
- "Design Considerations" on page 3–15

Overview

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (rden) and write-enable (wren) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

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Violating the setup or hold time on the M9K memory block input registers may corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations from a single address. Figure 3–6 shows the single-port memory configuration for Cyclone IV devices M9K memory blocks.

Figure 3–6. Single-Port Memory ⁽¹⁾, ⁽²⁾



Notes to Figure 3-6:

- (1) You can implement two single-port memory blocks in a single M9K block.
- (2) For more information, refer to "Packed Mode Support" on page 3-4.

During a write operation, the behavior of the RAM outputs is configurable. If you activate rden during a write operation, the RAM outputs show either the new data being written or the old data at that address. If you perform a write operation with rden deactivated, the RAM outputs retain the values they held during the most recent active rden signal.

To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about read-during-write mode, refer to "Read-During-Write Operations" on page 3–15.

The port width configurations for M9K blocks in single-port mode are as follow:

- 8192 × 1
- 4096 × 2
- 2048 × 4
- 1024 × 8
- 1024 × 9
- 512 × 16
- 512 × 18
- 256 × 32
- 256 × 36

18-Bit Multipliers

You can configure each embedded multiplier to support a single 18×18 multiplier for input widths of 10 to 18 bits.

Figure 4–3 shows the embedded multiplier configured to support an 18-bit multiplier.



Figure 4–3. 18-Bit Multiplier Mode

All 18-bit multiplier inputs and results are independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Also, you can dynamically change the signa and signb signals and send these signals through dedicated input registers.

- Low time count = 1 cycle
- rselodd = 1 effectively equals:
 - High time count = 1.5 cycles
 - Low time count = 1.5 cycles
 - Duty cycle = (1.5/3)% high time count and (1.5/3)% low time count

Scan Chain Description

Cyclone IV PLLs have a 144-bit scan chain.

Table 5–7 lists the number of bits for each component of the PLL.

Table 5–7.	Cyclone	IV PLL	Reprogramming Bits
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Pleak Nome		Number of Bits	
DIUCK Name	Counter	Other	Total
C4 (1)	16	2 (2)	18
C3	16	2 (2)	18
C2	16	2 (2)	18
C1	16	2 (2)	18
CO	16	2 (2)	18
М	16	2 (2)	18
Ν	16	2 (2)	18
Charge Pump	9	0	9
Loop Filter ⁽³⁾	9	0	9
Total number of bits:			144

Notes to Table 5-7:

(1) LSB bit for C4 low-count value is the first bit shifted into the scan chain.

- (2) These two control bits include <code>rbypass</code>, for bypassing the counter, and <code>rselodd</code>, to select the output clock duty cycle.
- (3) MSB bit for loop filter is the last bit shifted into the scan chain.

Figure 5–24 shows the scan chain order of the PLL components.

Figure 5–24. PLL Component Scan Chain Order



before the next edge; this may lead to pattern-dependent jitter. With pre-emphasis, the output current is momentarily boosted during switching to increase the output slew rate. The overshoot produced by this extra switching current is different from the overshoot caused by signal reflection. This overshoot happens only during switching, and does not produce ringing.

The Quartus II software allows two settings for programmable pre-emphasis control—0 and 1, in which 0 is pre-emphasis off and 1 is pre-emphasis on. The default setting is 1. The amount of pre-emphasis needed depends on the amplification of the high-frequency components along the transmission line. You must adjust the setting to suit your designs, as pre-emphasis decreases the amplitude of the low-frequency component of the output signal.

Figure 6–20 shows the differential output signal with pre-emphasis.

Figure 6–20. The Output Signal with Pre-Emphasis



High-Speed I/O Timing

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone IV devices. Timing for source-synchronous signaling is based on skew between the data and clock signals.

High-speed differential data transmission requires timing parameters provided by IC vendors and requires you to consider the board skew, cable skew, and clock jitter. This section provides information about high-speed I/O standards timing parameters in Cyclone IV devices.

Table 6–11 defines the parameters of the timing diagram shown in Figure 6–21.

Table 6–11. High-Speed I/O Timing Definitions (Part 1 of 2)

Parameter	Symbol	Description
Transmitter channel-to-channel skew ⁽¹⁾	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. $T_{SW} = T_{SU} + T_{hd} + PLL$ jitter.
Time unit interval	TUI	The TUI is the data-bit timing budget allowed for skew, propagation delays, and data sampling window.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: $SKM = \frac{(TUI - SW - TCCS)}{2}$

Figure 7–9 illustrates how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.



Figure 7–9. Extending the OE Disable by Half a Clock Cycle for a Write Transaction ⁽¹⁾

Note to Figure 7-9:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A_{OE} register D input.

OCT with Calibration

Cyclone IV devices support calibrated on-chip series termination (R_S OCT) in both vertical and horizontal I/O banks. To use the calibrated OCT, you must use the RUP and RDN pins for each R_S OCT control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO} for that given side.

 For more information about the Cyclone IV devices OCT calibration block, refer to the Cyclone IV Device I/O Features chapter.

PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by -90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

- The PLL is instantiated in the ALTMEMPHY megafunction. All outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories. PLL reconfiguration is used in the ALTMEMPHY megafunction to calibrate and track the read-capture phase to maintain the optimum margin.
- **For more information about usage of PLL outputs by the ALTMEMPHY** megafunction, refer to the *External Memory Interface Handbook*.

- "FPP Configuration" on page 8–40
- "JTAG Configuration" on page 8–45
- "Device Configuration Pins" on page 8–62

Configuration Features

Table 8–1 lists the configuration methods you can use in each configuration scheme.

Table 8–1. Configuration Features in Cyclone IV Devices

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade ⁽¹⁾
AS	Serial Configuration Device	~	\checkmark
AP	Supported Flash Memory (2)	_	\checkmark
DC	External Host with Flash Memory	\checkmark	✓ (3)
	Download Cable	~	_
FPP	External Host with Flash Memory	—	✓ (3)
ITAC based configuration	External Host with Flash Memory	—	_
o rAd based connyuration	Download Cable	—	_

Notes to Table 8-1:

(1) Remote update mode is supported when you use the Remote System Upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus® II software.

(2) For more information about the supported device families for the Micron commodity parallel flash, refer to Table 8–10 on page 8–22.

(3) Remote update mode is supported externally using the Parallel Flash Loader (PFL) with the Quartus II software.

Configuration Data Decompression

Cyclone IV devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to Cyclone IV devices. During configuration, Cyclone IV devices decompress the bitstream in real time and program the SRAM cells.

Compression may reduce the configuration bitstream size by 35 to 55%.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the Cyclone IV device. The time required by a Cyclone IV device to decompress a configuration file is less than the time required to send the configuration data to the device. There are two methods for enabling compression for the Cyclone IV device bitstreams in the Quartus II software:

- Before design compilation (through the Compiler Settings menu)
- After design compilation (through the **Convert Programming Files** dialog box)

To enable compression in the compiler settings of the project in the Quartus II software, perform the following steps:

- 1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
- 2. Click Device and Pin Options. The Device and Pin Options dialog box appears.

For more information about the operation of the Micron P30 Parallel NOR and P33 Parallel NOR flash memories, search for the keyword "P30" or "P33" on the Micron website (www.micron.com) to obtain the P30 or P33 family datasheet.

Single-Device AP Configuration

The following groups of interface pins are supported in Micron P30 and P33 flash memories:

- Control pins
- Address pins
- Data pins

The following control signals are from the supported parallel flash memories:

- CLK
- active-low reset (RST#)
- active-low chip enable (CE#)
- active-low output enable (OE#)
- active-low address valid (ADV#)
- active-low write enable (WE#)

The supported parallel flash memories output a control signal (WAIT) to Cyclone IV E devices to indicate when synchronous data is ready on the data bus. Cyclone IV E devices have a 24-bit address bus connecting to the address bus (A[24:1]) of the flash memory. A 16-bit bidirectional data bus (DATA[15..0]) provides data transfer between the Cyclone IV E device and the flash memory.

The following control signals are from the Cyclone IV E device to flash memory:

- DCLK
- active-low hard rest (nRESET)
- active-low chip enable (FLASH_nCE)
- active-low output enable for the DATA [15..0] bus and WAIT pin (nOE)
- active-low address valid signal and is used to write data into the flash (nAVD)
- active-low write enable and is used to write data into the flash (nWE)

Table 9–6 lists the estimated time for each CRC calculation with minimum and maximum clock frequencies for Cyclone IV devices.

Table	9–6.	CRC	Calculation	Time
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Dev	vice	Minimum Time (ms) ⁽¹⁾	Maximum Time (s) ⁽²⁾
	EP4CE6 (3)	5	2.29
	EP4CE10 (3)	5	2.29
	EP4CE15 (3)	7	3.17
	EP4CE22 (3)	9	4.51
Cyclone IV E	EP4CE30 (3)	15	7.48
	EP4CE40 (3)	15	7.48
	EP4CE55 (3)	23	11.77
	EP4CE75 (3)	31	15.81
	EP4CE115 (3)	45	22.67
	EP4CGX15	6	2.93
	EP4CGX22	12	5.95
		12	5.95
Cuelone IV CV		34 (4)	17.34 ⁽⁴⁾
	EP4CGX50	34	17.34
	EP4CGX75	34	17.34
	EP4CGX110	62	31.27
EP4CGX150		62	31.27

Notes to Table 9-6:

(1) The minimum time corresponds to the maximum error detection clock frequency and may vary with different processes, voltages, and temperatures (PVT).

(2) The maximum time corresponds to the minimum error detection clock frequency and may vary with different PVT.

(3) Only applicable for device with 1.2-V core voltage

(4) Only applicable for the F484 device package.

Software Support

Enabling the CRC error detection feature in the Quartus II software generates the CRC_ERROR output to the optional dual purpose CRC_ERROR pin.

To enable the error detection feature using CRC, perform the following steps:

- 1. Open the Quartus II software and load a project using Cyclone IV devices.
- 2. On the Assignments menu, click Settings. The Settings dialog box appears.
- 3. In the Category list, select **Device**. The **Device** page appears.
- 4. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears as shown in Figure 9–2.
- 5. In the **Device and Pin Options** dialog box, click the **Error Detection CRC** tab.
- 6. Turn on Enable error detection CRC.
- 7. In the **Divide error check frequency by** box, enter a valid divisor as documented in Table 9–5 on page 9–5.

Device	Boundary-Scan Register Length
EP4CGX75	1006
EP4CGX110	1495
EP4CGX150	1495

Table 10–1. B	Boundarv-Scan Re	aister Lenath for (Cyclone IV Devices	(Part 2 of 2)
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Note to Table 10–1:

(1) For the F484 package of the EP4CGX30 device, the boundary-scan register length is 1006.

Table 10–2 lists the IDCODE information for Cyclone IV devices.

Table 10-2.	IDCODE Information	for 32-Bit C	yclone IV Devices
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		IDCODE (32 Bits) (1	0	
Device	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) ⁽²⁾
EP4CE6	0000	0010 0000 1111 0001	000 0110 1110	1
EP4CE10	0000	0010 0000 1111 0001	000 0110 1110	1
EP4CE15	0000	0010 0000 1111 0010	000 0110 1110	1
EP4CE22	0000	0010 0000 1111 0011	000 0110 1110	1
EP4CE30	0000	0010 0000 1111 0100	000 0110 1110	1
EP4CE40	0000	0010 0000 1111 0100	000 0110 1110	1
EP4CE55	0000	0010 0000 1111 0101	000 0110 1110	1
EP4CE75	0000	0010 0000 1111 0110	000 0110 1110	1
EP4CE115	0000	0010 0000 1111 0111	000 0110 1110	1
EP4CGX15	0000	0010 1000 0000 0001	000 0110 1110	1
EP4CGX22	0000	0010 1000 0001 0010	000 0110 1110	1
EP4CGX30 (3)	0000	0010 1000 0000 0010	000 0110 1110	1
EP4CGX30 (4)	0000	0010 1000 0010 0011	000 0110 1110	1
EP4CGX50	0000	0010 1000 0001 0011	000 0110 1110	1
EP4CGX75	0000	0010 1000 0000 0011	000 0110 1110	1
EP4CGX110	0000	0010 1000 0001 0100	000 0110 1110	1
EP4CGX150	0000	0010 1000 0000 0100	000 0110 1110	1

Notes to Table 10-2:

(1) The MSB is on the left.

(2) The IDCODE LSB is always 1.

(3) The IDCODE is applicable for all packages except for the F484 package.

(4) The IDCODE is applicable for the F484 package only.

IEEE Std.1149.6 mandates the addition of two new instructions: EXTEST_PULSE and EXTEST_TRAIN. These two instructions enable edge-detecting behavior on the signal path containing the AC pins.

Visual Cue	Meaning	
	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. The suffix n denotes an active-low signal. For example, resetn.	
Courier type	Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.	
	Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).	
4	An angled arrow instructs you to press the Enter key.	
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.	
	Bullets indicate a list of items when the sequence of the items is not important.	
LP	The hand points to information that requires special attention.	
0	The question mark directs you to a software help system with related information.	
	The feet direct you to another document or website with related information.	
▋┯∎	The multimedia icon directs you to a related multimedia presentation.	
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.	
VIARNING	A warning calls attention to a condition or possible situation that can cause you injury.	
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.	

Clock Data Recovery

Each receiver channel has an independent CDR unit to recover the clock from the incoming serial data stream. The high-speed recovered clock is used to clock the deserializer for serial-to-parallel conversion of the received input data, and low-speed recovered clock to clock the receiver PCS blocks. Figure 1–15 illustrates the CDR unit block diagram.





Notes to Figure 1-15:

- (1) Optional RX local divider for CDR clocks from multipurpose PLL is only available in each CDR unit for EP4CGX30 (F484 package), EP4CGX50, and EP4CGX75 devices. This block is used with the transceiver dynamic reconfiguration feature. For more information, refer to the Cyclone IV Dynamic Reconfiguration chapter and AN 609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices.
- (2) CDR state transition in automatic lock mode is not dependent on rx_signaldetect signal, except when configured in PCI Express (PIPE) mode only.

Each CDR unit gets the reference clock from one of the two multipurpose phase-locked loops (PLLs) adjacent to the transceiver block. The CDR works by tracking the incoming data with a phase detector and finding the optimum sampling clock phase from the phase interpolator unit. The CDR operations are controlled by the LTR/LTD controller block, where the CDR may operate in the following states:

- Lock-to-reference (LTR) state—phase detector disabled and CDR ignores incoming data
- Lock-to-data (LTD) state—phase detector enabled and CDR tracks incoming data to find the optimum sampling clock phase

State transitions are supported with automatic lock mode and manual lock mode.

Automatic Lock Mode

Upon receiver power-up and reset cycle, the CDR is put into LTR state. Transition to the LTD state is performed automatically when both of the following conditions are met:

- Signal detection circuitry indicates the presence of valid signal levels at the receiver input buffer. This condition is valid for PCI Express (PIPE) mode only. CDR transitions are not dependent on signal detection circuitry in other modes.
- The recovered clock is within the configured part per million (ppm) frequency threshold setting with respect to the CDR clocks from multipurpose PLL.

The byte ordering block operates in either word-alignment-based byte ordering or user-controlled byte ordering modes.

In word-alignment-based byte ordering mode, the byte ordering block starts looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary when it detects a rising edge on the rx_syncstatus signal. Whenever the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if the pad byte insertion is necessary. If the byte ordering block detects another rising edge on the rx_syncstatus signal from the word aligner, it deasserts the rx_byteorderalignstatus signal and repeats the byte ordering operation.

In user-controlled byte ordering mode, the byte ordering operation is user-triggered using rx_enabyteord port. A rising edge on rx_enabyteord port triggers the byte ordering block to start looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary. When the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if a pad byte insertion is necessary.

RX Phase Compensation FIFO

The RX phase compensation FIFO compensates for the phase difference between the parallel receiver clock and the FPGA fabric interface clock, when interfacing the receiver channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP blocks). The FIFO is four words deep, with latency between two to three parallel clock cycles.

Figure 1–24 shows the RX phase compensation FIFO block diagram.



Figure 1–24. RX Phase Compensation FIFO Block Diagram

Note to Figure 1-24:

(1) Parameter x refers to the transceiver channel width, where 8, 10, 16, or 20 bits are supported.

The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in the Deterministic Latency functional mode. For more information, refer to "Deterministic Latency Mode" on page 1–73. For more information about FIFO clocking, refer to "FPGA Fabric-Transceiver Interface Clocking" on page 1–43.

Miscellaneous Receiver PCS Feature

The receiver PCS supports the following additional feature:

Output bit-flip—reverses the bit order at a byte level at the output of the receiver phase compensation FIFO. For example, if the 16-bit parallel receiver data at the output of the receiver phase compensation FIFO is '10111100 10101101' (16'hBCAD), enabling this option reverses the data on rx_dataout port to '00111101 10110101' (16'h3DB5).

Receiver Spread Spectrum Clocking

Asynchronous SSC is not supported in Cyclone IV devices. You can implement only synchronous SSC for SATA, V-by-One, and Display Port protocols in Basic mode.

PCI Express (PIPE) Mode

PIPE mode provides the transceiver channel datapath configuration that supports ×1, ×2, and ×4 initial lane width for PCIe Gen1 signaling rate with PIPE interface implementation. The Cyclone IV GX transceiver provides following features in PIPE mode:

- PIPE interface
- receiver detection circuitry
- electrical idle control
- signal detect at receiver
- lane synchronization with compliant state machine
- clock rate compensation with rate match FIFO
- Low-Latency Synchronous PCIe
- fast recovery from P0s state
- electrical idle inference
- compliance pattern transmission
- reset requirement

Figure 1–48 shows the transceiver channel datapath and clocking when configured in PIPE mode with ×1 channel configuration.

Figure 1–48. Transceiver Channel Datapath and Clocking when Configured in PIPE Mode with ×1 Channel Configuration



Notes to Figure 1-48:

- (1) Low-speed recovered clock.
- (2) High-speed recovered clock.

Transmitter Only Channel

This configuration contains only a transmitter channel. If you create a **Transmitter Only** instance in the ALTGX MegaWizard Plug-In Manager in Basic ×4 functional mode, use the reset sequence shown in Figure 2–3.





As shown in Figure 2–3, perform the following reset procedure for the **Transmitter Only** channel configuration:

- 1. After power up, assert pll_areset for a minimum period of 1 µs (the time between markers 1 and 2).
- 2. Keep the tx_digitalreset signal asserted during this time period. After you de-assert the pll_areset signal, the multipurpose PLL starts locking to the transmitter input reference clock.
- 3. When the multipurpose PLL locks, as indicated by the pll_locked signal going high (marker 3), de-assert the tx_digitalreset signal (marker 4). At this point, the transmitter is ready for transmitting data.

Table 3–5 describes the <code>rx_dataoutfull[31..0]</code> FPGA fabric-Transceiver channel interface signals.

Table 3–5. rx_da	taoutfull[310] FPGA Fa	abric-Transceiver Chan	nel Interface Signal D	escriptions (Part 1 of 3)

FPGA Fabric-Transceiver Channel Interface Description	Receive Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)							
	The following signals are used in 8-bit 8B/10B modes:							
	<pre>rx_dataoutfull[7:0]: 8-bit decoded data (rx_dataout)</pre>							
	<pre>rx_dataoutfull[8]: Control bit (rx_ctrldetect)</pre>							
	<pre>rx_dataoutfull[9]: Code violation status signal (rx_errdetect)</pre>							
	rx_dataoutfull[10]: rx_syncstatus							
8-bit FPGA fabric-Transceiver	<pre>rx_dataoutfull[11]: Disparity error status signal (rx_disperr)</pre>							
Channel Interface	<pre>rx_dataoutfull[12]: Pattern detect status signal (rx_patterndetect)</pre>							
	<pre>rx_dataoutfull[13]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes.</pre>							
	<pre>rx_dataoutfull[14]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes.</pre>							
	<pre>rx_dataoutfull[14:13]: PCI Express (PIPE) functional mode (rx_pipestatus)</pre>							
	<pre>rx_dataoutfull[15]: 8B/10B running disparity indicator (rx_runningdisp)</pre>							
	<pre>rx_dataoutfull[9:0]: 10-bit un-encoded data (rx_dataout)</pre>							
	rx_dataoutfull[10]:rx_syncstatus							
	<pre>rx_dataoutfull[11]: 8B/10B disparity error indicator (rx_disperr)</pre>							
10-hit FPGA fabric-Transceiver	rx_dataoutfull[12]:rx_patterndetect							
Channel Interface	rx_dataoutfull[13]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes							
	<pre>rx_dataoutfull[14]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes</pre>							
	<pre>rx_dataoutfull[15]: 8B/10B running disparity indicator (rx_runningdisp)</pre>							

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Symbol/	• ····	C6				C7, 17			11		
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Signal detect/loss threshold	PIPE mode	65	_	175	65	_	175	65	_	175	mV
t _{LTR} (10)	—		_	75		_	75	_	—	75	μs
t _{LTR-LTD_Manual} (11)	—	15	_	_	15	—		15	_	—	μs
t _{LTD} (12)	—	0	100	4000	0	100	4000	0	100	4000	ns
t _{LTD_Manual} <i>(13)</i>	—		_	4000			4000	_		4000	ns
t _{LTD_Auto} (14)	—	_	_	4000		—	4000		_	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	_	_	_	17000	_	_	17000	_	_	17000	recon fig_c lk cycles
	DC Gain Setting = 0		0	_	_	0	_	_	0	_	dB
Programmable DC gain	DC Gain Setting = 1	_	3	_	_	3	_	_	3	_	dB
	DC Gain Setting = 2	_	6	_	_	6	_	_	6	_	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	_	600	_	2500	600	_	2500	600	_	2500	Mbps
Data rate (F484 and larger package)	_	600	_	3125	600	_	3125	600	_	2500	Mbps
V _{OCM}	0.65 V setting	_	650	_		650		_	650	_	mV
Differential on-chip	100– Ω setting	_	100	_		100		_	100	—	Ω
termination resistors	150– Ω setting	_	150	_	_	150		_	150	—	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA	Compliant								_	
Rise time	—	50	_	200	50	—	200	50	—	200	ps
Fall time		50	_	200	50	—	200	50	—	200	ps
Intra-differential pair skew	_	_	_	15	_	_	15	_	_	15	ps
Intra-transceiver block skew	_	_	_	120	_	_	120	_	_	120	ps

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

		Numbor		Max Offset								
Parameter	Paths Affected	of	Min Offset	Fa	ast Corn	er	Slow Corner					Unit
		Setting		C6	17	A7	C6	C7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1-42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

		Numbor		Max Offset								
Parameter	Paths Affected	of	Min Offset	Fast Corner			Slow Corner					Unit
		Setting		C6	17	A7	C6	C7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2)

Notes to Table 1-43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.