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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	645
Number of Logic Elements/Cells	10320
Total RAM Bits	423936
Number of I/O	179
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce10f17c8ln

Table 5-3. GCLK Network Connections for Cyclone IV E Devices ⁽¹⁾ (Part 3 of 3)

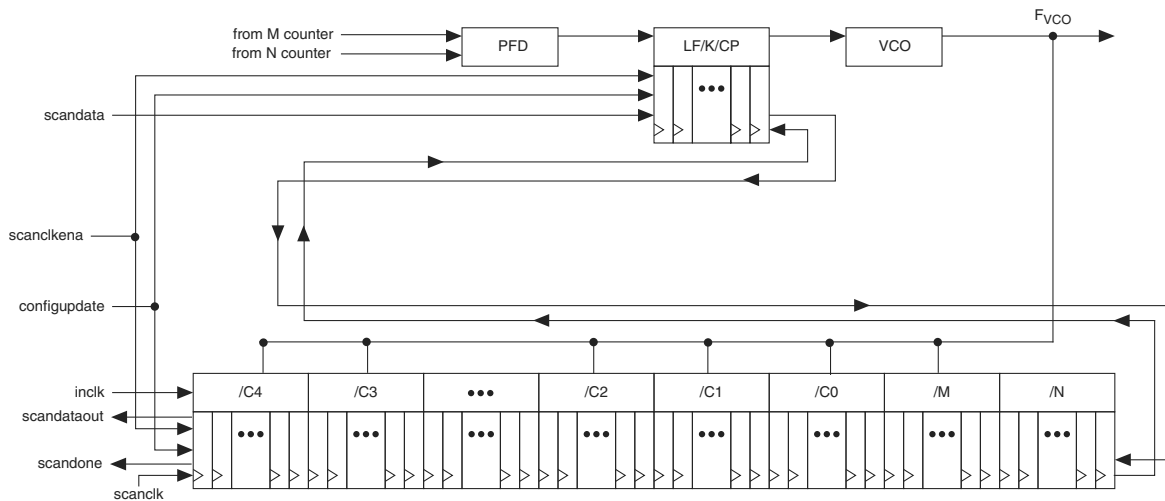
GCLK Network Clock Sources	GCLK Networks																			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
DPCLK2 ⁽⁴⁾ CDPCLK1, or CDPCLK2 ^{(2), (5)}	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK5 ⁽⁴⁾ DPCLK7 ⁽²⁾	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK4 ⁽⁴⁾ DPCLK6 ⁽²⁾	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK6 ⁽⁴⁾ CDPCLK5, or CDPCLK6 ^{(2), (5)}	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK3 ⁽⁴⁾ CDPCLK4, or CDPCLK3 ^{(2), (5)}	—	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—
DPCLK8	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
DPCLK11	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
DPCLK9	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
DPCLK10	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—
DPCLK5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—
DPCLK2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
DPCLK4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
DPCLK3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓


Notes to Table 5-3:

- (1) EP4CE6 and EP4CE10 devices only have GCLK networks 0 to 9.
- (2) These pins apply to all Cyclone IV E devices except EP4CE6 and EP4CE10 devices.
- (3) EP4CE6 and EP4CE10 devices only have PLL_1 and PLL_2.
- (4) This pin applies only to EP4CE6 and EP4CE10 devices.
- (5) Only one of the two CDPCLK pins can feed the clock control block. You can use the other pin as a regular I/O pin.

Figure 5-22 shows how to adjust PLL counter settings dynamically by shifting their new settings into a serial shift register chain or scan chain. Serial data shifts to the scan chain via the `scandata` port, and shift registers are clocked by `scanclk`. The maximum `scanclk` frequency is 100 MHz. After shifting the last bit of data, asserting the `configupdate` signal for at least one `scanclk` clock cycle synchronously updates the PLL configuration bits with the data in the scan registers.

Figure 5-22. PLL Reconfiguration Scan Chain



 The counter settings are updated synchronously to the clock frequency of the individual counters. Therefore, not all counters update simultaneously.

To reconfigure the PLL counters, perform the following steps:

1. The `scanclkena` signal is asserted at least one `scanclk` cycle prior to shifting in the first bit of `scandata` (D0).
2. Serial data (`scandata`) is shifted into the scan chain on the second rising edge of `scanclk`.
3. After all 144 bits have been scanned into the scan chain, the `scanclkena` signal is de-asserted to prevent inadvertent shifting of bits in the scan chain.
4. The `configupdate` signal is asserted for one `scanclk` cycle to update the PLL counters with the contents of the scan chain.
5. The `scandone` signal goes high indicating that the PLL is being reconfigured. A falling edge indicates that the PLL counters have been updated with new settings.
6. Reset the PLL using the `areset` signal if you make any changes to the M, N, post-scale output C counters, or the I_{CP} , R, C settings.
7. You can repeat steps 1 through 5 to reconfigure the PLL any number of times.

Table 5–10. Loop Filter Control of High Frequency Capacitor

LFC[1]	LFC[0]	Setting (Decimal)
0	0	0
0	1	1
1	1	3

Bypassing a PLL Counter

Bypassing a PLL counter results in a divide (N, C0 to C4 counters) factor of one.

Table 5–11 lists the settings for bypassing the counters in PLLs of Cyclone IV devices.

Table 5–11. PLL Counter Settings

PLL Scan Chain Bits [0..8] Settings								Description
LSB							MSB	
X	X	X	X	X	X	X	1 ⁽¹⁾	PLL counter bypassed
X	X	X	X	X	X	X	0 ⁽¹⁾	PLL counter not bypassed

Note to Table 5–11:

(1) Bypass bit.

To bypass any of the PLL counters, set the bypass bit to 1. The values on the other bits are then ignored.

Dynamic Phase Shifting

The dynamic phase shifting feature allows the output phase of individual PLL outputs to be dynamically adjusted relative to each other and the reference clock without sending serial data through the scan chain of the corresponding PLL. This feature simplifies the interface and allows you to quickly adjust t_{CO} delays by changing output clock phase shift in real time. This is achieved by incrementing or decrementing the VCO phase-tap selection to a given C counter or to the M counter. The phase is shifted by 1/8 the VCO frequency at a time. The output clocks are active during this phase reconfiguration process.

Table 5–12 lists the control signals that are used for dynamic phase shifting.

Table 5–12. Dynamic Phase Shifting Control Signals (Part 1 of 2)

Signal Name	Description	Source	Destination
phasecounterselect[2..0]	Counter Select. Three bits decoded to select either the M or one of the C counters for phase adjustment. One address map to select all C counters. This signal is registered in the PLL on the rising edge of <code>scanclk</code> .	Logic array or I/O pins	PLL reconfiguration circuit
phaseupdown	Selects dynamic phase shift direction; 1 = UP, 0 = DOWN. Signal is registered in the PLL on the rising edge of <code>scanclk</code> .	Logic array or I/O pins	PLL reconfiguration circuit
phasestep	Logic high enables dynamic phase shifting.	Logic array or I/O pins	PLL reconfiguration circuit

devices. The internal oscillator is designed to ensure that its maximum frequency is guaranteed to meet EPCS device specifications. Cyclone IV devices offer the option to select `CLKUSR` as the external clock source for `DCLK`. You can change the clock source option in the Quartus II software in the **Configuration** tab of the **Device and Pin Options** dialog box.



EPCS1 does not support Cyclone IV devices because of its insufficient memory capacity.

Table 8-6. AS DCLK Output Frequency

Oscillator	Minimum	Typical	Maximum	Unit
40 MHz	20	30	40	MHz

In configuration mode, the Cyclone IV device enables the serial configuration device by driving the `nCS0` output pin low, which connects to the `nCS` pin of the configuration device. The Cyclone IV device uses the `DCLK` and `DATA[1]` pins to send operation commands and read address signals to the serial configuration device. The configuration device provides data on its `DATA` pin, which connects to the `DATA[0]` input of the Cyclone IV device.

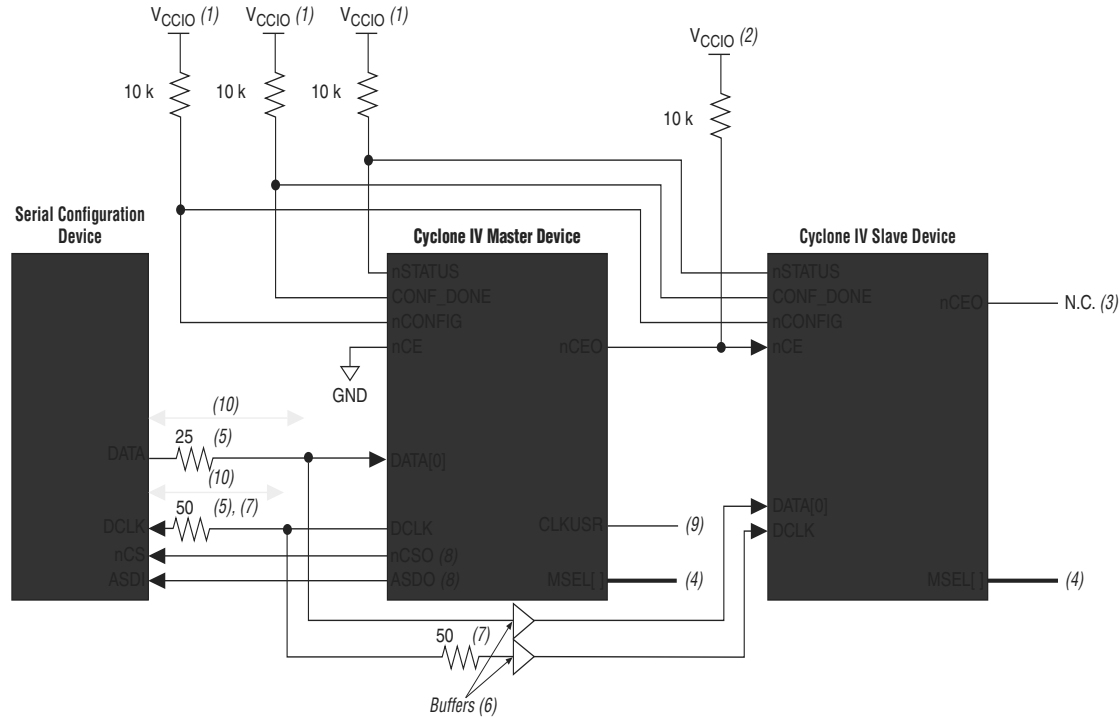
All AS configuration pins (`DATA[0]`, `DCLK`, `nCS0`, and `DATA[1]`) have weak internal pull-up resistors that are always active. After configuration, these pins are set as input tri-stated and are driven high by the weak internal pull-up resistors.

The timing parameters for AS mode are not listed here because the t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , t_{CF2ST1} , and t_{CD2UM} timing parameters are identical to the timing parameters for PS mode shown in Table 8-12 on page 8-36.

Multi-Device AS Configuration

You can configure multiple Cyclone IV devices with a single serial configuration device. When the first device captures all its configuration data from the bitstream, it drives the `nCEO` pin low, enabling the next device in the chain. If the last device in the chain is a Cyclone IV device, you can leave the `nCEO` pin of the last device unconnected or use it as a user I/O pin after configuration. The `nCONFIG`, `nSTATUS`, `CONF_DONE`, `DCLK`, and `DATA[0]` pins of each device in the chain are connected together (Figure 8-3).

Figure 8-3. Multi-Device AS Configuration



Notes to Figure 8-3:

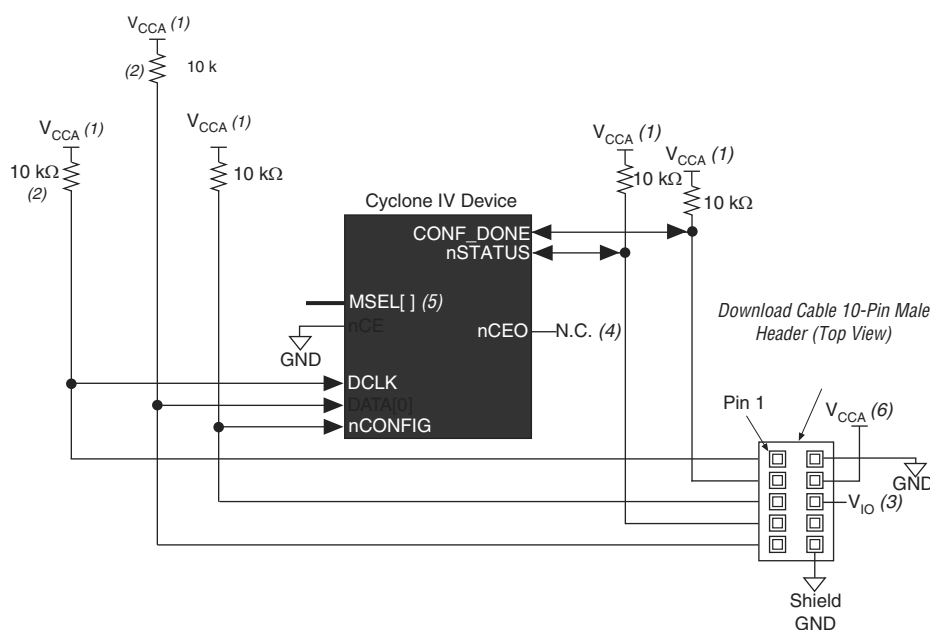
- (1) Connect the pull-up resistors to the `VCCIO` supply of the bank in which the pin resides.
- (2) Connect the pull-up resistor to the `VCCIO` supply voltage of I/O bank in which the `nCEO` pin resides.
- (3) You can leave the `nCEO` pin unconnected or use it as a user I/O pin when it does not feed the `nCEO` pin of another device.
- (4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the master device of the Cyclone IV device in AS mode and the slave devices in PS mode. To connect the `MSEL` pins for the master device in AS mode and slave devices in PS mode, refer to Table 8-3 on page 8-8, Table 8-4 on page 8-8, and Table 8-5 on page 8-9. Connect the `MSEL` pins directly to `VCCA` or GND.
- (5) Connect the series resistor at the near end of the serial configuration device.
- (6) Connect the repeater buffers between the master and slave devices of the Cyclone IV device for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8-5.
- (7) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.
- (8) These pins are dual-purpose I/O pins. The `nCSO` pin functions as `FLASH_nCEO` pin in AP mode. The `ASDO` pin functions as `DATA[1]` pin in AP and FPP modes.
- (9) Only Cyclone IV GX devices have an option to select `CLKUSR` (40 MHz maximum) as the external clock source for `DCLK`.
- (10) For multi-devices AS configuration using Cyclone IV E with 1.0 V core voltage, the maximum board trace-length from the serial configuration device to the junction-split on both `DCLK` and `Data0` line is 3.5 inches.

The programming hardware or download cable then places the configuration data one bit at a time on the DATA[0] pin of the device. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-k Ω pull-up resistor for the device to initialize.

When you use a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software if an error occurs. Additionally, the **Enable user-supplied start-up clock (CLKUSR)** option has no effect on device initialization, because this option is disabled in the .sof when programming the device with the Quartus II Programmer and download cable. Therefore, if you turn on the CLKUSR option, you do not have to provide a clock on CLKUSR when you configure the device with the Quartus II Programmer and a download cable.

Figure 8-17 shows PS configuration for Cyclone IV devices with a download cable.

Figure 8-17. PS Configuration Using a Download Cable



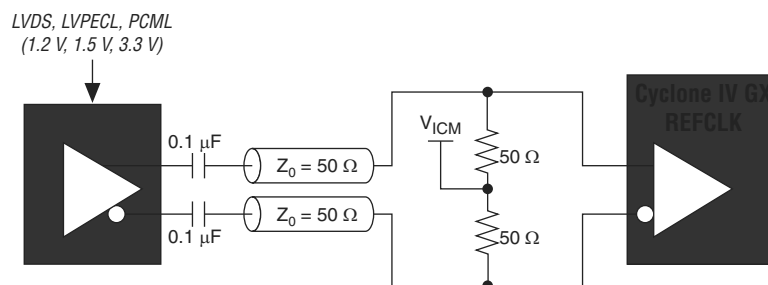
Notes to Figure 8-17:

- (1) You must connect the pull-up resistor to the same supply voltage as the V_{CCA} supply.
- (2) The pull-up resistors on DATA[0] and DCLK are only required if the download cable is the only configuration scheme used on your board. This is to ensure that DATA[0] and DCLK are not left floating after configuration. For example, if you also use a configuration device, the pull-up resistors on DATA[0] and DCLK are not required.
- (3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. With the USB-Blaster, ByteBlaster II, ByteBlaster MV, and EthernetBlaster, this pin is a no connect.
- (4) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (5) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8-3 on page 8-8, Table 8-4 on page 8-8, and Table 8-5 on page 8-9 for PS configuration schemes. Connect the MSEL pins directly to V_{CCA} or GND.
- (6) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA} . Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

When Cyclone IV devices successfully load the application configuration, they enter user mode. In user mode, the soft logic (the Nios II processor or state machine and the remote communication interface) assists the Cyclone IV device in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and starts system reconfiguration.

Figure 1-27 shows an example of the termination scheme for AC-coupled connections for REFCLK pins.

Figure 1-27. AC-Coupled Termination Scheme for a Reference Clock

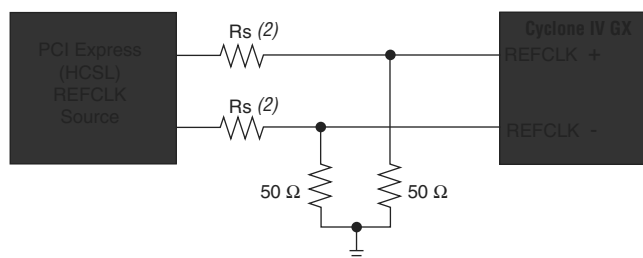


Note to Figure 1-27:

- (1) For more information about the V_{ICM} value, refer to the *Cyclone IV Device Datasheet* chapter.

Figure 1-28 shows an example termination scheme for the REFCLK pin when configured as a HCSL input.

Figure 1-28. Termination Scheme for a Reference Clock When Configured as HCSL ⁽¹⁾



Notes to Figure 1-28:

- (1) No biasing is required if the reference clock signals are generated from a clock source that conforms to the PCIe specification.
(2) Select values as recommended by the PCIe clock source vendor.

Transceiver Channel Datapath Clocking

Channel datapath clocking varies with channel configuration options and PCS configurations. This section describes the clock distribution from the left PLLs for transceiver channels and the datapath clocking in various supported configurations.

Table 1-7 lists the clocks generated by the PLLs for transceiver datapath.

Table 1-7. PLL Clocks for Transceiver Datapath

Clock	Usage
CDR clocks	Receiver CDR unit
High-speed clock	Transmitter serializer block in PMA
Low-speed clock	Transmitter PCS blocks Receiver PCS blocks when rate match FIFO enabled

When the byte serializer is enabled, the low-speed clock frequency is halved before feeding into the read clock of TX phase compensation FIFO. The low-speed clock is available in the FPGA fabric as `tx_clkout` port, which can be used in the FPGA fabric to send transmitter data and control signals.

Figure 1-33. Transmitter Only Datapath Clocking in Non-Bonded Channel Configuration

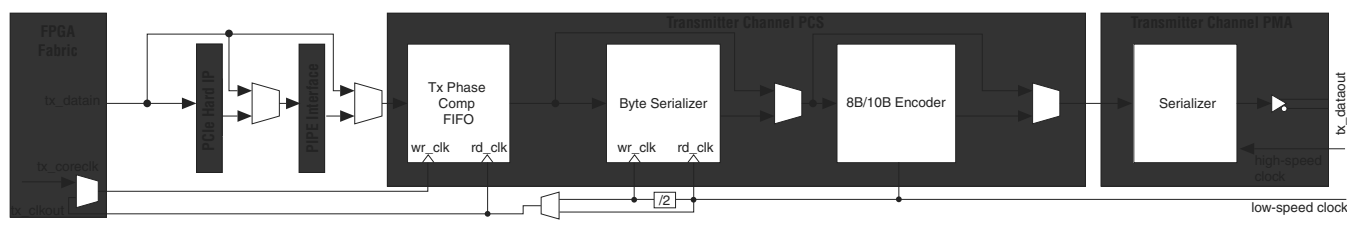
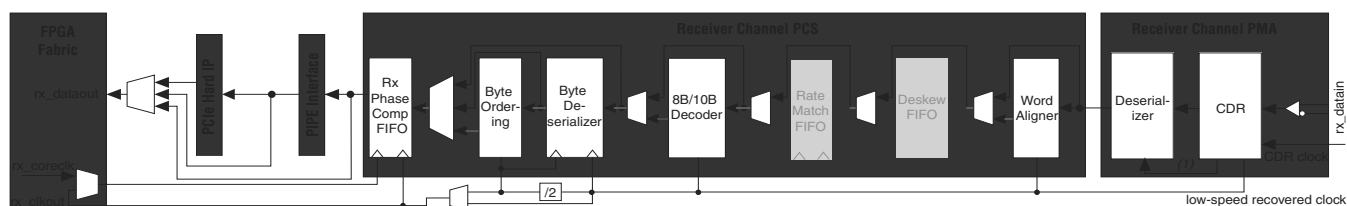


Figure 1-34 shows the datapath clocking in receiver only operation. In this mode, the receiver PCS supports configuration without the rate match FIFO. The CDR unit in the channel recovers the clock from the received serial data and generates the high-speed recovered clock for the deserializer, and low-speed recovered clock for forwarding to the receiver PCS. The low-speed recovered clock feeds to the following blocks in the receiver PCS:

- word aligner
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the low-speed recovered clock frequency is halved before feeding into the write clock of the RX phase compensation FIFO. The low-speed recovered clock is available in the FPGA fabric as `rx_clkout` port, which can be used in the FPGA fabric to capture receiver data and status signals.

Figure 1-34. Receiver Only Datapath Clocking without Rate Match FIFO in Non-Bonded Channel Configuration



Note to Figure 1-34:

- (1) High-speed recovered clock.

When the transceiver is configured for transmitter and receiver operation in non-bonded channel configuration, the receiver PCS supports configuration with and without the rate match FIFO. The difference is only at the receiver datapath clocking. The transmitter datapath clocking is identical to transmitter only operation mode as shown in Figure 1-33.

Signal Detect at Receiver

In PIPE mode, signal detection is supported with the built-in signal threshold detection circuitry. When electrical idle inference is not enabled, the `rx_signaldetect` signal is inverted and available as `pipeelecidle` port in the PIPE interface.

Lane Synchronization

In PIPE mode, the word aligner is configured in automatic synchronization state machine mode that complies with the PCIe specification. Table 1–16 lists the synchronization state machine parameters that implement the PCIe-compliant synchronization.

Table 1–16. Synchronization State Machine Parameters ⁽¹⁾

Parameter	Value
Number of valid synchronization (/K28.5/) code groups received to achieve synchronization	4
Number of erroneous code groups received to lose synchronization	17
Number of continuous good code groups received to reduce the error count by one	16

Note to Table 1–16:

(1) The word aligner supports 10-bit pattern lengths in PIPE mode.

Clock Rate Compensation

In PIPE mode, the rate match FIFO compensates up to ± 300 ppm (600 ppm total) difference between the upstream transmitter and the local receiver reference clock. In PIPE mode, the rate match FIFO operation is compliant to the version 2.0 of the PCIe Base Specification. The PCIe protocol requires the receiver to recognize a skip (SKP) ordered set, and inserts or deletes only one SKP symbol per SKP ordered set received to prevent the rate match FIFO from overflowing or underflowing. The SKP ordered set is a /K28.5/ comma (COM) symbol followed by one to five consecutive /K28.0/ SKP symbols, which are sent by transmitter during the inter-packet gap.

The rate match operation begins after the synchronization state machine in the word aligner indicates synchronization is acquired, as indicated with logic high on `rx_syncstatus` signal. Rate match FIFO insertion and deletion events are communicated to FPGA fabric on the `pipestatus[2..0]` port from each channel.

Low-Latency Synchronous PCIe

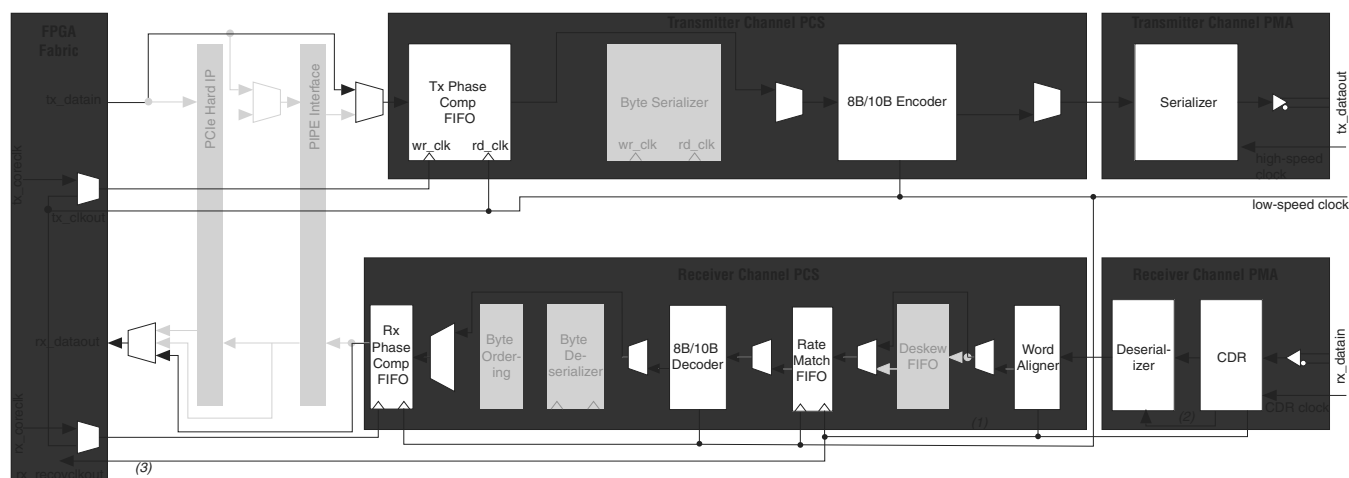
In PIPE mode, the Cyclone IV GX transceiver supports a lower latency in synchronous PCIe by reducing the latency across the rate match FIFO. In synchronous PCIe, the system uses a common reference clocking that gives a 0 ppm difference between the upstream transmitter's and local receiver's reference clock.



When using common reference clocking, the transceiver supports spread-spectrum clocking. For more information about the SSC support in PCIe Express (PIPE) mode, refer to the *Cyclone IV Device Data Sheet*.

Figure 1-55 shows the transceiver channel datapath and clocking when configured in GIGE mode.

Figure 1-55. Transceiver Channel Datapath and Clocking when Configured in GIGE Mode

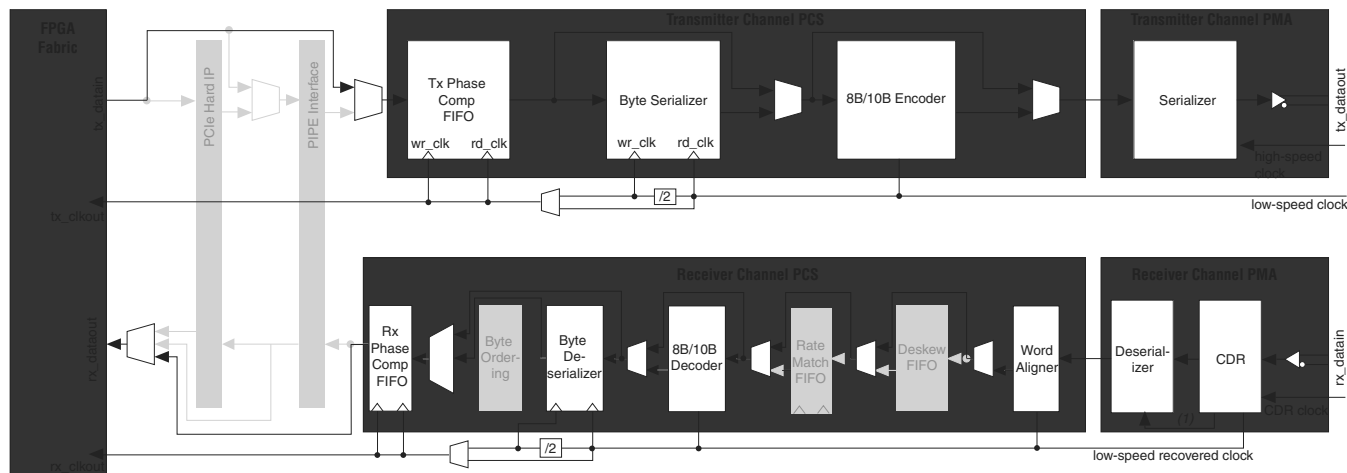


Notes to Figure 1-55:

- (1) Low-speed recovered clock.
- (2) High-speed recovered clock.
- (3) Optional rx_recovclkout port from CDR low-speed recovered clock is available for applications such as Synchronous Ethernet.

Figure 1-66 shows the transceiver channel datapath and clocking when configured in deterministic latency mode.

Figure 1-66. Transceiver Channel Datapath and Clocking when Configured in Deterministic Latency Mode



Note to Figure 1-66:

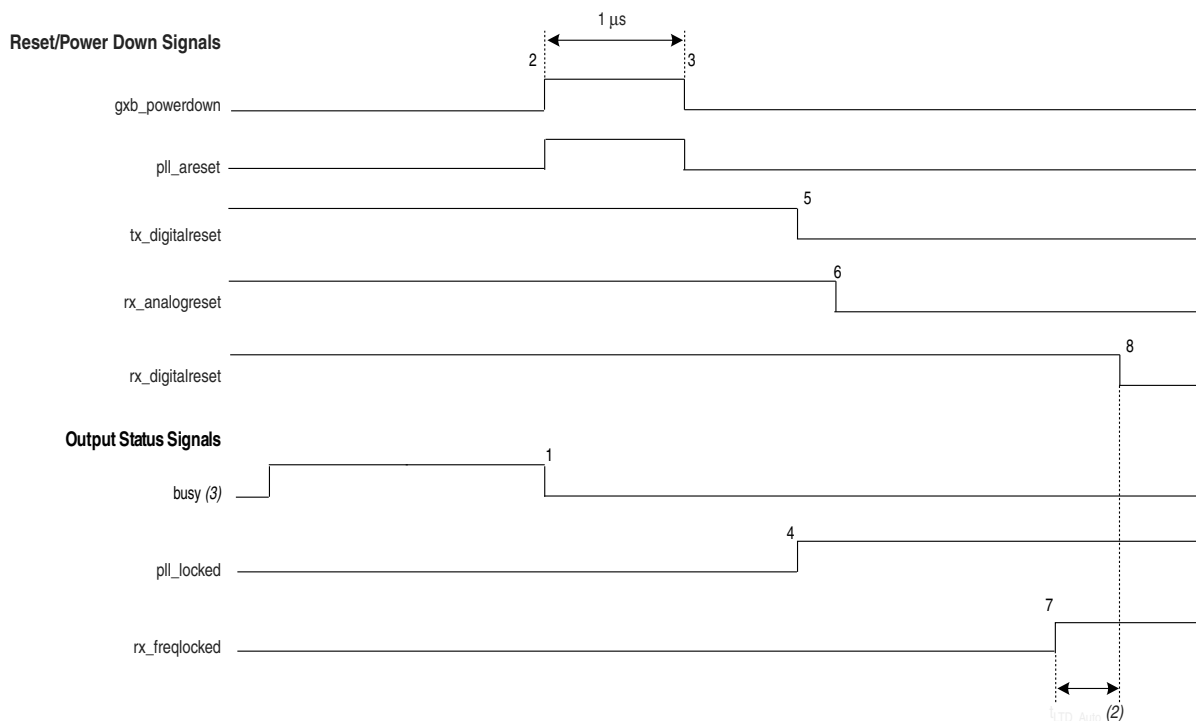
- (1) High-speed recovered clock.

Table 1–27. Receiver Ports in ALTGX Megafunction for Cyclone IV GX (Part 3 of 3)

Block	Port Name	Input/ Output	Clock Domain	Description
RX PCS	rx_coreclk	Output	Clock signal	Optional read clock port for the RX phase compensation FIFO.
	rx_phase_comp_fifo_error	Output	Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes)	RX phase compensation FIFO full or empty indicator. ■ A high level indicates FIFO is either full or empty.
	rx_bitslipboundaryselectout	Output	Asynchronous signal.	Indicate the number of bits slipped in the word aligner configured in manual alignment mode. ■ Values range from 0 to 9.
RX PMA	rx_datain	Input	N/A	Receiver serial data input port.
	rx_freqlocked	Output	Asynchronous signal	Receiver CDR lock state indicator ■ A high level indicates the CDR is in LTD state. ■ A low level indicates the CDR is in LTR state.
	rx_locktodata	Input	Asynchronous signal	Receiver CDR LTD state control signal ■ A high level forces the CDR to LTD state ■ When deasserted, the receiver CDR lock state depends on the rx_locktorefclk signal level.
	rx_locktorefclk	Input	Asynchronous signal	Receiver CDR LTR state control signal. ■ The rx_locktorefclk and rx_locktodata signals control whether the receiver CDR states as follows: [rx_locktodata:rx_locktorefclk] ■ 2'b00—receiver CDR is in automatic lock mode ■ 2b'01—receiver CDR is in manual lock mode (LTR state) ■ 2b'1x—receiver CDR is in manual lock mode (LTD state)
	rx_signaldetect	Output	Asynchronous signal	Signal threshold detect indicator. ■ Available in Basic mode when 8B/10B encoder/decoder is used, and in PIPE mode. ■ A high level indicates that the signal present at the receiver input buffer is above the programmed signal detection threshold value.
	rx_recovclkout	Output	Clock signal	CDR low-speed recovered clock ■ Only available in the GIGE mode for applications such as Synchronous Ethernet.

The deassertion of the busy signal indicates proper completion of the offset cancellation process on the receiver channel.

Figure 2–13. Sample Reset Sequence of a Receiver and Transmitter Channels-Receiver CDR in Automatic Lock Mode with the Optional gxb_powerdown Signal ⁽¹⁾



Notes to Figure 2–13:

- (1) The gxb_powerdown signal must not be asserted during the offset cancellation sequence.
- (2) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.
- (3) The busy signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the busy signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

Simulation Requirements

The following are simulation requirements:

- The gxb_powerdown port is optional. In simulation, if the gxb_powerdown port is not instantiated, you must assert the tx_digitalreset, rx_digitalreset, and rx_analogreset signals appropriately for correct simulation behavior.
- If the gxb_powerdown port is instantiated, and the other reset signals are not used, you must assert the gxb_powerdown signal for at least 1 μ s for correct simulation behavior.
- You can deassert the rx_digitalreset signal immediately after the rx_freqlocked signal goes high to reduce the simulation run time. It is not necessary to wait for t_{LTD_Auto} (as suggested in the actual reset sequence).
- The busy signal is deasserted after about 20 parallel reconfig_clk clock cycles in order to reduce simulation run time. For silicon behavior in hardware, you can follow the reset sequences described in the previous pages.

Table 3–3. Cyclone IV GX Supported Dynamic Reconfiguration Mode (Part 2 of 2)

Dynamic Reconfiguration Supported Mode	Operational Mode			Quartus II Instances			.mif Requirements
	Transmitter Only	Receiver Only	Transmitter and Receiver Only	ALTGX	ALTGX_ RECONFIG	ALTPLL_ RECONFIG	
Channel Reconfiguration							
Channel Interface	✓	✓	✓	✓	✓	—	✓
Data Rate Division in Receiver Channel	—	✓	✓	✓	✓	—	✓
PLL Reconfiguration	✓	✓	✓	✓	—	✓	✓

The following modes are available for dynamically reconfiguring the Cyclone IV transceivers:

- “PMA Controls Reconfiguration Mode” on page 3–13
- “Transceiver Channel Reconfiguration Mode” on page 3–21
 - Channel interface (.mif based)
 - Data rate division in receiver channel (.mif based)

The following sections describe each of these modes in detail.

The following modes are unsupported for dynamic reconfiguration:

- Dynamically enable/disable PRBS or BIST
- Switch between a receiver-only channel and a transmitter-only channel
- Switch between a ×1 mode to a bonded ×4 mode

PMA Controls Reconfiguration Mode

You can dynamically reconfigure the following PMA controls for all supported transceiver configurations channels as configured in the ALTGX instances:

- Pre-emphasis settings
- Equalization settings (channel reconfiguration mode does not support equalization settings)
- DC gain settings
- V_{OD} settings

You can use the analog reconfiguration feature to dynamically reconfigure the transceivers channels setting in either the transmitter or the receivers in the PMA blocks. You can update the PMA controls on-the-fly based on the desired input. You can perform both read and write transaction separately for this analog reconfiguration mode.

Read Transaction

If you want to read the existing values from a specific channel connected to the ALTGX_RECONFIG instance, observe the corresponding byte positions of the PMA control output port after the read transaction is completed.

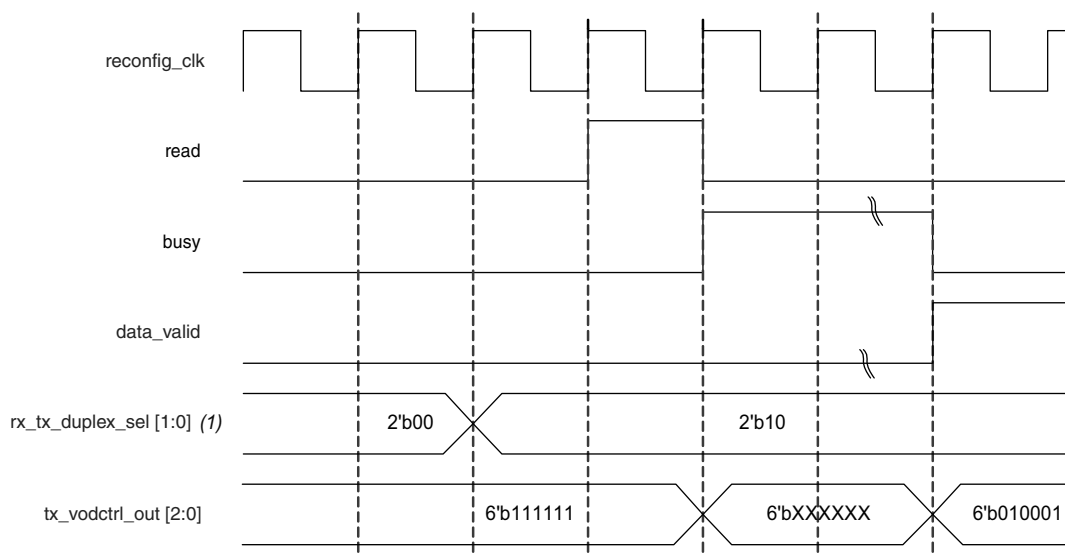
For example, if the number of channels controlled by the ALTGX_RECONFIG is two, the tx_vodctrl_out is 6 bits wide. The tx_vodctrl_out[2:0] signal corresponds to channel 1 and the tx_vodctrl_out[5:3] signal corresponds to channel 2.

To complete a read transaction to the V_{OD} values of the second channel, perform the following steps:

1. Before you initiate a read transaction, set the rx_tx_duplex_sel port to 2'b10 so that only the transmit PMA controls are read from the transceiver channel.
2. Ensure that the busy signal is low before you start a read transaction.
3. Assert the read signal for one reconfig_clk clock cycle. This initiates the read transaction.
4. The busy output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy reading the PMA control settings.
5. When the read transaction has completed, the busy signal goes low. The data_valid signal is asserted, indicating that the data available at the read control signal is valid.
6. To read the current V_{OD} values in channel 2, observe the values in tx_vodctrl_out[5:3].

In the waveform example shown in Figure 3-7, the transmit V_{OD} settings written in channels 1 and 2 prior to the read transaction are 3'b001 and 3'b010, respectively.

Figure 3-7. Read Transaction Waveform—Use the same control signal for all the channels Option Enabled



Note to Figure 3-7:

- (1) In this waveform example, you want to read from only the transmitter portion of all the channels.



Simultaneous write and read transactions are not allowed.

Table 3-5. rx_dataoutfull[31..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions (Part 3 of 3)

FPGA Fabric-Transceiver Channel Interface Description	Receive Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)
20-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 10 bits	Two 10-bit Data (rx_dataout) rx_dataoutfull[9:0] - rx_dataout (LSByte) and rx_dataoutfull[25:16] - rx_dataout (MSByte)
	Two Receiver Sync Status Bits rx_dataoutfull[10] - rx_syncstatus (LSB) and rx_dataoutfull[26] - rx_syncstatus (MSB)
	rx_dataoutfull[11] and rx_dataoutfull[27]: 8B/10B disparity error indicator (rx_disperr)
	Two Receiver Pattern Detect Bits rx_dataoutfull[12] - rx_patterndetect (LSB) and rx_dataoutfull[28] - rx_patterndetect (MSB)
	rx_dataoutfull[13] and rx_dataoutfull[29]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes
	rx_dataoutfull[14] and rx_dataoutfull[30]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes
	rx_dataoutfull[15] and rx_dataoutfull[31]: 8B/10B running disparity indicator (rx_runningdisp)

Data Rate Reconfiguration Mode Using RX Local Divider

The RX local divider resides in the RX PMA block for every channels. This is a hardware feature where a /2 divider is available in each of the receiver channel for the supported device. You can use this RX local divider to reconfigure the data rate at the receiver channel. This can be used for protocols such as SDI that has data rates in divisions of 2.

By using this RX local divider, you can support two different data rates without using additional transceiver PLLs. This dynamic reconfiguration mode is available only for the receiver and not applicable to the transmitter. This reconfiguration mode using the RX local divider (/2) is only supported and available in EP4CGX30 (F484 package), EP4CGX50, and EP4CGX75 devices.



For more information about this RX local divider, refer to the *Cyclone IV GX Transceiver Architecture* chapter.


 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration

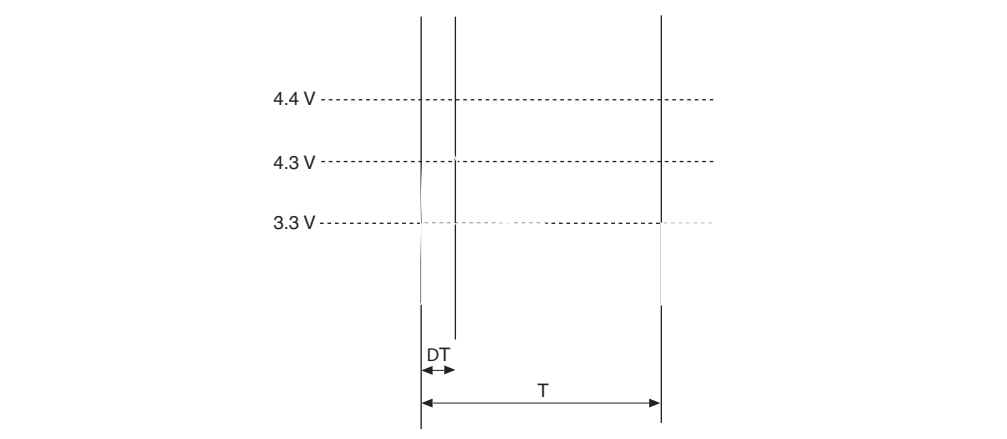


Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1–42:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Notes to Table 1–43:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.