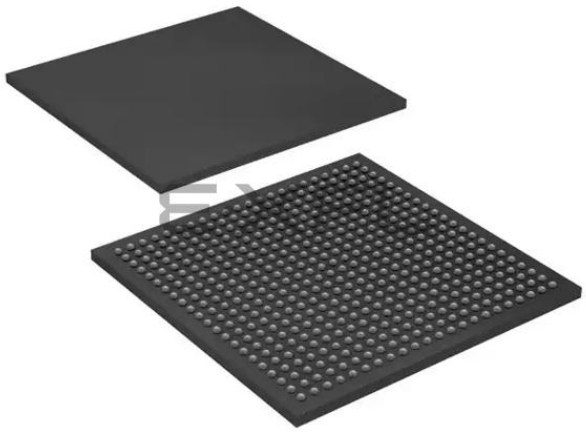

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

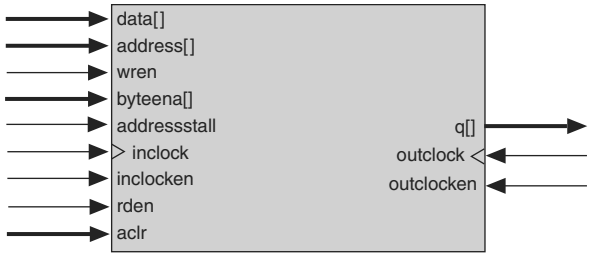
Details	
Product Status	Active
Number of LABs/CLBs	7155
Number of Logic Elements/Cells	114480
Total RAM Bits	3981312
Number of I/O	280
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce115f23c7

☞ Violating the setup or hold time on the M9K memory block input registers may corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations from a single address. Figure 3–6 shows the single-port memory configuration for Cyclone IV devices M9K memory blocks.

Figure 3–6. Single-Port Memory (1), (2)



Notes to Figure 3–6:

(1) You can implement two single-port memory blocks in a single M9K block.
(2) For more information, refer to "Packed Mode Support" on page 3–4.

During a write operation, the behavior of the RAM outputs is configurable. If you activate `rden` during a write operation, the RAM outputs show either the new data being written or the old data at that address. If you perform a write operation with `rden` deactivated, the RAM outputs retain the values they held during the most recent active `rden` signal.

To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about read-during-write mode, refer to "Read-During-Write Operations" on page 3–15.

The port width configurations for M9K blocks in single-port mode are as follow:

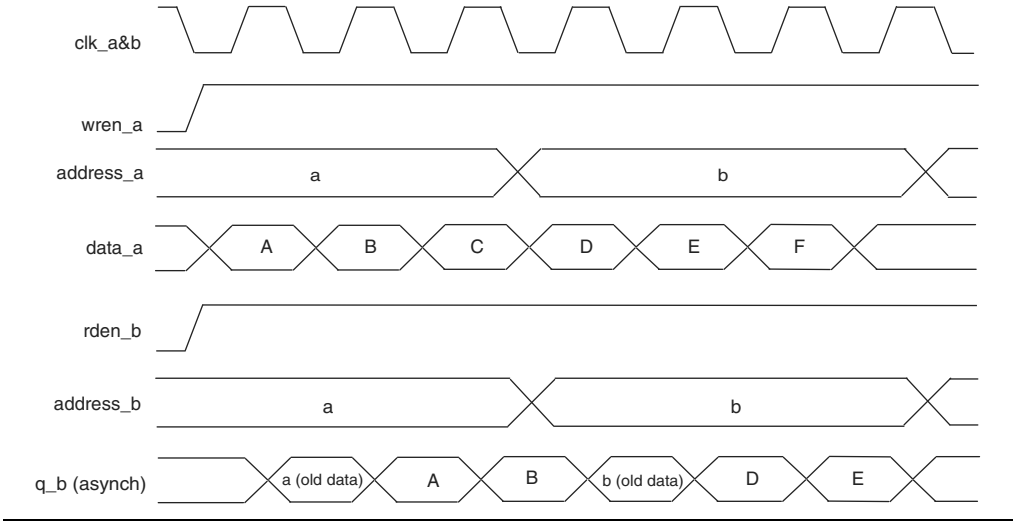
- 8192 × 1
- 4096 × 2
- 2048 × 4
- 1024 × 8
- 1024 × 9
- 512 × 16
- 512 × 18
- 256 × 32
- 256 × 36

In this mode, you also have two output choices: **Old Data** mode or **Don't Care** mode. In **Old Data** mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In **Don't Care** mode, the same operation results in a "Don't Care" or unknown value on the RAM outputs.

For more information about how to implement the desired behavior, refer to the *RAM Megafunction User Guide*.

Figure 3–16 shows a sample functional waveform of mixed port read-during-write behavior for **Old Data** mode. In **Don't Care** mode, the old data is replaced with "Don't Care".

Figure 3–16. Mixed Port Read-During-Write: Old Data Mode



For mixed-port read-during-write operation with dual clocks, the relationship between the clocks determines the output behavior of the memory. If you use the same clock for the two clocks, the output is the old data from the address location. However, if you use different clocks, the output is unknown during the mixed-port read-during-write operation. This unknown value may be the old or new data at the address location, depending on whether the read happens before or after the write.

Conflict Resolution

When you are using M9K memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Because there is no conflict resolution circuitry built into M9K memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict-resolution logic external to the M9K memory block.

Power-Up Conditions and Memory Initialization

The M9K memory block outputs of Cyclone IV devices power up to zero (cleared) regardless of whether the output registers are used or bypassed. All M9K memory blocks support initialization using a **.mif**. You can create **.mif**s in the Quartus II software and specify their use using the RAM MegaWizard Plug-In Manager when instantiating memory in your design. Even if memory is pre-initialized (for example, using a **.mif**), it still powers up with its outputs cleared. Only the subsequent read after power up outputs the pre-initialized values.

For more information about **.mif**s, refer to the *RAM Megafunction User Guide* and the *Quartus II Handbook*.

Power Management

The M9K memory block clock enables of Cyclone IV devices allow you to control clocking of each M9K memory block to reduce AC power consumption. Use the `rden` signal to ensure that read operations only occur when necessary. If your design does not require read-during-write, reduce power consumption by deasserting the `rden` signal during write operations or any period when there are no memory operations. The Quartus II software automatically powers down any unused M9K memory blocks to save static power.

Document Revision History

Table 3–6 shows the revision history for this chapter.

Table 3–6. Document Revision History

Date	Version	Changes
November 2011	1.1	Updated the “Byte Enable Support” section.
November 2009	1.0	Initial release.

Deterministic Latency Compensation Mode

The deterministic latency mode compensates for the delay of the multipurpose PLLs through the clock network and serializer in Common Public Radio Interface (CPRI) applications. In this mode, the PLL PFD feedback path compensates the latency uncertainty in `Tx dataout` and `Tx clkout` paths relative to the reference clock.

Hardware Features

Cyclone IV PLLs support several features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase shifting implementations, and programmable duty cycles.

Clock Multiplication and Division

Each Cyclone IV PLL provides clock synthesis for PLL output ports using M/(N*post-scale counter) scaling factors. The input clock is divided by a pre-scale factor, N, and is then multiplied by the M feedback factor. The control loop drives the VCO to match f_{IN} (M/N). Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO value is the least common multiple of the output frequencies that meets its frequency specifications. For example, if output frequencies required from one PLL are 33 and 66 MHz, the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz in the VCO range). Then, the post-scale counters scale down the VCO frequency for each output port.

There is one pre-scale counter, N, and one multiply counter, M, per PLL, with a range of 1 to 512 for both M and N. The N counter does not use duty cycle control because the purpose of this counter is only to calculate frequency division. There are five generic post-scale counters per PLL that can feed GCLKs or external clock outputs. These post-scale counters range from 1 to 512 with a 50% duty cycle setting. The post-scale counters range from 1 to 256 with any non-50% duty cycle setting. The sum of the high/low count values chosen for a design selects the divide value for a given counter.

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the ALTPLL megafunction.

Phase alignment between output counters is determined using the t_{PLL_PSERR} specification.

Document Revision History

Table 5–14 lists the revision history for this chapter.

Table 5–14. Document Revision History

Date	Version	Changes
October 2012	2.4	■ Updated “Manual Override” and “PLL Cascading” sections. ■ Updated Figure 5–9.
November 2011	2.3	■ Updated the “Dynamic Phase Shifting” section. ■ Updated Figure 5–26.
December 2010	2.2	■ Updated for the Quartus II software version 10.1 release. ■ Updated Figure 5–3 and Figure 5–10. ■ Updated “GCLK Network Clock Source Generation”, “PLLs in Cyclone IV Devices”, and “Manual Override” sections. ■ Minor text edits.
July 2010	2.1	■ Updated Figure 5–2, Figure 5–3, Figure 5–4, and Figure 5–10. ■ Updated Table 5–1, Table 5–2, and Table 5–5. ■ Updated “Clock Feedback Modes” section.
February 2010	2.0	■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release. ■ Updated “Clock Networks” section. ■ Updated Table 5–1 and Table 5–2. ■ Added Table 5–3. ■ Updated Figure 5–2, Figure 5–3, and Figure 5–9. ■ Added Figure 5–4 and Figure 5–10.
November 2009	1.0	Initial release.

Table 6–2 on page 6–7 shows the possible settings for I/O standards with current strength control. These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for IOH and IOL of the corresponding I/O standard.

☞ When you use programmable current strength, on-chip series termination (R_S OCT) is not available.

Slew Rate Control

The output buffer for each Cyclone IV I/O pin provides optional programmable output slew-rate control. Table 6–2 on page 6–7 shows the possible slew rate option and the Quartus II default slew rate setting. However, these fast transitions may introduce noise transients in the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Because each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength of 8 mA or higher.

☞ You cannot use the programmable slew rate feature when using OCT with calibration.

☞ You cannot use the programmable slew rate feature when using the 3.0-V PCI, 3.0-V PCI-X, 3.3-V LVTTL, or 3.3-V LVCMOS I/O standards. Only the fast slew rate (default) setting is available.

Open-Drain Output

Cyclone IV devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that are asserted by multiple devices in your system.

Bus Hold

Each Cyclone IV device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

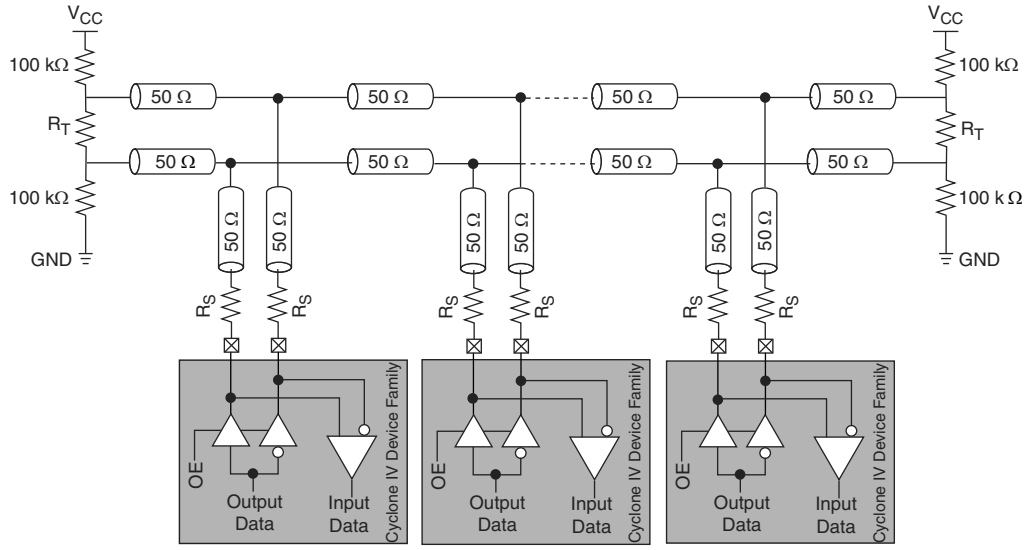
The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

☞ If you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on dedicated clock pins.

Bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Figure 6–14 shows a typical BLVDS topology with multiple transmitter and receiver pairs.

Figure 6–14. BLVDS Topology with Cyclone IV Devices Transmitters and Receivers



The BLVDS I/O standard is supported on the top, bottom, and right I/O banks of Cyclone IV devices. The BLVDS transmitter uses two single-ended output buffers with the second output buffer programmed as inverted, while the BLVDS receiver uses a true LVDS input buffer. The transmitter and receiver share the same pins. An output-enabled (OE) signal is required to tristate the output buffers when the LVDS input buffer receives a signal.

For more information, refer to the *Cyclone IV Device Datasheet* chapter.

Designing with BLVDS

The BLVDS bidirectional communication requires termination at both ends of the bus in BLVDS. The termination resistor (R_T) must match the bus differential impedance, which in turn depends on the loading on the bus. Increasing the load decreases the bus differential impedance. With termination at both ends of the bus, termination is not required between the two signals at the input buffer. A single series resistor (R_S) is required at the output buffer to match the output buffer impedance to the transmission line impedance. However, this series resistor affects the voltage swing at the input buffer. The maximum data rate achievable depends on many factors.

Altera recommends that you perform simulation using the IBIS model while considering factors such as bus loading, termination values, and output and input buffer location on the bus to ensure that the required performance is achieved.

For more information about BLVDS interface support in Altera devices, refer to *AN 522: Implementing Bus LVDS Interface in Supported Altera Device Families*.

Differential SSTL I/O Standard Support in Cyclone IV Devices

The differential SSTL I/O standard is a memory-bus standard used for applications such as high-speed DDR SDRAM interfaces. Cyclone IV devices support differential SSTL-2 and SSTL-18 I/O standards. The differential SSTL output standard is only supported at PLL#_CLKOUT pins using two single-ended SSTL output buffers (PLL#_CLKOUTp and PLL#_CLKOUTn), with the second output programmed to have opposite polarity. The differential SSTL input standard is supported on the GCLK pins only, treating differential inputs as two single-ended SSTL and only decoding one of them.

The differential SSTL I/O standard requires two differential inputs with an external reference voltage (VREF) as well as an external termination voltage (VTT) of 0.5 × V_{CCIO} to which termination resistors are connected.

For differential SSTL electrical specifications, refer to "Differential I/O Standard Termination" on page 6–15 and the *Cyclone IV Device Datasheet* chapter.

Figure 6–8 on page 6–15 shows the differential SSTL Class I and Class II interface.

Differential HSTL I/O Standard Support in Cyclone IV Devices

The differential HSTL I/O standard is used for the applications designed to operate in 0 V to 1.2 V, 0 V to 1.5 V, or 0 V to 1.8 V HSTL logic switching range. Cyclone IV devices support differential HSTL-18, HSTL-15, and HSTL-12 I/O standards. The differential HSTL input standard is available on GCLK pins only, treating the differential inputs as two single-ended HSTL and only decoding one of them. The differential HSTL output standard is only supported at the PLL#_CLKOUT pins using two single-ended HSTL output buffers (PLL#_CLKOUT*p* and PLL#_CLKOUT*n*), with the second output programmed to have opposite polarity.

The differential HSTL I/O standard requires two differential inputs with an external reference voltage (VREF), as well as an external termination voltage (VTT) of 0.5 × V_{CCIO} to which termination resistors are connected.

For differential HSTL signaling characteristics, refer to "Differential I/O Standard Termination" on page 6–15 and the *Cyclone IV Device Datasheet* chapter.

Figure 6–7 on page 6–15 shows the differential HSTL Class I and Class II interface.

True Differential Output Buffer Feature

Cyclone IV devices true differential transmitters offer programmable pre-emphasis—you can turn it on or off. The default setting is on.

Programmable Pre-Emphasis

The programmable pre-emphasis boosts the high frequencies of the output signal to compensate the frequency-dependant attenuation of the transmission line to maximize the data eye opening at the far-end receiver. Without pre-emphasis, the output current is limited by the V_{OD} specification and the output impedance of the transmitter. At high frequency, the slew rate may not be fast enough to reach full V_{OD}

There are no series resistors required in AP configuration mode for Cyclone IV E devices when using the Micron flash at 2.5-, 3.0-, and 3.3-V I/O standard. The output buffer of the Micron P30 IBIS model does not overshoot above 4.1 V. Thus, series resistors are not required for the 2.5-, 3.0-, and 3.3-V AP configuration option. However, if there are any other devices sharing the same flash I/Os with Cyclone IV E devices, all shared pins are still subject to the 4.1-V limit and may require series resistors.

Default read mode of the supported parallel flash memory and all writes to the parallel flash memory are asynchronous. Both the parallel flash families support a synchronous read mode, with data supplied on the positive edge of DCLK.

The serial clock (DCLK) generated by Cyclone IV E devices controls the entire configuration cycle and provides timing for the parallel interface.

Multi-Device AP Configuration

You can configure multiple Cyclone IV E devices using a single parallel flash. You can cascade multiple Cyclone IV E devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone IV E device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, DATA[15..8], and DATA[7..0] pins of each device in the chain are connected (Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27).

The first Cyclone IV E device in the chain, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27, is the configuration master device and controls the configuration of the entire chain. You must connect its MSEL pins to select the AP configuration scheme. The remaining Cyclone IV E devices are used as configuration slaves. You must connect their MSEL pins to select the FPP configuration scheme. Any other Altera device that supports FPP configuration can also be part of the chain as a configuration slave.

The following are the configurations for the DATA[15..0] bus in a multi-device AP configuration:

- Byte-wide multi-device AP configuration
- Word-wide multi-device AP configuration

The **.rbf** used by the JRunner software driver cannot be a compressed **.rbf** because the JRunner software driver uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information about the JRunner software driver, refer to *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website at (www.altera.com).

Combining JTAG and AS Configuration Schemes

You can combine the AS configuration scheme with the JTAG-based configuration (Figure 8–28). This setup uses two 10-pin download cable headers on the board. One download cable is used in JTAG mode to configure the Cyclone IV device directly through the JTAG interface. The other download cable is used in AS mode to program the serial configuration device in-system through the AS programming interface. If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration terminates.

Programming Serial Configuration Devices In-System with the JTAG Interface

Cyclone IV devices in a single- or multiple-device chain support in-system programming of a serial configuration device with the JTAG interface through the SFL design. The intelligent host or download cable of the board can use the four JTAG pins on the Cyclone IV device to program the serial configuration device in system, even if the host or download cable cannot access the configuration pins (DCLK, DATA, ASDI, and nCS pins).

The SFL design is a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the Cyclone IV device that uses their JTAG interface to access the EPCS JTAG Indirect Configuration Device Programming (**.jic**) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the SFL design.

In a multiple device chain, you must only configure the master device that controls the serial configuration device. Slave devices in the multiple device chain that are configured by the serial configuration device do not have to be configured when using this feature. To successfully use this feature, set the MSEL pins of the master device to select the AS configuration scheme (Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9). The serial configuration device in-system programming through the Cyclone IV device JTAG interface has three stages, which are described in the following sections:

- "Loading the SFL Design"
- "ISP of the Configuration Device" on page 8–56
- "Reconfiguration" on page 8–57

Loading the SFL Design

The SFL design is a design inside the Cyclone IV device that bridges the JTAG interface and AS interface with glue logic.

The intelligent host uses the JTAG interface to configure the master device with a SFL design. The SFL design allows the master device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and active-low chip select (nCS) pins.

Table 1–27. Receiver Ports in ALTGX Megafunction for Cyclone IV GX (Part 1 of 3)

Block	Port Name	Input/ Output	Clock Domain	Description
RX PCS	rx_syncstatus	Output	Synchronous to `tx_clkout` (non-bonded modes with rate match FIFO), `rx_clkout` (non-bonded modes without rate match FIFO), `coreclkout` (bonded modes), or `rx_coreclk` (when using the optional `rx_coreclk` input)	Word alignment synchronization status indicator. This signal passes through the RX Phase Compensation FIFO. ■ Not available in bit-slip mode
	rx_patternde tect	Output	Synchronous to `tx_clkout` (non-bonded modes with rate match FIFO), `rx_clkout` (non-bonded modes without rate match FIFO), `coreclkout` (bonded modes), or `rx_coreclk` (when using the optional `rx_coreclk` input)	Indicates when the word alignment logic detects the alignment pattern in the current word boundary. This signal passes through the RX Phase Compensation FIFO.
	rx_bitslip	Input	Asynchronous signal. Minimum pulse width is two parallel clock cycles.	Bit-slip control for the word aligner configured in bit-slip mode. ■ At every rising edge, word aligner slips one bit into the received data stream, effectively shifting the word boundary by one bit.
	rx_rlv	Output	Asynchronous signal. Driven for a minimum of two recovered clock cycles in configurations without byte serializer and a minimum of three recovered clock cycles in configurations with byte serializer.	Run-length violation indicator. ■ A high pulse indicates that the number of consecutive 1s or 0s in the received data stream exceeds the programmed run length violation threshold.
	rx_invpolarity	Input	Asynchronous signal. Minimum pulse width is two parallel clock cycles.	Generic receiver polarity inversion control. ■ A high level to invert the polarity of every bit of the 8- or 10-bit data to the word aligner.
	rx_enapattern align	Input	Asynchronous signal.	Controls the word aligner operation configured in manual alignment mode.
	rx_rmfifodata inserted	Output	Synchronous to `tx_clkout` (non-bonded modes) or `coreclkout` (bonded modes)	Rate match FIFO insertion status indicator. ■ A high level indicates the rate match pattern byte is inserted to compensate for the ppm difference in the reference clock frequencies between the upstream transmitter and the local receiver.
	rx_rmfifodata deleted	Output	Synchronous to `tx_clkout` (non-bonded modes) or `coreclkout` (bonded modes)	Rate match FIFO deletion status indicator. ■ A high level indicates the rate match pattern byte is deleted to compensate for the ppm difference in the reference clock frequencies between the upstream transmitter and the local receiver.

Table 3–1. Glossary of Terms Used in this Chapter (Part 2 of 2)

Term	Description
Memory Initialization File, also known as **.mif**	A file with the **.mif** extension will be generated for **.mif**-based reconfiguration mode. It can be either in Channel Reconfiguration mode or PLL Reconfiguration mode. ■ Channel Reconfiguration mode—this file contains information about the various ALTGX MegaWizard Plug-In Manager options that you set. Each word in the **.mif** is 16 bits wide. The dynamic reconfiguration controller writes information from the **.mif** into the transceiver channel. ■ PLL Reconfiguration mode—this file contains information about the various PLL parameters and settings that you use to configure the transceiver PLL to different output frequency. The **.mif** file is 144 × 1-bit size. During PLL reconfiguration mode, the PLL reconfiguration controller shifts these 144-bit serially into the transceiver PLL.
PMA controls	Represents **analog controls** (**Voltage Output Differential** [V_{OD}], **Pre-emphasis**, **DC Gain**, and **Manual Equalization**) as displayed in both the ALTGX and ALTGX_RECONFIG MegaWizard Plug-In Managers.
Transceiver channel	Refers to a transmitter channel, a receiver channel, or a duplex channel that has both PMA and PCS blocks.

Dynamic Reconfiguration Controller Architecture

The dynamic reconfiguration controller is a soft intellectual property (IP) that utilizes FPGA-fabric resources. You can use only one controller per transceiver block. You cannot use the dynamic reconfiguration controller to control multiple Cyclone IV devices or any off-chip interfaces.

Table 3–2. Dynamic Reconfiguration Controller Port List (ALTGX_RECONFIG Instance) (Part 4 of 7)

<table>
<tr><th>Port Name</th><th>Input/ Output</th><th>Description</th></tr>
<tr><td colspan="3">Analog Settings Control/Status Signals</td></tr>
<tr><td>tx_vodctrl[2..0] (1)</td><td>Input</td><td>This is an optional transmit buffer V_{OD} control signal. It is 3 bits per transmitter channel. The number of settings varies based on the transmit buffer supply setting and the termination resistor setting on the TX Analog screen of the ALTGX MegaWizard Plug-In Manager.

The width of this signal is fixed to 3 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Use same control signal for all the channels option in the Analog controls screen. Otherwise, the width of this signal is 3 bits per channel.

The following shows the V_{OD} values corresponding to the tx_vodctrl settings for 100-Ω termination.

For more information, refer to the “Programmable Output Differential Voltage” section of the Cyclone IV GX Device Datasheet chapter.
<table>
<tr><th>tx_vodctrl[2:0]</th><th>Corresponding ALTGX instance settings</th><th>Corresponding V_{OD} settings (mV)</th></tr>
<tr><td>3’b001</td><td>1</td><td>400</td></tr>
<tr><td>3’b010</td><td>2</td><td>600</td></tr>
<tr><td>3’b011</td><td>3</td><td>800</td></tr>
<tr><td>3’b111</td><td>4 (2)</td><td>900 (2)</td></tr>
<tr><td>3’b100</td><td>5</td><td>1000</td></tr>
<tr><td>3’b101</td><td>6</td><td>1200</td></tr>
<tr><td colspan="3">All other values => N/A</td></tr>
</table>
</td></tr>
</table>

There are three methods that you can use to dynamically reconfigure the PMA controls of a transceiver channel:

- "Method 1: Using logical_channel_address to Reconfigure Specific Transceiver Channels" on page 3–14
- "Method 2: Writing the Same Control Signals to Control All the Transceiver Channels" on page 3–16
- "Method 3: Writing Different Control Signals for all the Transceiver Channels at the Same Time" on page 3–19

Method 1: Using logical_channel_address to Reconfigure Specific Transceiver Channels

Enable the `logical_channel_address` port by selecting the **Use 'logical_channel_address' port** option on the **Analog controls** tab. This method is applicable only for a design where the dynamic reconfiguration controller controls more than one channel.

You can additionally reconfigure either the receiver portion, transmitter portion, or both the receiver and transmitter portions of the transceiver channel by setting the corresponding value on the `rx_tx_duplex_sel` input port. For more information, refer to Table 3–2 on page 3–4.

Connecting the PMA Control Ports

The selected PMA control ports remain fixed in width, regardless of the number of channels controlled by the ALTGX_RECONFIG instance:

- `tx_vodctrl` and `tx_vodctrl_out` are fixed to 3 bits
- `tx_preemp` and `tx_preemp_out` are fixed to 5 bits
- `rx_eqdcgain` and `rx_eqdcgain_out` are fixed to 2 bits
- `rx_eqctrl` and `rx_eqctrl_out` are fixed to 4 bits

Write Transaction

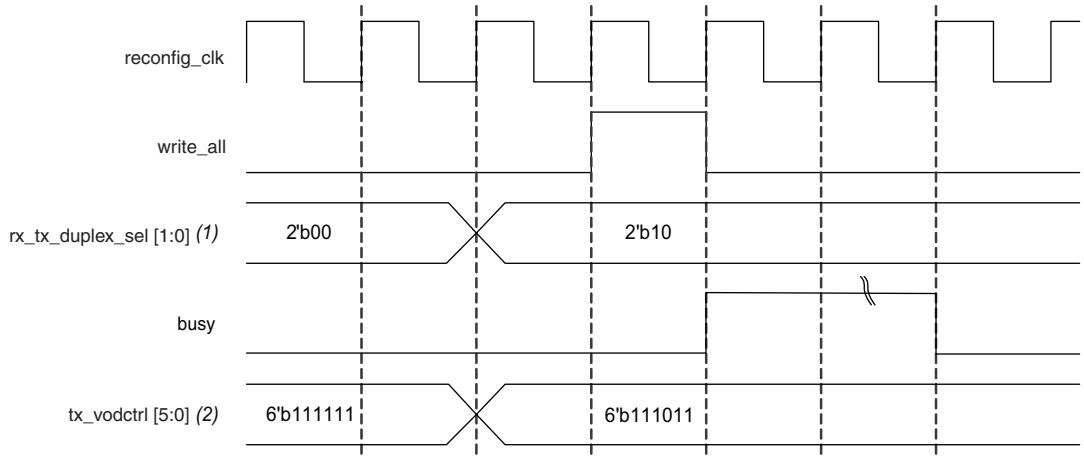
To complete a write transaction, perform the following steps:

1. Set the selected PMA control ports to the desired settings (for example, `tx_vodctrl` = **3'b001**).
2. Set the `logical_channel_address` input port to the logical channel address of the transceiver channel whose PMA controls you want to reconfigure.
3. Set the `rx_tx_duplex_sel` port to **2'b10** so that only the transmit PMA controls are written to the transceiver channel.
4. Ensure that the `busy` signal is low before you start a write transaction.
5. Assert the `write_all` signal for one `reconfig_clk` clock cycle.

The `busy` output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy writing the PMA control values. When the write transaction has completed, the `busy` signal goes low.

Figure 3–8 shows a write transaction waveform with the **Use the same control signal for all the channels** option disabled.

Figure 3–8. Write Transaction Waveform—Use the same control signal for all the channels Option Disabled



Notes to Figure 3–8:

(1) In this waveform example, you want to write to only the transmitter portion of the channel.

(2) In this waveform example, the number of channels controlled by the dynamic reconfiguration controller (the ALTGX_RECONFIG instance) is two and that the `tx_vodctrl` control port is enabled.

☞ Simultaneous write and read transactions are not allowed.

Read Transaction

The read transaction in Method 3 is identical to that in Method 2. Refer to "Read Transaction" on page 3–18.

☞ This is the slowest method. You have to write all the PMA settings for all channels even if you may only be changing one parameter on the channel. Altera recommends using the `logical_channel_address` method for time-critical applications.

For each method, you can additionally reconfigure the PMA setting of both transmitter and receiver portion, transmitter portion only, or receiver portion only of the transceiver channel. For more information, refer to "Dynamic Reconfiguration Controller Port List" on page 3–4. You can enable the `rx_tx_duplex_sel` port by selecting the **Use 'rx_tx_duplex_sel' port to enable RX only, TX only or duplex reconfiguration** option on the **Error checks** tab of the ALTGX_RECONFIG MegaWizard Plug-In Manager.

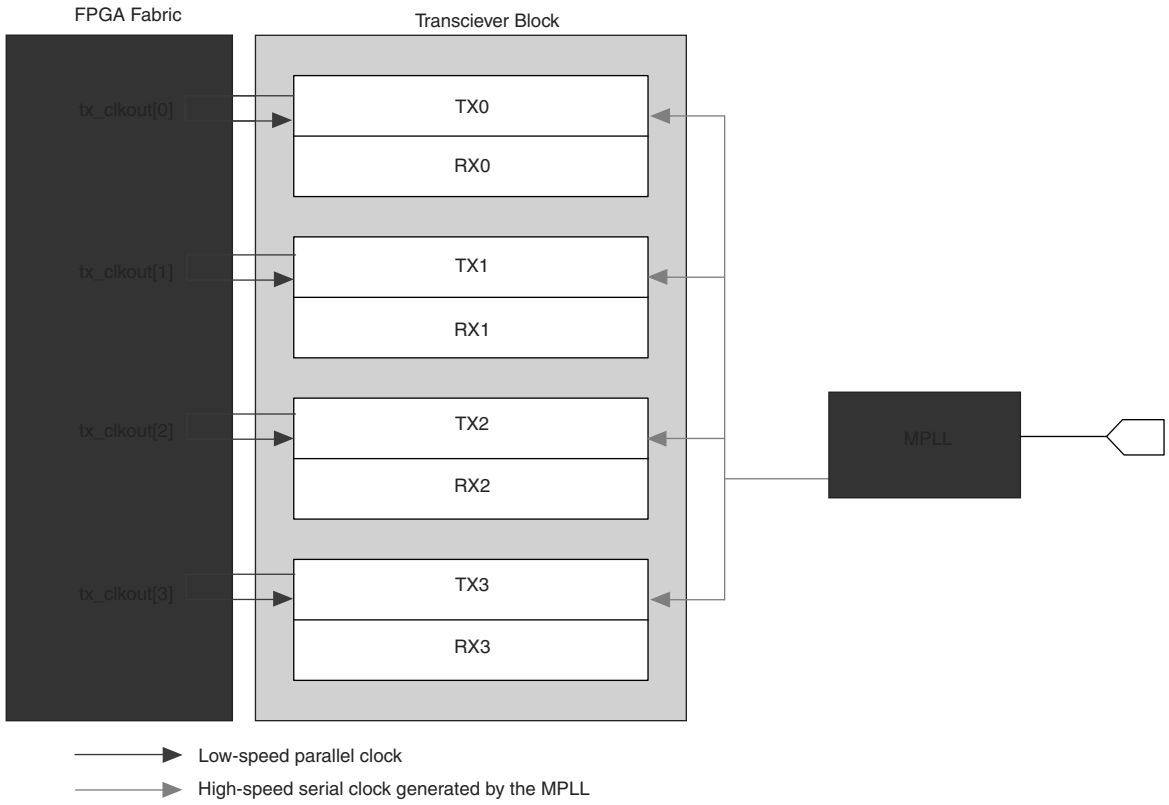
Figure 3–9 shows the ALTGX_RECONFIG connection to the ALTGX instances when set in analog reconfiguration mode. For the port information, refer to the "Dynamic Reconfiguration Controller Port List" on page 3–4.

Option 2: Use the Respective Channel Transmitter Core Clocks

- Enable this option if you want the individual transmitter channel `tx_clkout` signals to provide the write clock to their respective Transmit Phase Compensation FIFOs.
- This option is typically enabled when each transceiver channel is reconfigured to a different functional mode using channel reconfiguration.

Figure 3–12 shows how each transmitter channel's `tx_clkout` signal provides a clock to the Transmit Phase Compensation FIFOs of the respective transceiver channels.

Figure 3–12. Option 2 for Transmitter Core Clocking (Channel Reconfiguration Mode)



Receiver core clocking refers to the clock that is used to read the parallel data from the Receiver Phase Compensation FIFO into the FPGA fabric. You can use one of the following clocks to read from the Receive Phase Compensation FIFO:

- `rx_coreclk`—you can use a clock of the same frequency as `rx_clkout` from the FPGA fabric to provide the read clock to the Receive Phase Compensation FIFO. If you use `rx_coreclk`, it overrides the `rx_clkout` options in the ALTGX MegaWizard Plug-In Manager.
- `rx_clkout`—the Quartus II software automatically routes `rx_clkout` to the FPGA fabric and back into the Receive Phase Compensation FIFO.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Signal detect/loss threshold	PIPE mode	65	—	175	65	—	175	65	—	175	mV
t_{LTR} *(10)*	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR-LTD\_Manual}$ *(11)*	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD} *(12)*	—	0	100	4000	0	100	4000	0	100	4000	ns
t_{LTD_Manual} *(13)*	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} *(14)*	—	—	—	4000	—	—	4000	—	—	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	—	—	17000	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package)	—	600	—	3125	600	—	3125	600	—	2500	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA	Compliant									—
Rise time	—	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	—	—	—	120	—	—	120	—	—	120	ps