



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	7155
Number of Logic Elements/Cells	114480
Total RAM Bits	3981312
Number of I/O	280
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce115f23c8l

Cyclone IV Device Family Architecture

This section describes Cyclone IV device architecture and contains the following topics:

- “FPGA Core Fabric”
- “I/O Features”
- “Clock Management”
- “External Memory Interfaces”
- “Configuration”
- “High-Speed Transceivers (Cyclone IV GX Devices Only)”
- “Hard IP for PCI Express (Cyclone IV GX Devices Only)”

FPGA Core Fabric

Cyclone IV devices leverage the same core fabric as the very successful Cyclone series devices. The fabric consists of LEs, made of 4-input look up tables (LUTs), memory blocks, and multipliers.

Each Cyclone IV device M9K memory block provides 9 Kbits of embedded SRAM memory. You can configure the M9K blocks as single port, simple dual port, or true dual port RAM, as well as FIFO buffers or ROM. They can also be configured to implement any of the data widths in Table 1–7.

Table 1–7. M9K Block Data Widths for Cyclone IV Device Family

Mode	Data Width Configurations
Single port or simple dual port	×1, ×2, ×4, ×8/9, ×16/18, and ×32/36
True dual port	×1, ×2, ×4, ×8/9, and ×16/18

The multiplier architecture in Cyclone IV devices is the same as in the existing Cyclone series devices. The embedded multiplier blocks can implement an 18×18 or two 9×9 multipliers in a single block. Altera offers a complete suite of DSP IP including finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions for use with the multiplier blocks. The Quartus® II design software’s DSP Builder tool integrates MathWorks Simulink and MATLAB design environments for a streamlined DSP design flow.



For more information, refer to the *Logic Elements and Logic Array Blocks in Cyclone IV Devices*, *Memory Blocks in Cyclone IV Devices*, and *Embedded Multipliers in Cyclone IV Devices* chapters.

Logic Array Blocks

Logic array blocks (LABs) contain groups of LEs.

Topology

Each LAB consists of the following features:

- 16 LEs
- LAB control signals
- LE carry chains
- Register chains
- Local interconnect

The local interconnect transfers signals between LEs in the same LAB. Register chain connections transfer the output of one LE register to the adjacent LE register in an LAB. The Quartus II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local and register chain connections for performance and area efficiency.

Figure 2-4 shows the LAB structure for Cyclone IV devices.

Figure 2-4. Cyclone IV Device LAB Structure

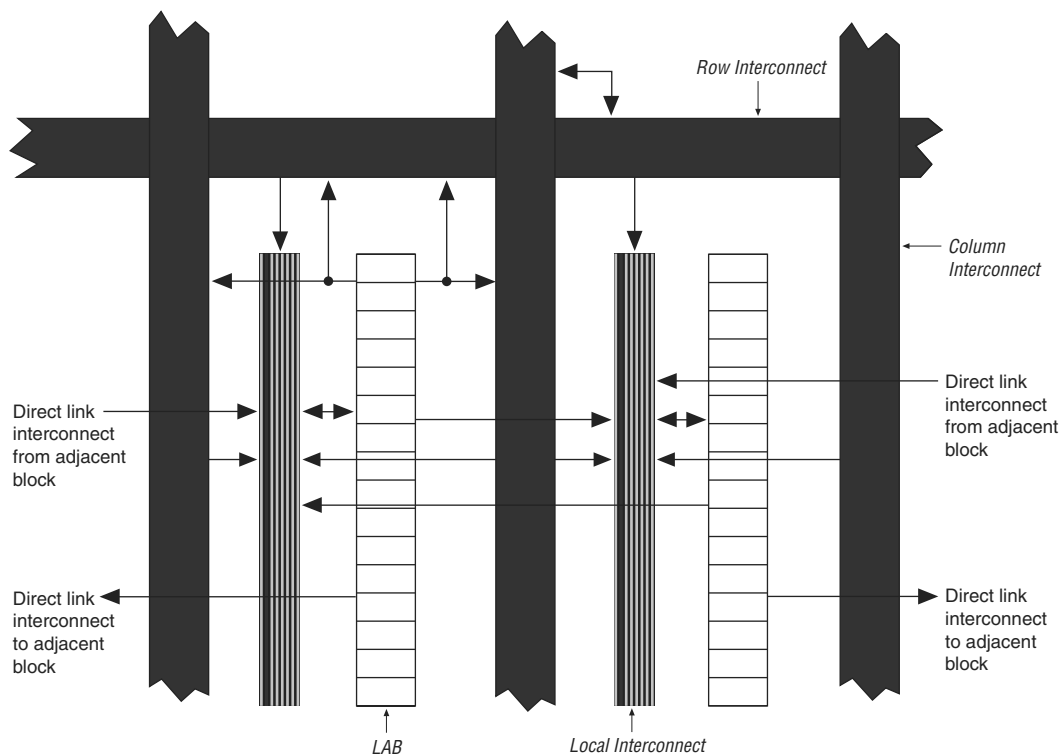
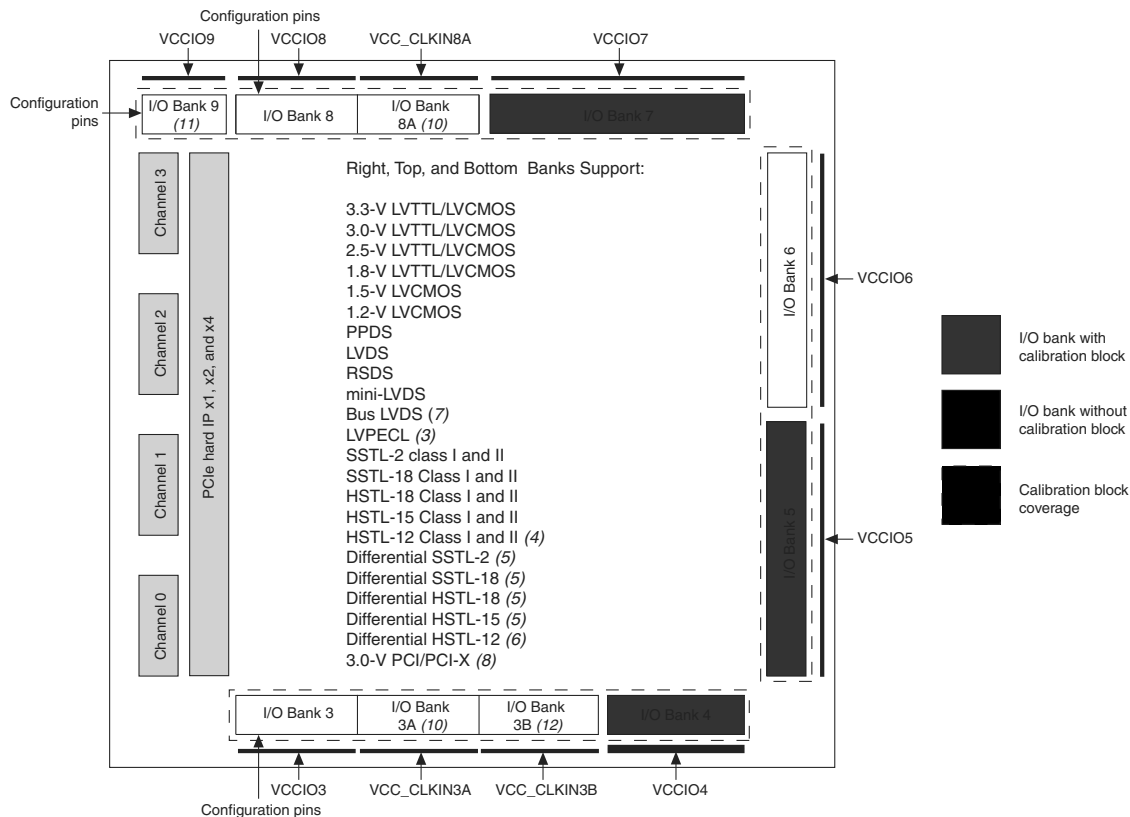


Figure 6–10 and Figure 6–11 show the overview of Cyclone IV GX I/O banks.

Figure 6–10. Cyclone IV GX I/O Banks for EP4CGX15, EP4CGX22, and EP4CGX30 (1), (2), (9)

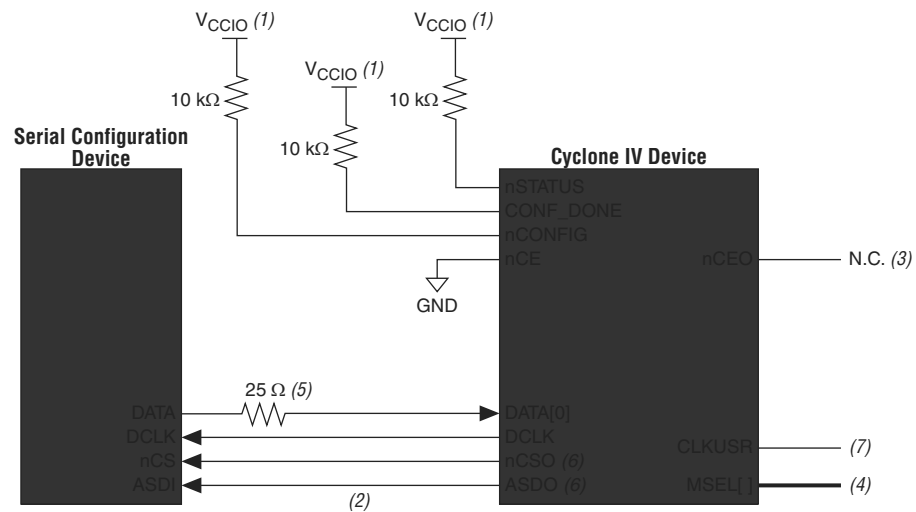


Notes to Figure 6–10:

- (1) This is a top view of the silicon die. For exact pin locations, refer to the pin list and the Quartus II software. Channels 2 and 3 are not available in EP4CGX15 and F169 package type in EP4CGX22 and EP4CGX30 devices.
- (2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 5 and 6 only. External resistors are needed for the differential outputs in column I/O banks.
- (3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
- (4) The HSTL-12 Class II is supported in column I/O banks 4, 7, and 8.
- (5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.
- (6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 4, 7, and 8.
- (7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses the LVDS input buffer.
- (8) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.
- (9) The OCT block is located in the shaded banks 4, 5, and 7.
- (10) There are two dedicated clock input I/O banks (I/O bank 3A and I/O bank 8A) that can be used for either high-speed serial interface (HSSI) input reference clock pins or clock input pins.
- (11) There are dual-purpose I/O pins in bank 9. If input pins with V_{REF} I/O standards are used on these dual-purpose I/O pins during user mode, they share the V_{REF} pin in bank 8. These dual-purpose I/O pins in bank 9 when used in user mode also support R_S OCT without calibration and they share the OCT block with bank 8.
- (12) There are four dedicated clock input in I/O bank 3B for the EP4CGX30F484 device that can be used for either HSSI input reference clock pins or clock input pins.


This four-pin interface connects to Cyclone IV device pins, as shown in Figure 8-2.


Figure 8-2. Single-Device AS Configuration



Notes to Figure 8-2:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Cyclone IV devices use the ASDO-to-ASDI path to control the configuration device.
- (3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8-3 on page 8-8, Table 8-4 on page 8-8, and Table 8-5 on page 8-9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) Connect the series resistor at the near end of the serial configuration device.
- (6) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as the DATA[1] pin in AP and FPP modes.
- (7) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

 To tri-state the configuration bus for AS configuration schemes, you must tie nCE high and nCONFIG low.

 The 25-Ω resistor at the near end of the serial configuration device for DATA[0] works to minimize the driver impedance mismatch with the board trace and reduce the overshoot seen at the Cyclone IV device DATA[0] input pin.

In the single-device AS configuration, the maximum board loading and board trace length between the supported serial configuration device and the Cyclone IV device must follow the recommendations in Table 8-7 on page 8-18.

The DCLK generated by the Cyclone IV device controls the entire configuration cycle and provides timing for the serial interface. Cyclone IV devices use an internal oscillator or an external clock source to generate the DCLK. For Cyclone IV E devices, you can use a 40-MHz internal oscillator to generate the DCLK and for Cyclone IV GX devices you can use a slow clock (20 MHz maximum) or a fast clock (40 MHz maximum) from the internal oscillator or an external clock from CLKUSR to generate the DCLK. There are some variations in the internal oscillator frequency because of the process, voltage, and temperature (PVT) conditions in Cyclone IV

During device configuration, Cyclone IV E devices read configuration data using the parallel interface and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where an external host controls the interface.

AP Configuration Supported Flash Memories

The AP configuration controller in Cyclone IV E devices is designed to interface with two industry-standard flash families—the Micron P30 Parallel NOR flash family and the Micron P33 Parallel NOR flash family. Unlike serial configuration devices, both of the flash families supported in AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash after entering user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Micron P30 flash family and the P33 flash family support a continuous synchronous burst read mode at 40 MHz DCLK frequency for reading data from the flash. Additionally, the Micron P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.



Cyclone IV E devices use a 40-MHz oscillator for the AP configuration scheme. The oscillator is the same oscillator used in the Cyclone IV E AS configuration scheme.

Table 8–10 lists the supported families of the commodity parallel flash for the AP configuration scheme.

Table 8–10. Supported Commodity Flash for AP Configuration Scheme for Cyclone IV E Devices ⁽¹⁾

Flash Memory Density	Micron P30 Flash Family ⁽²⁾	Micron P33 Flash Family ⁽³⁾
64 Mbit	✓	✓
128 Mbit	✓	✓
256 Mbit	✓	✓

Notes to Table 8–10:


- (1) The AP configuration scheme only supports flash memory speed grades of 40 MHz and above.
- (2) 3.3-, 3.0-, 2.5-, and 1.8-V I/O options are supported for the Micron P30 flash family.
- (3) 3.3-, 3.0- and 2.5-V I/O options are supported for the Micron P33 flash family.

Configuring Cyclone IV E devices from the Micron P30 and P33 family 512-Mbit flash memory is possible, but you must properly drive the extra address and FLASH_nCE pins as required by these flash memories.



To check for supported speed grades and package options, refer to the respective flash datasheets.

The AP configuration scheme in Cyclone IV E devices supports flash speed grades of 40 MHz and above. However, AP configuration for all these speed grades must be capped at 40 MHz. The advantage of faster speed grades is realized when your design in the Cyclone IV E devices accesses flash memory in user mode.

 JTAG configuration allows an unlimited number of Cyclone IV devices to be cascaded in a JTAG chain.


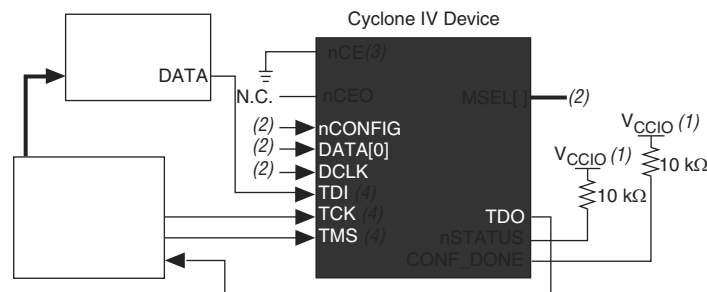
 For more information about configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera FPGA Chains* chapter in volume 2 of the *Configuration Handbook*.

Figure 8-27 shows JTAG configuration with a Cyclone IV device and a microprocessor.

Figure 8-27. JTAG Configuration of a Single Device Using a Microprocessor




Notes to Figure 8-27:

- (1) You must connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.
- (3) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into TDI, TMS, and TCK must fit the maximum overshoot outlined in Equation 8-1 on page 8-5.

Configuring Cyclone IV Devices with Jam STAPL

Jam™ STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

 For more information about JTAG and Jam STAPL in embedded environments, refer to *AN 425: Using Command-Line Jam STAPL Solution for Device Programming*. To download the Jam Player, visit the Altera website (www.altera.com).

Configuring Cyclone IV Devices with the JRunner Software Driver

The JRunner software driver allows you to configure Cyclone IV devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The supported programming input file is in .rbf format. The JRunner software driver also requires a Chain Description File (.cdf) generated by the Quartus II software. The JRunner software driver is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

Table 8-20. Dedicated Configuration Pins on the Cyclone IV Device (Part 2 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	<ul style="list-style-type: none"> Status output—the target Cyclone IV device drives the CONF_DONE pin low before and during configuration. After all the configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input—after all the data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. <p>Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect bus holds or ADC to CONF_DONE pin.</p>
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the Cyclone IV device with a low signal to allow configuration. You must hold nCE pin low during configuration, initialization, and user-mode. In a single-device configuration, you must tie the nCE pin low. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. You must hold the nCE pin low for successful JTAG programming of the device.
nCEO	N/A if option is on. I/O if option is off.	All	Output open-drain	<p>Output that drives low when configuration is complete. In a single-device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In a multi-device configuration, this pin feeds the nCE pin of the next device. The nCEO of the last device in the chain is left floating or used as a user I/O pin after configuration.</p> <p>If you use the nCEO pin to feed the nCE pin of the next device, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor.</p> <p>If you use the nCEO pin as a user I/O pin after configuration, set the state of the pin on the Dual-Purpose Pin settings.</p>
nCSO, FLASH_nCE (1)	I/O	AS, AP (2)	Output	<p>Output control signal from the Cyclone IV device to the serial configuration device in AS mode that enables the configuration device. This pin functions as nCSO in AS mode and FLASH_nCE in AP mode.</p> <p>Output control signal from the Cyclone IV device to the parallel flash in AP mode that enables the flash. Connects to the CE# pin on the Micron P30 or P33 flash. (2)</p> <p>This pin has an internal pull-up resistor that is always active.</p>

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

- Chapter 1. Cyclone IV Transceivers Architecture
Revised: *February 2015*
Part Number: *CYIV-52001-3.7*
- Chapter 2. Cyclone IV Reset Control and Power Down
Revised: *September 2014*
Part Number: *CYIV-52002-1.4*
- Chapter 3. Cyclone IV Dynamic Reconfiguration
Revised: *November 2011*
Part Number: *CYIV-52003-2.1*

- Programmable equalization—boosts the high-frequency gain of the incoming signal up to 7 dB. This compensates for the low-pass filter effects of the transmission media. The amount of high-frequency gain required depends on the loss characteristics of the physical medium.
- Programmable DC gain—provides equal boost to incoming signal across the frequency spectrum with DC gain settings up to 6 dB.
- Programmable differential OCT—provides calibrated OCT at 100 Ω or 150 Ω with on-chip receiver common mode voltage at 0.82 V. The common mode voltage is tri-stated when you disable the OCT to use external termination.
- Offset cancellation—corrects the analog offset voltages that might exist from process variations between the positive and negative differential signals in the equalizer stage and CDR circuit.
- Signal detection—detects if the signal level present at the receiver input buffer is higher than the threshold with a built-in signal threshold detection circuitry. The circuitry has a hysteresis response that filters out any high-frequency ringing caused by ISI effects or high-frequency losses in the transmission medium. Detection is indicated by the assertion of the `rx_signaldetect` signal. Signal detection is only supported when 8B/10B encoder/decoder block is enabled. When not supported, the `rx_signaldetect` signal is forced high, bypassing the signal detection function.



Disable OCT to use external termination if the link requires a 85 Ω termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.



For specifications on programmable equalization and DC gain settings, refer to the *Cyclone IV Device Data Sheet*.

The byte ordering block operates in either word-alignment-based byte ordering or user-controlled byte ordering modes.

In word-alignment-based byte ordering mode, the byte ordering block starts looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary when it detects a rising edge on the rx_syncstatus signal. Whenever the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if the pad byte insertion is necessary. If the byte ordering block detects another rising edge on the rx_syncstatus signal from the word aligner, it deasserts the rx_byteorderalignstatus signal and repeats the byte ordering operation.

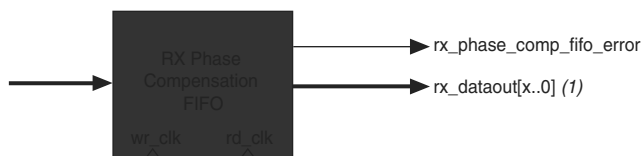
In user-controlled byte ordering mode, the byte ordering operation is user-triggered using rx_enabyteord port. A rising edge on rx_enabyteord port triggers the byte ordering block to start looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary. When the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if a pad byte insertion is necessary.

RX Phase Compensation FIFO

The RX phase compensation FIFO compensates for the phase difference between the parallel receiver clock and the FPGA fabric interface clock, when interfacing the receiver channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP blocks). The FIFO is four words deep, with latency between two to three parallel clock cycles.

Figure 1-24 shows the RX phase compensation FIFO block diagram.

Figure 1-24. RX Phase Compensation FIFO Block Diagram



Note to Figure 1-24:

(1) Parameter x refers to the transceiver channel width, where 8, 10, 16, or 20 bits are supported.

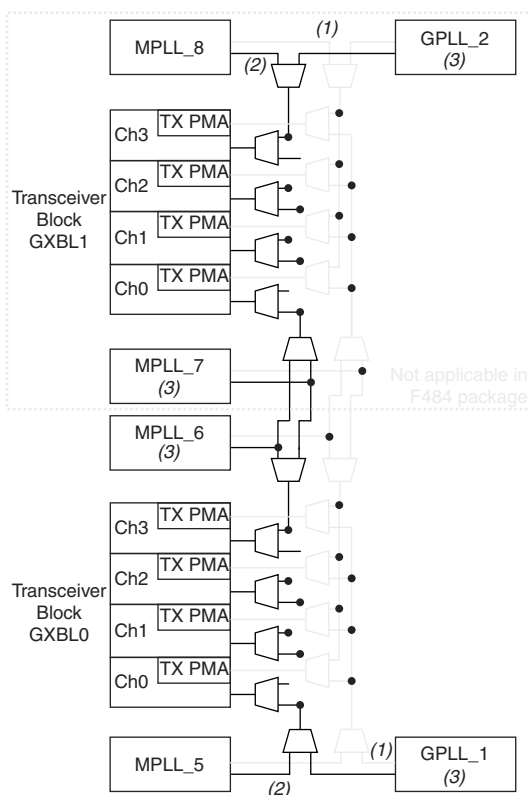


The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in the Deterministic Latency functional mode. For more information, refer to “Deterministic Latency Mode” on page 1-73. For more information about FIFO clocking, refer to “FPGA Fabric-Transceiver Interface Clocking” on page 1-43.

Miscellaneous Receiver PCS Feature

The receiver PCS supports the following additional feature:

- **Output bit-flip**—reverses the bit order at a byte level at the output of the receiver phase compensation FIFO. For example, if the 16-bit parallel receiver data at the output of the receiver phase compensation FIFO is '10111100 10101101' (16'hBCAD), enabling this option reverses the data on rx_dataout port to '00111101 10110101' (16'h3DB5).

Figure 1–32. Clock Distribution in Non-Bonded Channel Configuration for Transceivers in F484 and Larger Packages**Notes to Figure 1–32:**

- (1) High-speed clock.
- (2) Low-speed clock.
- (3) These PLLs have restricted clock driving capability and may not reach all connected channels. For details, refer to Table 1–9.

The transceiver datapath clocking varies in non-bonded channel configuration depending on the PCS configuration.

Figure 1–33 shows the datapath clocking in transmitter only operation. In this mode, each channel selects the high- and low-speed clock from one of the supported PLLs. The high-speed clock feeds to the serializer for parallel to serial operation. The low-speed clock feeds to the following blocks in the transmitter PCS:

- 8B/10B encoder
- read clock of the byte serializer
- read clock of the TX phase compensation FIFO

In configuration with rate match FIFO, the transmitter datapath clocking is identical to Transmitter Only operation as shown in Figure 1-38. In each bonded receiver channel, the CDR unit recovers the clock from serial received data and generates the high- and low-speed recovered clock for each bonded channel. The high-speed recovered clock feeds the channel's deserializer, and low-speed recovered clock is forwarded to receiver PCS. The individual low-speed recovered clock feeds to the following blocks in the receiver PCS:

- word aligner
- write clock of rate match FIFO

The common bonded low-speed clock that is used in all bonded transmitter PCS datapaths feeds the following blocks in each bonded receiver PCS:

- read clock of rate match FIFO
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the common bonded low-speed clock frequency is halved before feeding to the write clock of RX phase compensation FIFO. The common bonded low-speed clock is available in FPGA fabric as `coreclkout` port, which can be used in FPGA fabric to send transmitter data and control signals, and capture receiver data and status signals from the bonded channels.

FPGA Fabric-Transceiver Interface Clocking

The FPGA fabric-transceiver interface clocks consists of clock signals from the FPGA fabric to the transceiver blocks, and from the transceiver blocks to the FPGA fabric. These clock resources use the global clock networks (GCLK) in the FPGA core.



For information about the GCLK resources in the Cyclone IV GX devices, refer to *Clock Networks and PLLs in Cyclone IV Devices* chapter.

Table 1-11 lists the FPGA fabric-transceiver interface clocks.

Table 1-11. FPGA Fabric-Transceiver Interface Clocks (Part 1 of 2)

Clock Name	Clock Description	Interface Direction
tx_clkout	Phase compensation FIFO clock	Transceiver to FPGA fabric
rx_clkout	Phase compensation FIFO clock	Transceiver to FPGA fabric
coreclkout	Phase compensation FIFO clock	Transceiver to FPGA fabric
fixed_clk	125MHz receiver detect clock in PIPE mode	FPGA fabric to transceiver
reconfig_clk ^{(1), (2)}	Transceiver dynamic reconfiguration and offset cancellation clock	FPGA fabric to transceiver

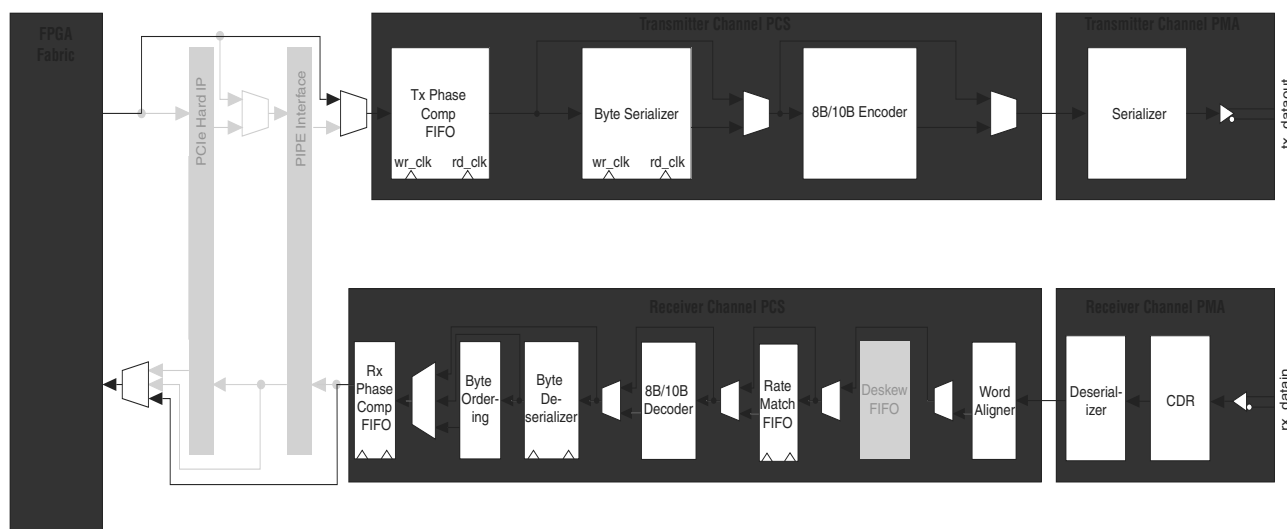
Table 1–14. Transceiver Functional Modes for Protocol Implementation (Part 2 of 2)

Functional Mode	Protocol	Key Feature	Reference
Deterministic Latency	Proprietary, CPRI, OBSAI	TX PLL phase frequency detector (PFD) feedback, registered mode FIFO, TX bit-slip control	“Deterministic Latency Mode” on page 1–73
SDI	SDI	High-speed SERDES, CDR	“SDI Mode” on page 1–76

Basic Mode

The Cyclone IV GX transceiver channel datapath is highly flexible in Basic mode to implement proprietary protocols. SATA, V-by-One, and Display Port protocol implementations in Cyclone IV GX transceiver are supported with Basic mode.

Figure 1–44 shows the transceiver channel datapath supported in Basic mode.

Figure 1–44. Transceiver Channel Datapath in Basic Mode

PIPE Interface

The PIPE interface provides a standard interface between the PCIe-compliant PHY and MAC layer as defined by the version 2.00 of the PIPE Architecture specification for Gen1 (2.5 Gbps) signaling rate. Any core or IP implementing the PHY MAC, data link, and transaction layers that supports PIPE 2.00 can be connected to the Cyclone IV GX transceiver configured in PIPE mode. Table 1–15 lists the PIPE-specific ports available from the Cyclone IV GX transceiver configured in PIPE mode and the corresponding port names in the PIPE 2.00 specification.

Table 1–15. Transceiver-FPGA Fabric Interface Ports in PIPE Mode

Transceiver Port Name	PIPE 2.00 Port Name
tx_datain[15..0] ⁽¹⁾	TxData[15..0]
tx_ctrlenable[1..0] ⁽¹⁾	TxDataK[1..0]
rx_dataout[15..0] ⁽¹⁾	RxData[15..0]
rx_ctrlldetect[1..0] ⁽¹⁾	RxDataK[1..0]
tx_detectrxloop	TxDetectRx/Loopback
tx_forceelecidle	TxElecIdle
tx_forcedispcompliance	TxCompliance
pipe8b10binvpolarity	RxPolarity
powerdn[1..0] ⁽²⁾	PowerDown[1..0]
pipedatavalid	RxValid
pipephydonestatus	PhyStatus
pipeelecidle	RxElecIdle
pipestatus	RxStatus[2..0]

Notes to Table 1–15:

- (1) When used with PCIe hard IP block, the byte SERDES is not used. In this case, the data ports are 8 bits wide and control identifier is 1 bit wide.
- (2) Cyclone IV GX transceivers do not implement power saving measures in lower power states (P0s, P1, and P2), except when putting the transmitter buffer in electrical idle in the lower power states.

Receiver Detection Circuitry

In PIPE mode, the transmitter supports receiver detection function with a built-in circuitry in the transmitter PMA. The PCIe protocol requires the transmitter to detect if a receiver is present at the far end of each lane as part of the link training and synchronization state machine sequence. This feature requires the following conditions:

- transmitter output buffer to be tri-stated
- have OCT utilization
- 125 MHz clock on the fixedclk port

The circuit works by sending a pulse on the common mode of the transmitter. If an active PCIe receiver is present at the far end, the time constant of the step voltage on the trace is higher compared to when the receiver is not present. The circuitry monitors the time constant of the step signal seen on the trace to decide if a receiver was detected.

Table 1-25. PRBS, High and Low Frequency Patterns, and Channel Settings (Part 2 of 2)

Patterns	Polynomial	8-bit Channel Width				10-bit Channel Width			
		Channel Width of 8 bits ⁽¹⁾	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	Channel Width of 10-bits ⁽¹⁾	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages
Low Frequency ⁽²⁾	1111100000	N	—	—	—	Y	—	2.5	3.125

Notes to Table 1-25:

- (1) Channel width refers to the **What is the channel width?** option in the **General** screen of the ALTGX MegaWizard Plug-In Manager. Based on the selection, an 8 or 10 bits wide pattern is generated as indicated by a **Yes (Y)** or **No (N)**.
- (2) A verifier and associated rx_bistdone and rx_bisterr signals are not available for the specified patterns.

You can enable the serial loopback option to loop the generated PRBS patterns to the receiver channel for verifier to check the PRBS patterns. When the PRBS pattern is received, the rx_bisterr and rx_bistdone signals indicate the status of the verifier. After the word aligner restores the word boundary, the rx_bistdone signal is driven high when the verifier receives a complete pattern cycle and remains asserted until it is reset using the rx_digitalreset port. After the assertion of rx_bistdone, the rx_bisterr signal is asserted for a minimum of three rx_clkout cycles when errors are detected in the data and deasserts if the following PRBS sequence contains no error. You can reset the PRBS pattern generator and verifier by asserting the tx_digitalreset and rx_digitalreset ports, respectively.


 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration

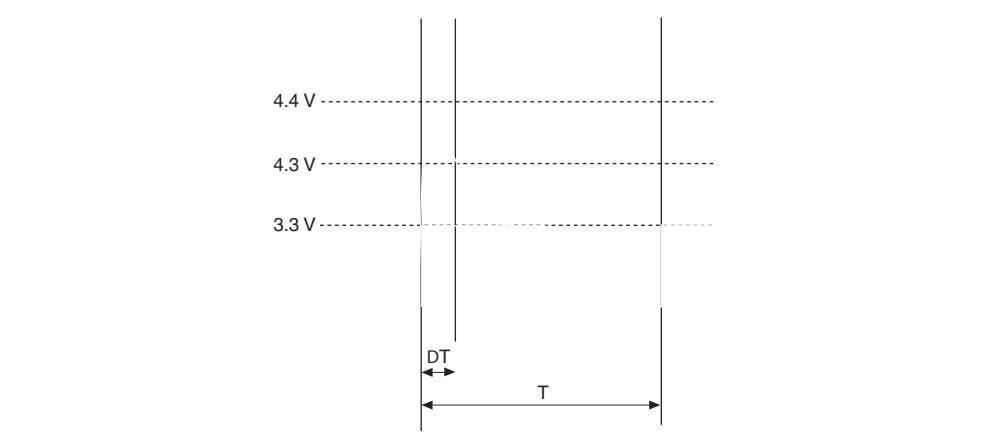


Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V _{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V _I	DC input voltage	—	–0.5	—	3.6	V
V _O	DC output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
t _{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁷⁾	50 µs	—	50 ms	—
		Fast POR ⁽⁸⁾	50 µs	—	3 ms	—
I _{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1–4:

- (1) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set V_{CC_CLKIN} to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.
- (6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1–5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V _{ESDHBM}	ESD voltage using the HBM (GPIOs) ⁽¹⁾	± 2000	V
	ESD using the HBM (HSSI I/Os) ⁽²⁾	± 1000	V
V _{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) ⁽²⁾	± 250	V

Notes to Table 1–5:

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.
- (2) This value is applicable only to Cyclone IV GX devices.

Figure 1-2 shows the lock time parameters in manual mode.


 LTD = lock-to-data. LTR = lock-to-reference.

Figure 1-2. Lock Time Parameters for Manual Mode

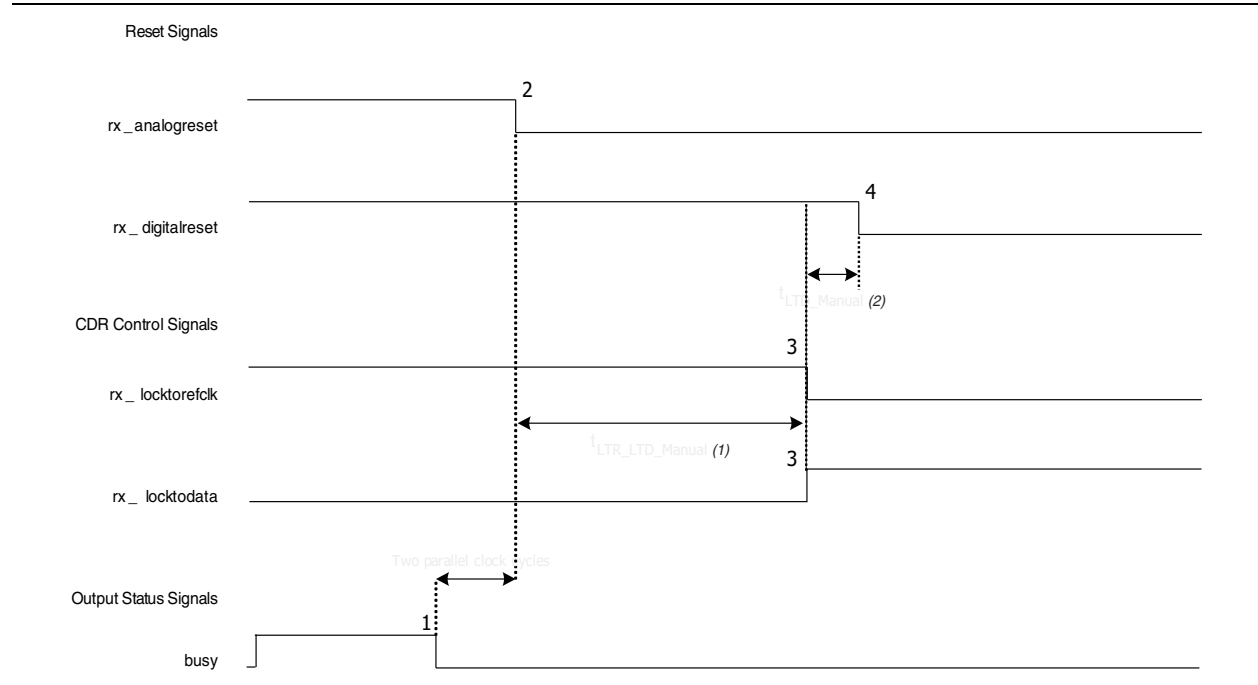


Figure 1-3 shows the lock time parameters in automatic mode.

Figure 1-3. Lock Time Parameters for Automatic Mode

