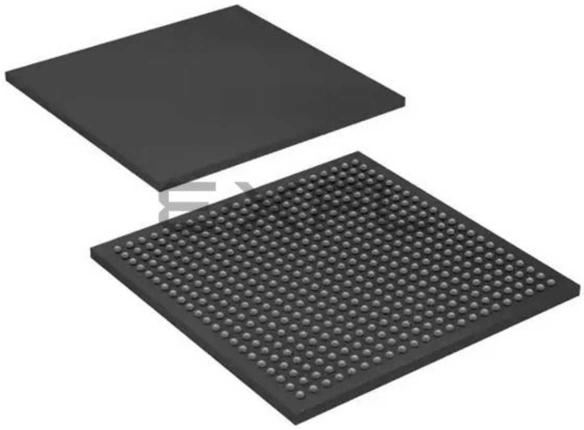

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	7155
Number of Logic Elements/Cells	114480
Total RAM Bits	3981312
Number of I/O	280
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce115f23c9l

Cyclone IV Device Family Architecture

This section describes Cyclone IV device architecture and contains the following topics:

- "FPGA Core Fabric"
- "I/O Features"
- "Clock Management"
- "External Memory Interfaces"
- "Configuration"
- "High-Speed Transceivers (Cyclone IV GX Devices Only)"
- "Hard IP for PCI Express (Cyclone IV GX Devices Only)"

FPGA Core Fabric

Cyclone IV devices leverage the same core fabric as the very successful Cyclone series devices. The fabric consists of LEs, made of 4-input look up tables (LUTs), memory blocks, and multipliers.

Each Cyclone IV device M9K memory block provides 9 Kbits of embedded SRAM memory. You can configure the M9K blocks as single port, simple dual port, or true dual port RAM, as well as FIFO buffers or ROM. They can also be configured to implement any of the data widths in Table 1–7.

Table 1–7. M9K Block Data Widths for Cyclone IV Device Family

Mode	Data Width Configurations
Single port or simple dual port	×1, ×2, ×4, ×8/9, ×16/18, and ×32/36
True dual port	×1, ×2, ×4, ×8/9, and ×16/18

The multiplier architecture in Cyclone IV devices is the same as in the existing Cyclone series devices. The embedded multiplier blocks can implement an 18 × 18 or two 9 × 9 multipliers in a single block. Altera offers a complete suite of DSP IP including finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions for use with the multiplier blocks. The Quartus® II design software's DSP Builder tool integrates MathWorks Simulink and MATLAB design environments for a streamlined DSP design flow.

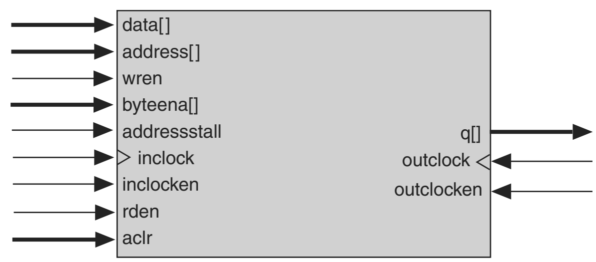
For more information, refer to the *Logic Elements and Logic Array Blocks in Cyclone IV Devices*, *Memory Blocks in Cyclone IV Devices*, and *Embedded Multipliers in Cyclone IV Devices* chapters.

☞ Violating the setup or hold time on the M9K memory block input registers may corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations from a single address. Figure 3–6 shows the single-port memory configuration for Cyclone IV devices M9K memory blocks.

Figure 3–6. Single-Port Memory *(1)*, *(2)*



Notes to Figure 3–6:

(1) You can implement two single-port memory blocks in a single M9K block.
(2) For more information, refer to "Packed Mode Support" on page 3–4.

During a write operation, the behavior of the RAM outputs is configurable. If you activate `rden` during a write operation, the RAM outputs show either the new data being written or the old data at that address. If you perform a write operation with `rden` deactivated, the RAM outputs retain the values they held during the most recent active `rden` signal.

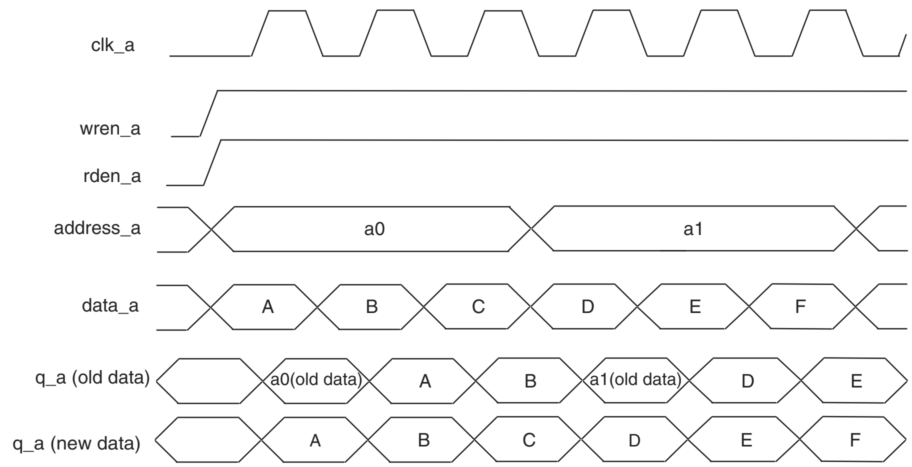
To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about read-during-write mode, refer to "Read-During-Write Operations" on page 3–15.

The port width configurations for M9K blocks in single-port mode are as follow:

- 8192 × 1
- 4096 × 2
- 2048 × 4
- 1024 × 8
- 1024 × 9
- 512 × 16
- 512 × 18
- 256 × 32
- 256 × 36

Figure 3–7 shows a timing waveform for read and write operations in single-port mode with unregistered outputs. Registering the outputs of the RAM simply delays the `q` output by one clock cycle.

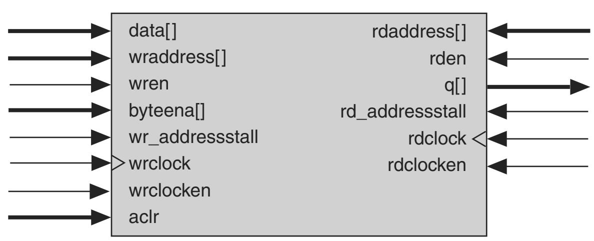
Figure 3–7. Cyclone IV Devices Single-Port Mode Timing Waveform



Simple Dual-Port Mode

Simple dual-port mode supports simultaneous read and write operations to different locations. Figure 3–8 shows the simple dual-port memory configuration.

Figure 3–8. Cyclone IV Devices Simple Dual-Port Memory *(1)*



Note to Figure 3–8:

(1) Simple dual-port RAM supports input or output clock mode in addition to the read or write clock mode shown.

Cyclone IV devices M9K memory blocks support mixed-width configurations, allowing different read and write port widths. Table 3–3 lists mixed-width configurations.

Table 3–3. Cyclone IV Devices M9K Block Mixed-Width Configurations (Simple Dual-Port Mode) ***(Part 1 of 2)***

Read Port	Write Port								
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36
8192 × 1	✓	✓	✓	✓	✓	✓	—	—	—
4096 × 2	✓	✓	✓	✓	✓	✓	—	—	—
2048 × 4	✓	✓	✓	✓	✓	✓	—	—	—
1024 × 8	✓	✓	✓	✓	✓	✓	—	—	—

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–5 and Figure 6–6.

Figure 6–5. Cyclone IV Devices HSTL I/O Standard Termination

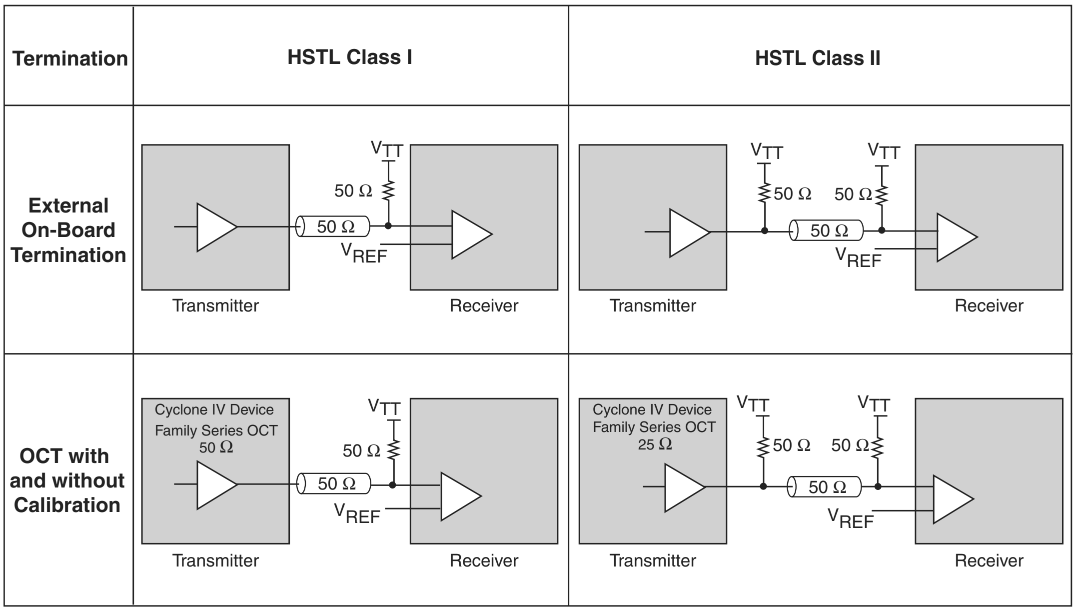


Figure 6–6. Cyclone IV Devices SSTL I/O Standard Termination

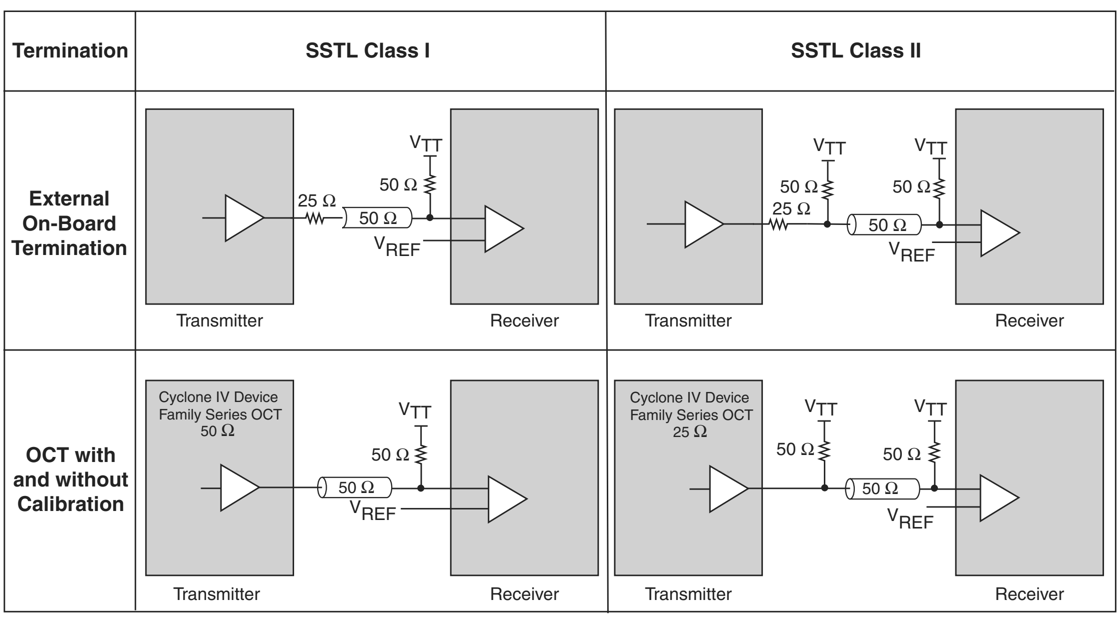


Figure 6–16. RSDS, Mini-LVDS, or PPDS Interface with External Resistor Network on the Top and Bottom I/O Banks *(1)*

Note to Figure 6–16:

(1) R_S and R_P values are pending characterization.

A resistor network is required to attenuate the output voltage swing to meet RSDS, mini-LVDS, and PPDS specifications when using emulated transmitters. You can modify the resistor network values to reduce power or improve the noise margin.

The resistor values chosen must satisfy Equation 6–1.

Equation 6–1. Resistor Network

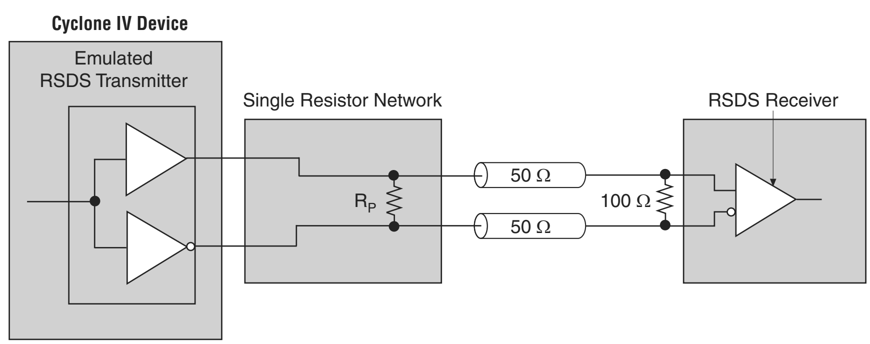
$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\ \Omega$$

Altera recommends that you perform simulations using Cyclone IV devices IBIS models to validate that custom resistor values meet the RSDS, mini-LVDS, or PPDS requirements.

It is possible to use a single external resistor instead of using three resistors in the resistor network for an RSDS interface, as shown in Figure 6–17. The external single-resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. However, the performance of the single-resistor solution is lower than the performance with the three-resistor network.

Figure 6–17 shows the RSDS interface with a single resistor network on the top and bottom I/O banks.

Figure 6–17. RSDS Interface with Single Resistor Network on the Top and Bottom I/O Banks *(1)*



Note to Figure 6–17:

(1) R_P value is pending characterization.

Differential SSTL I/O Standard Support in Cyclone IV Devices

The differential SSTL I/O standard is a memory-bus standard used for applications such as high-speed DDR SDRAM interfaces. Cyclone IV devices support differential SSTL-2 and SSTL-18 I/O standards. The differential SSTL output standard is only supported at `PLL#_CLKOUT` pins using two single-ended SSTL output buffers (`PLL#_CLKOUTp` and `PLL#_CLKOUTn`), with the second output programmed to have opposite polarity. The differential SSTL input standard is supported on the GCLK pins only, treating differential inputs as two single-ended SSTL and only decoding one of them.

The differential SSTL I/O standard requires two differential inputs with an external reference voltage (`VREF`) as well as an external termination voltage (`VTT`) of 0.5 × V_{CCIO} to which termination resistors are connected.

For differential SSTL electrical specifications, refer to "Differential I/O Standard Termination" on page 6–15 and the *Cyclone IV Device Datasheet* chapter.

Figure 6–8 on page 6–15 shows the differential SSTL Class I and Class II interface.

Differential HSTL I/O Standard Support in Cyclone IV Devices

The differential HSTL I/O standard is used for the applications designed to operate in 0 V to 1.2 V, 0 V to 1.5 V, or 0 V to 1.8 V HSTL logic switching range. Cyclone IV devices support differential HSTL-18, HSTL-15, and HSTL-12 I/O standards. The differential HSTL input standard is available on GCLK pins only, treating the differential inputs as two single-ended HSTL and only decoding one of them. The differential HSTL output standard is only supported at the `PLL#_CLKOUT` pins using two single-ended HSTL output buffers (`PLL#_CLKOUT`*p* and `PLL#_CLKOUT`*n*), with the second output programmed to have opposite polarity.

The differential HSTL I/O standard requires two differential inputs with an external reference voltage (`VREF`), as well as an external termination voltage (`VTT`) of 0.5 × V_{CCIO} to which termination resistors are connected.

For differential HSTL signaling characteristics, refer to "Differential I/O Standard Termination" on page 6–15 and the *Cyclone IV Device Datasheet* chapter.

Figure 6–7 on page 6–15 shows the differential HSTL Class I and Class II interface.

True Differential Output Buffer Feature

Cyclone IV devices true differential transmitters offer programmable pre-emphasis—you can turn it on or off. The default setting is on.

Programmable Pre-Emphasis

The programmable pre-emphasis boosts the high frequencies of the output signal to compensate the frequency-dependant attenuation of the transmission line to maximize the data eye opening at the far-end receiver. Without pre-emphasis, the output current is limited by the V_{OD} specification and the output impedance of the transmitter. At high frequency, the slew rate may not be fast enough to reach full V_{OD}

Board Design Considerations

This section explains how to achieve the optimal performance from a Cyclone IV I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. You must consider the critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques to get the best performance from Cyclone IV devices.

Use the following general guidelines to improve signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters, such as trace width, trace thickness, and the distance between two differential traces.
- Maintain equal distance between traces in differential I/O standard pairs as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).
- Longer traces have more inductance and capacitance. These traces must be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° corners on board traces.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the impedance of the connector and termination.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the TCCS value increases.
- Limit vias because they cause discontinuities.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines* and *AN 315: Guidelines for Designing High-Speed FPGA PCBs.*

Software Overview

Cyclone IV devices high-speed I/O system interfaces are created in core logic by a Quartus II software megafunction because they do not have a dedicated circuit for the SERDES. Cyclone IV devices use the I/O registers and LE registers to improve the timing performance and support the SERDES. The Quartus II software allows you to design your high-speed interfaces using ALTLVDS megafunction. This megafunction

Figure 7–3 shows the location and numbering of the `DQS`, `DQ`, or CQ# pins in I/O banks of the Cyclone IV GX device in the 324-pin FBGA package only.

Figure 7–3. DQS, CQ, or CQ# Pins for Cyclone IV GX Devices in the 324-Pin FBGA Package

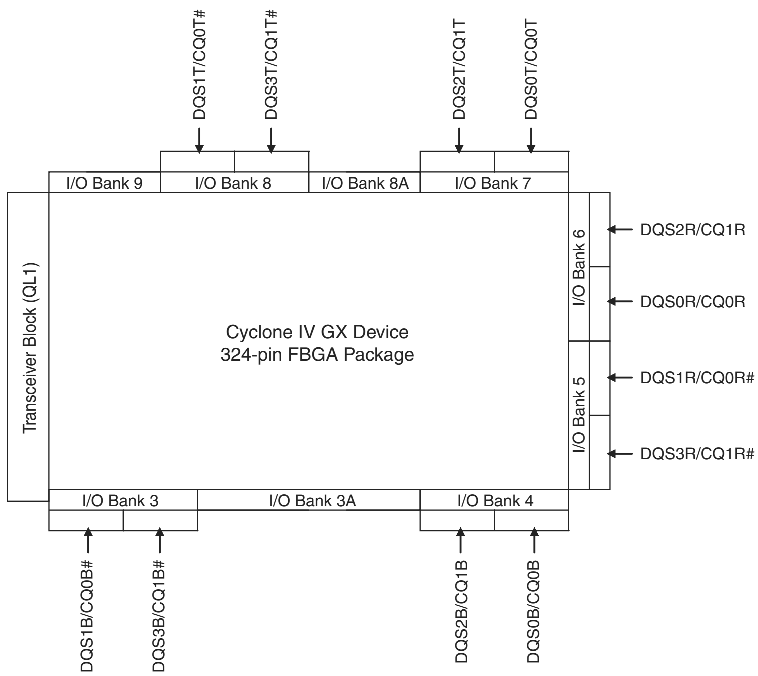


Figure 7–4 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV GX device in the 169-pin FBGA package.

Figure 7–4. DQS, CQ, or CQ# Pins for Cyclone IV GX Devices in the 169-Pin FBGA Package

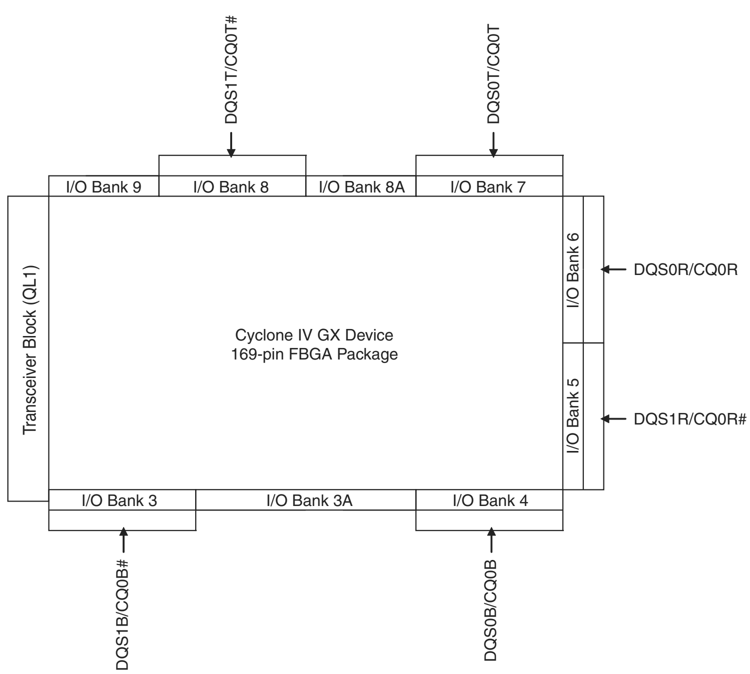
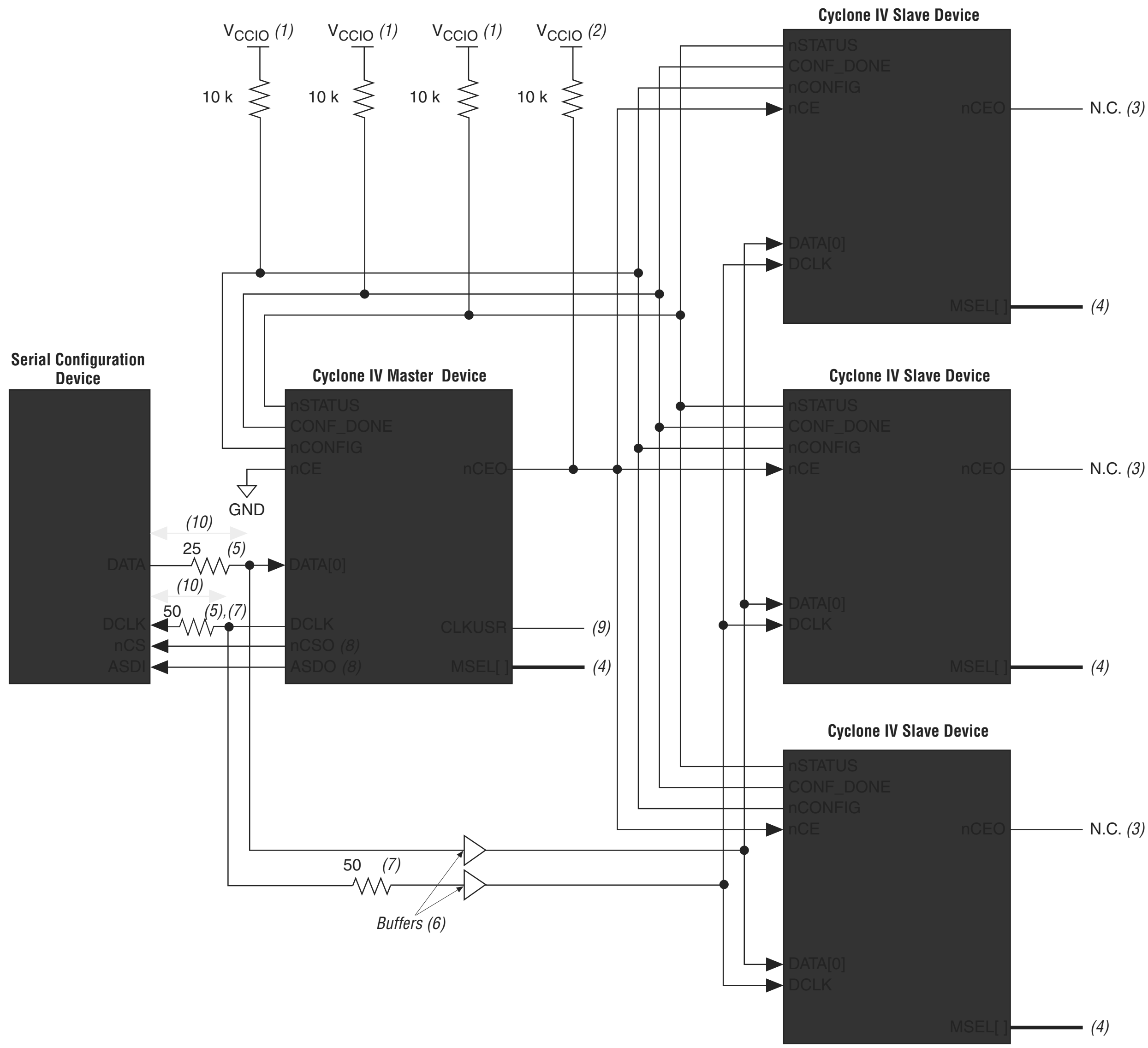


Figure 8–4. Multi-Device AS Configuration in Which Devices Receive the Same Data with Multiple .sof



Notes to Figure 8–4:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the `nCE` pin resides.

(3) The `nCEO` pin is left unconnected or used as a user I/O pin when it does not feed the `nCE` pin of another device.

(4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the master device in AS mode and the slave devices in PS mode. To connect the `MSEL` pins for the master device in AS mode and the slave devices in PS mode, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the `MSEL` pins directly to V_{CCA} or GND.

(5) Connect the series resistor at the near end of the serial configuration device.

(6) Connect the repeater buffers between the master and slave devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.

(7) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

(8) These pins are dual-purpose I/O pins. The `nCSO` pin functions as `FLASH_nCE` pin in AP mode. The `ASDO` pin functions as `DATA[1]` pin in AP and FPP modes.

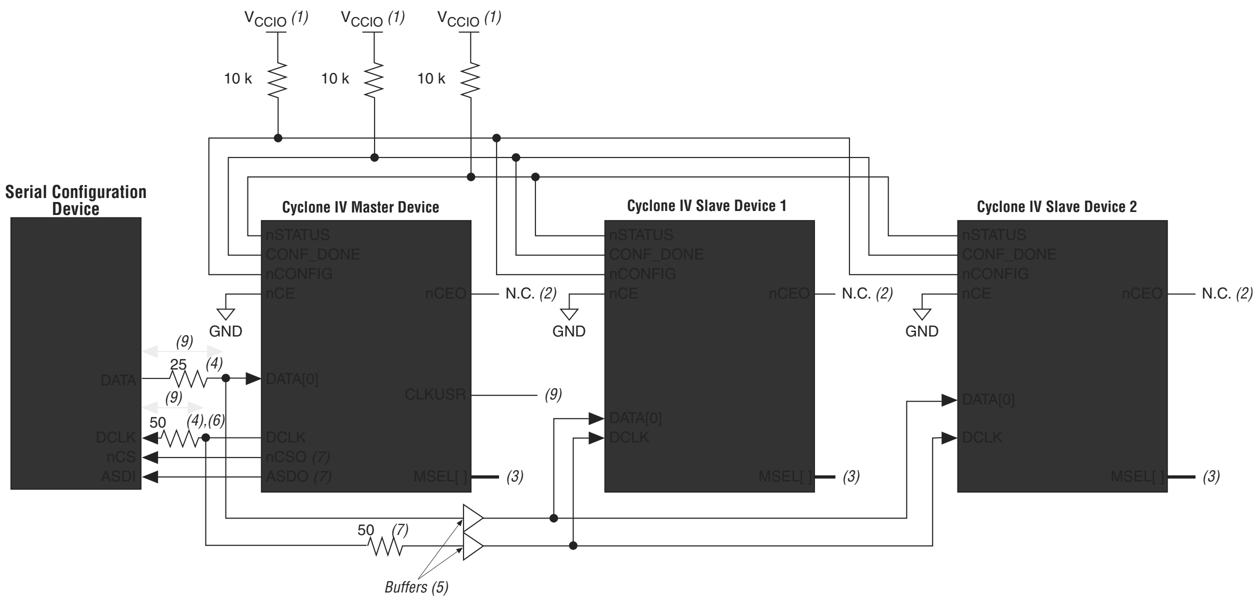
(9) Only Cyclone IV GX devices have an option to select `CLKUSR` (40 MHz maximum) as the external clock source for `DCLK`.

(10) For multi-devices AS configuration using Cyclone IV E with 1,0 V core voltage, the maximum board trace-length from the serial configuration device to the junction-split on both `DCLK` and `Data0` line is 3.5 inches.

Single SRAM Object File

The second method configures both the master device and slave devices with the same **.sof**. The serial configuration device stores one copy of the **.sof**. You must set up one or more slave devices in the chain. All the slave devices must be set up in the same way (Figure 8–5).

Figure 8–5. Multi-Device AS Configuration in Which Devices Receive the Same Data with a Single .sof



Notes to Figure 8–5:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin is left unconnected or used as a user I/O pin when it does not feed the `nCE` pin of another device.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the master device of the Cyclone IV device in AS mode and the slave devices in PS mode. To connect the `MSEL` pins for the master device in AS mode and slave devices in PS mode, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the `MSEL` pins directly to V_{CCA} or GND.

(4) Connect the series resistor at the near end of the serial configuration device.

(5) Connect the repeater buffers between the master and slave devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in “Configuration and JTAG Pin I/O Requirements” on page 8–5.

(6) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

(7) These pins are dual-purpose I/O pins. The `nCSO` pin functions as `FLASH_nCE` pin in AP mode. The `ASDO` pin functions as `DATA[1]` pin in AP and FPP modes.

(8) Only Cyclone IV GX devices have an option to select `CLKUSR` (40 MHz maximum) as the external clock source for `DCLK`.

(9) For multi-devices AS configuration using Cyclone IV E with 1,0 V core voltage, the maximum board trace-length from the serial configuration device to the junction-split on both `DCLK` and `Data0` line is 3.5 inches.

In this setup, all the Cyclone IV devices in the chain are connected for concurrent configuration. This reduces the AS configuration time because all the Cyclone IV devices are configured in one configuration cycle. Connect the `nCE` input pins of all the Cyclone IV devices to GND. You can either leave the `nCEO` output pins on all the Cyclone IV devices unconnected or use the `nCEO` output pins as normal user I/O pins. The `DATA` and `DCLK` pins are connected in parallel to all the Cyclone IV devices.

During device configuration, Cyclone IV E devices read configuration data using the parallel interface and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where an external host controls the interface.

AP Configuration Supported Flash Memories

The AP configuration controller in Cyclone IV E devices is designed to interface with two industry-standard flash families—the Micron P30 Parallel NOR flash family and the Micron P33 Parallel NOR flash family. Unlike serial configuration devices, both of the flash families supported in AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash after entering user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Micron P30 flash family and the P33 flash family support a continuous synchronous burst read mode at 40 MHz `DCLK` frequency for reading data from the flash. Additionally, the Micron P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.

☞ Cyclone IV E devices use a 40-MHz oscillator for the AP configuration scheme. The oscillator is the same oscillator used in the Cyclone IV E AS configuration scheme.

Table 8–10 lists the supported families of the commodity parallel flash for the AP configuration scheme.

Table 8–10. Supported Commodity Flash for AP Configuration Scheme for Cyclone IV E Devices (1)

Flash Memory Density	Micron P30 Flash Family (2)	Micron P33 Flash Family (3)
64 Mbit	✓	✓
128 Mbit	✓	✓
256 Mbit	✓	✓

Notes to Table 8–10:

(1) The AP configuration scheme only supports flash memory speed grades of 40 MHz and above.

(2) 3.3- , 3.0-, 2.5-, and 1.8-V I/O options are supported for the Micron P30 flash family.

(3) 3.3-, 3.0- and 2.5-V I/O options are supported for the Micron P33 flash family.

Configuring Cyclone IV E devices from the Micron P30 and P33 family 512-Mbit flash memory is possible, but you must properly drive the extra address and `FLASH_nCE` pins as required by these flash memories.

To check for supported speed grades and package options, refer to the respective flash datasheets.

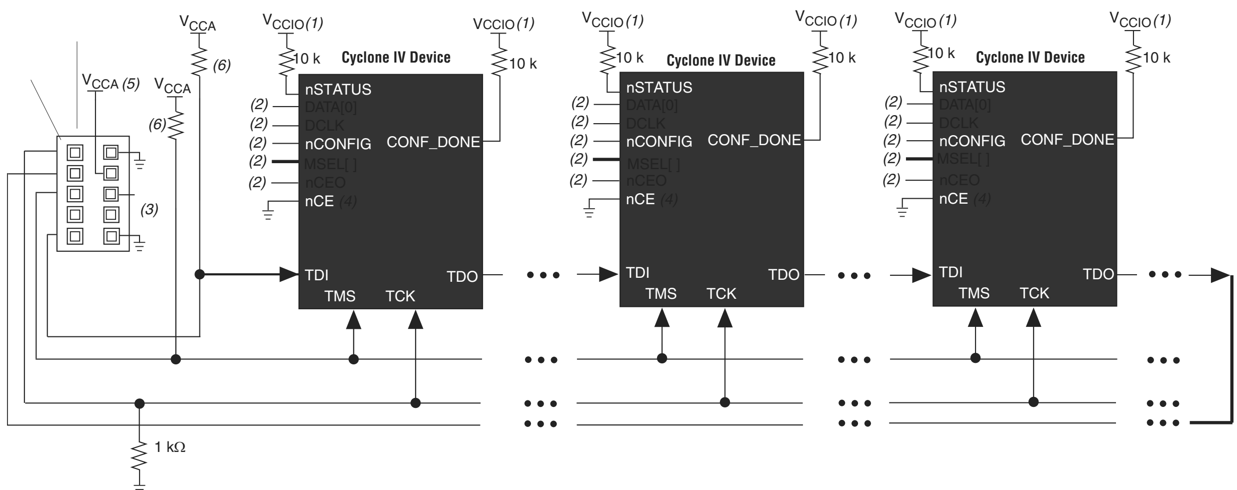
The AP configuration scheme in Cyclone IV E devices supports flash speed grades of 40 MHz and above. However, AP configuration for all these speed grades must be capped at 40 MHz. The advantage of faster speed grades is realized when your design in the Cyclone IV E devices accesses flash memory in user mode.

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system with JTAG BST circuitry. Figure 8–25 and Figure 8–26 show multi-device JTAG configuration.

For devices using 2.5-, 3.0-, and 3.3-V V_{CCIO} supply, you must refer to Figure 8–25. All I/O inputs must maintain a maximum AC voltage of 4.1 V because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using 2.5-, 3.0-, and 3.3- V V_{CCIO} supply. You must power up the V_{CC} of the download cable with a 2.5-V V_{CCA} supply. For device using V_{CCIO} of 1.2, 1.5 V, and 1.8 V, refer to Figure 8–26. You can power up the V_{CC} of the download cable with the supply from V_{CCIO}.

Figure 8–25. JTAG Configuration of Multiple Devices Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 8–25:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

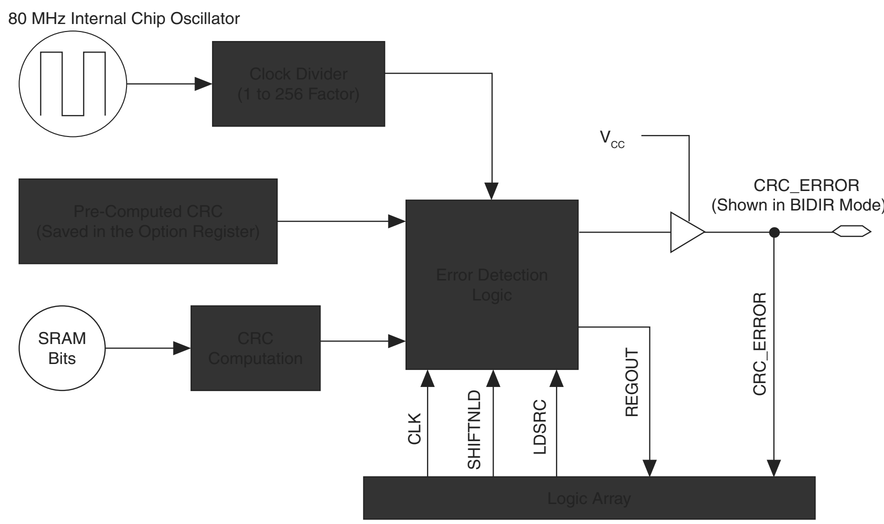
(4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.

(5) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

(6) Resistor value can vary from 1 kΩ to 10 kΩ.

Figure 9–3 shows the error detection block diagram in FPGA devices and shows the interface that the WYSIWYG atom enables in your design.

Figure 9–3. Error Detection Block Diagram



☞ The user logic is affected by the soft error failure, so reading out the 32-bit CRC signature through the `regout` should not be relied upon to detect a soft error. You should rely on the `CRC_ERROR` output signal itself, because this `CRC_ERROR` output signal cannot be affected by a soft error.

To enable the `cycloneiv_crcblock` WYSIWYG atom, you must name the atom for each Cyclone IV device accordingly.

Example 9–1 shows an example of how to define the input and output ports of a WYSIWYG atom in a Cyclone IV device.

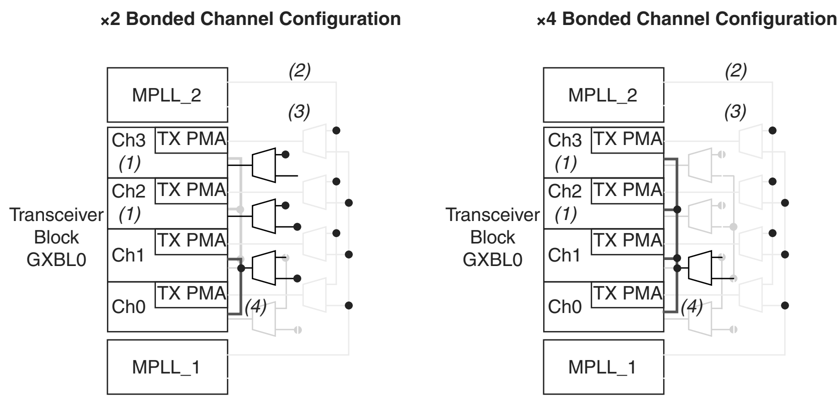
Example 9–1. Error Detection Block Diagram

```
cycloneiv_crcblock<crcblock_name>

(

.clk(<clock source>),

.shiftnld(<shiftnld source>),

.ldsrc(<ldsrc source>),

.crcerror(<crcerror out destination>),

.regout(<output destination>),

);
```

Chapter 2. Cyclone IV Reset Control and Power Down

Figure 1–36 and Figure 1–37 show the independent high-speed clock and bonded low-speed clock distributions for transceivers in F324 and smaller packages, and in F484 and larger packages in bonded (×2 and ×4) channel configuration.

Figure 1–36. Clock Distribution in Bonded (×2 and ×4) Channel Configuration for Transceivers in F324 and Smaller Packages.



Notes to Figure 1–36:

1. Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
2. High-speed clock.
3. Low-speed clock.
4. Bonded common low-speed clock path.

PCIe Initialization/Compliance Phase

After the device is powered up, a PCIe-compliant device goes through the compliance phase during initialization. The rx_digitalreset signal must be deasserted during this compliance phase to achieve transitions on the pipephydonestatus signal, as expected by the link layer. The rx_digitalreset signal is deasserted based on the assertion of the rx_freqlocked signal.

During the initialization/compliance phase, do not use the rx_freqlocked signal to trigger a deassertion of the rx_digitalreset signal. Instead, perform the following reset sequence:

1. After power up, assert pll_areset for a minimum period of 1 μs (the time between markers 1 and 2). Keep the tx_digitalreset, rx_analogreset, and rx_digitalreset signals asserted during this time period. After you deassert the pll_areset signal, the multipurpose PLL starts locking to the input reference clock.
2. After the multipurpose PLL locks, as indicated by the pll_locked signal going high (marker 3), deassert tx_digitalreset. For a receiver operation, after deassertion of busy signal, wait for two parallel clock cycles to deassert the rx_analogreset signal. After rx_analogreset is deasserted, the receiver CDR starts locking to the receiver input reference clock.
3. Deassert both the rx_analogreset signal (marker 6) and rx_digitalreset signal (marker 7) together, as indicated in Figure 2–10. After deasserting rx_digitalreset, the pipephydonestatus signal transitions from the transceiver channel to indicate the status to the link layer. Depending on its status, pipephydonestatus helps with the continuation of the compliance phase. After successful completion of this phase, the device enters into the normal operation phase.

PCIe Normal Phase

For the normal PCIe phase:

1. After completion of the Initialization/Compliance phase, during the normal operation phase at the Gen1 data rate, when the rx_freqlocked signal is deasserted (marker 9 in Figure 2–10).
2. Wait for the rx_freqlocked signal to go high again. In this phase, the received data is valid (not electrical idle) and the receiver CDR locks to the incoming data. Proceed with the reset sequence after assertion of the rx_freqlocked signal.
3. After the rx_freqlocked signal goes high, wait for at least t_{LTD_Manual} before asserting rx_digitalreset (marker 12 in Figure 2–10) for two parallel receive clock cycles so that the receiver phase compensation FIFO is initialized. For bonded PCIe Gen 1 mode (×2 and ×4), wait for all the rx_freqlocked signals to go high, then wait for t_{LTD_Manual} before asserting rx_digitalreset for 2 parallel clock cycles.

Table 3–4 describes the `tx_datainfull[21..0]` FPGA fabric-transceiver channel interface signals.

Table 3–4. tx_datainfull[21..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions (1)

FPGA Fabric-Transceiver Channel Interface Description	Transmit Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)
8-bit FPGA fabric-Transceiver Channel Interface	`tx_datainfull[7:0]`: 8-bit data (`tx_datain`)
	The following signals are used only in 8B/10B modes:
	`tx_datainfull[8]`: Control bit (`tx_ctrlenable`)
	`tx_datainfull[9]` Transmitter force disparity Compliance (PCI Express [PIPE]) (`tx_forcedisp`) in all modes except PCI Express (PIPE) functional mode. For PCI Express (PIPE) functional mode, (`tx_forcedispcompliance`) is used.
	■ For non-PIPE: `tx_datainfull[10]`: Forced disparity value (`tx_dispval`) ■ For PCIe: `tx_datainfull[10]`: Forced electrical idle (`tx_forceelecidle`)
10-bit FPGA fabric-Transceiver Channel Interface	`tx_datainfull[9:0]`: 10-bit data (`tx_datain`)
16-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 8/10 bits	Two 8-bit Data (`tx_datain`) `tx_datainfull[7:0]` - `tx_datain` (LSByte) and `tx_datainfull[18:11]` - `tx_datain` (MSByte)
	The following signals are used only in 8B/10B modes:
	`tx_datainfull[8]` - `tx_ctrlenable` (LSB) and `tx_datainfull[19]` - `tx_ctrlenable` (MSB)
	Force Disparity Enable ■ For non-PIPE: `tx_datainfull[9]` - `tx_forcedisp` (LSB) and `tx_datainfull[20]` - `tx_forcedisp` (MSB) ■ For PCIe: `tx_datainfull[9]` - `tx_forcedispcompliance` and `tx_datainfull[20]` - 0
	Force Disparity Value ■ For non-PIPE: `tx_datainfull[10]` - `tx_dispval` (LSB) and `tx_datainfull[21]` - `tx_dispval` (MSB) ■ For PCIe: `tx_datainfull[10]` - `tx_forceelecidle` and `tx_datainfull[21]` - `tx_forceelecidle`
20-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 10 bits	Two 10-bit Data (`tx_datain`) `tx_datainfull[9:0]` - `tx_datain` (LSByte) and `tx_datainfull[20:11]` - `tx_datain` (MSByte)

Note to Table 3–4:

(1) For all transceiver-related ports, refer to the “Transceiver Port Lists” section in the *Cyclone IV GX Transceiver Architecture* chapter.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) *(15)*	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) *(15)*	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V_{ICM}	V_{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector *(4)*	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) *(8)*	—	—	—	350 to –5350 *(7)*, *(9)*	—	—	350 to –5350 *(7)*, *(9)*	—	—	350 to –5350 *(7)*, *(9)*	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2)

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1–42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2)

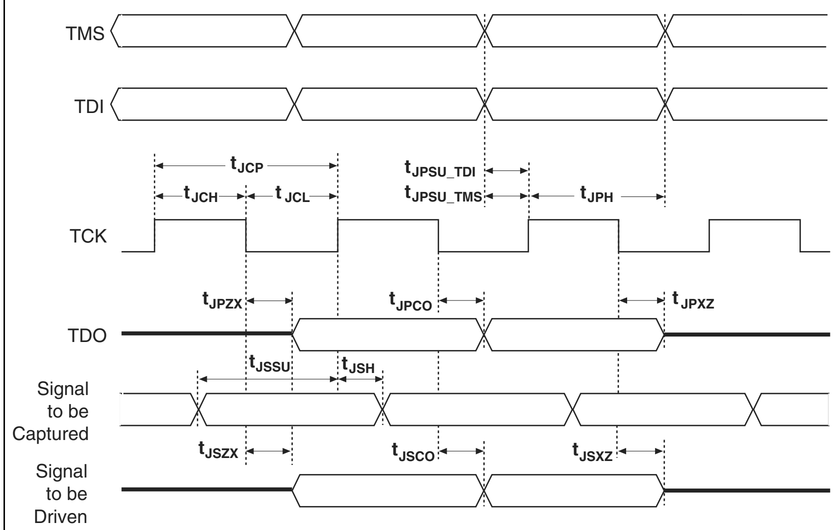
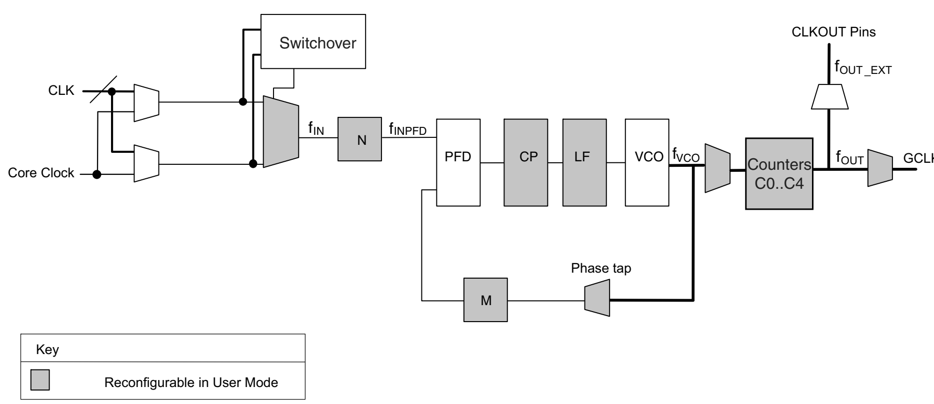
Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Notes to Table 1–43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–46. Glossary (Part 2 of 5)

Letter	Term	Definitions
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following highlights the PLL specification parameters: 
Q	—	—