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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	7155
Number of Logic Elements/Cells	114480
Total RAM Bits	3981312
Number of I/O	528
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce115f29c8

Asynchronous Clear

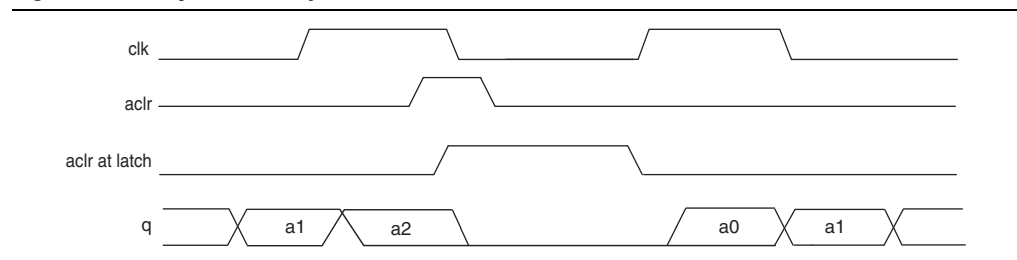
Cyclone IV devices support asynchronous clears for read address registers, output registers, and output latches only. Input registers other than read address registers are not supported. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are immediately seen. If your RAM does not use output registers, you can still clear the RAM outputs using the output latch asynchronous clear feature.



Asserting asynchronous clear to the read address register during a read operation may corrupt the memory content.

Figure 3–5 shows the functional waveform for the asynchronous clear feature.

Figure 3–5. Output Latch Asynchronous Clear Waveform



You can selectively enable asynchronous clears per logical memory using the Quartus II RAM MegaWizard™ Plug-In Manager.



For more information, refer to the *RAM Megafunction User Guide*.

There are three ways to reset registers in the M9K blocks:


- Power up the device
- Use the `aclr` signal for output register only
- Assert the device-wide reset signal using the `DEV_CLRn` option

Memory Modes

Cyclone IV devices M9K memory blocks allow you to implement fully-synchronous SRAM memory in multiple modes of operation. Cyclone IV devices M9K memory blocks do not support asynchronous (unregistered) memory inputs.

M9K memory blocks support the following modes:

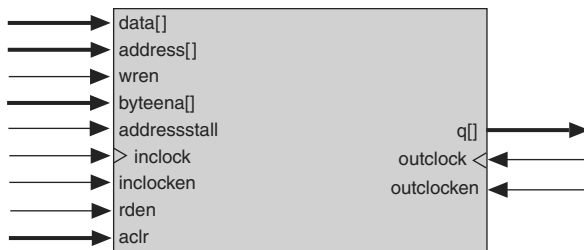
- Single-port
- Simple dual-port
- True dual-port
- Shift-register
- ROM
- FIFO

 Violating the setup or hold time on the M9K memory block input registers may corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations from a single address. Figure 3-6 shows the single-port memory configuration for Cyclone IV devices M9K memory blocks.

Figure 3-6. Single-Port Memory ⁽¹⁾, ⁽²⁾



Notes to Figure 3-6:

- (1) You can implement two single-port memory blocks in a single M9K block.
- (2) For more information, refer to “Packed Mode Support” on page 3-4.

During a write operation, the behavior of the RAM outputs is configurable. If you activate `rden` during a write operation, the RAM outputs show either the new data being written or the old data at that address. If you perform a write operation with `rden` deactivated, the RAM outputs retain the values they held during the most recent active `rden` signal.

To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about read-during-write mode, refer to “Read-During-Write Operations” on page 3-15.

The port width configurations for M9K blocks in single-port mode are as follow:

- 8192×1
- 4096×2
- 2048×4
- 1024×8
- 1024×9
- 512×16
- 512×18
- 256×32
- 256×36

4. Embedded Multipliers in Cyclone IV Devices

CYIV-51004-1.1

Cyclone® IV devices include a combination of on-chip resources and external interfaces that help increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. Cyclone IV devices, either alone or as DSP device co-processors, are used to improve price-to-performance ratios of DSP systems. Particular focus is placed on optimizing Cyclone IV devices for applications that benefit from an abundance of parallel processing resources, which include video and image processing, intermediate frequency (IF) modems used in wireless communications systems, and multi-channel communications and video systems.

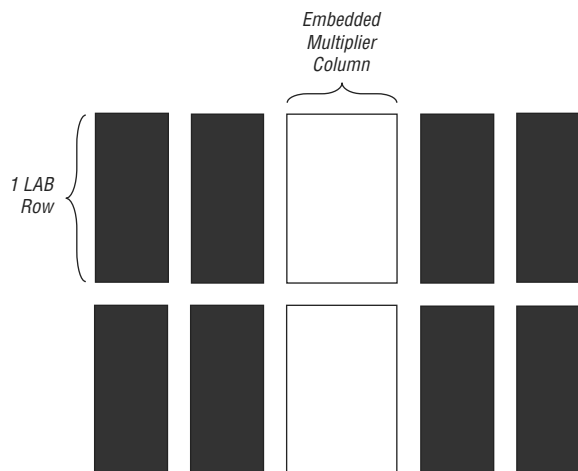
This chapter contains the following sections:

- “Embedded Multiplier Block Overview” on page 4–1
- “Architecture” on page 4–2
- “Operational Modes” on page 4–4

Embedded Multiplier Block Overview

Figure 4–1 shows one of the embedded multiplier columns with the surrounding logic array blocks (LABs). The embedded multiplier is configured as either one 18×18 multiplier or two 9×9 multipliers. For multiplications greater than 18×18 , the Quartus® II software cascades multiple embedded multiplier blocks together. There are no restrictions on the data width of the multiplier, but the greater the data width, the slower the multiplication process.

Figure 4–1. Embedded Multipliers Arranged in Columns with Adjacent LABs



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Figure 6-16. RSDS, Mini-LVDS, or PPDS Interface with External Resistor Network on the Top and Bottom I/O Banks ⁽¹⁾

Note to Figure 6-16:

(1) R_S and R_P values are pending characterization.

A resistor network is required to attenuate the output voltage swing to meet RSDS, mini-LVDS, and PPDS specifications when using emulated transmitters. You can modify the resistor network values to reduce power or improve the noise margin.

The resistor values chosen must satisfy Equation 6-1.

Equation 6-1. Resistor Network

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50 \, \Omega$$

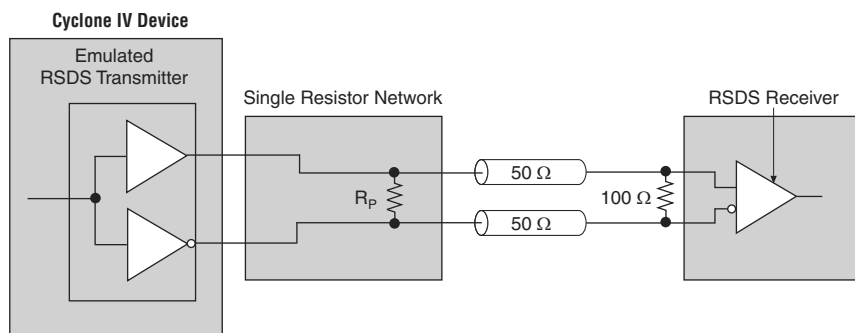


Altera recommends that you perform simulations using Cyclone IV devices IBIS models to validate that custom resistor values meet the RSDS, mini-LVDS, or PPDS requirements.

It is possible to use a single external resistor instead of using three resistors in the resistor network for an RSDS interface, as shown in Figure 6-17. The external single-resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. However, the performance of the single-resistor solution is lower than the performance with the three-resistor network.

Figure 6-17 shows the RSDS interface with a single resistor network on the top and bottom I/O banks.

Figure 6-17. RSDS Interface with Single Resistor Network on the Top and Bottom I/O Banks ⁽¹⁾



Note to Figure 6-17:

(1) R_P value is pending characterization.

The first Cyclone IV device in the chain is the configuration master and it controls the configuration of the entire chain. Other Altera devices that support PS configuration can also be part of the chain as configuration slaves.



In the multi-device AS configuration, the board trace length between the serial configuration device and the master device of the Cyclone IV device must follow the recommendations in Table 8-7 on page 8-18.

The `nSTATUS` and `CONF_DONE` pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8-3 on page 8-13. These pins are open-drain bidirectional pins on the devices. When the first device asserts `nCEO` (after receiving all its configuration data), it releases its `CONF_DONE` pin. However, the subsequent devices in the chain keep this shared `CONF_DONE` line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release `CONF_DONE`, the pull-up resistor drives a high level on `CONF_DONE` line and all devices simultaneously enter initialization mode.



Although you can cascade Cyclone IV devices, serial configuration devices cannot be cascaded or chained together.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device, enable the compression feature, or both. When configuring multiple devices, the size of the bitstream is the sum of the individual device's configuration bitstream.

Configuring Multiple Cyclone IV Devices with the Same Design

Certain designs require that you configure multiple Cyclone IV devices with the same design through a configuration bitstream, or a `.sof`. You can do this through the following methods:

- Multiple `.sof`
- Single `.sof`



For both methods, the serial configuration devices cannot be cascaded or chained together.

Multiple SRAM Object Files

Two copies of the `.sof` are stored in the serial configuration device. Use the first copy to configure the master device of the Cyclone IV device and the second copy to configure all remaining slave devices concurrently. All slave devices must have the same density and package. The setup is similar to Figure 8-3 on page 8-13.

To configure four identical Cyclone IV devices with the same `.sof`, you must set up the chain similar to the example shown in Figure 8-4. The first device is the master device and its `MSEL` pins must be set to select AS configuration. The other three slave devices are set up for concurrent configuration and their `MSEL` pins must be set to select PS configuration. The `nCEO` pin from the master device drives the `nCE` input pins on all three slave devices, as well as the `DATA` and `DCLK` pins that connect in parallel to all

- For more information about the operation of the Micron P30 Parallel NOR and P33 Parallel NOR flash memories, search for the keyword “P30” or “P33” on the Micron website (www.micron.com) to obtain the P30 or P33 family datasheet.

Single-Device AP Configuration

The following groups of interface pins are supported in Micron P30 and P33 flash memories:

- Control pins
- Address pins
- Data pins

The following control signals are from the supported parallel flash memories:

- CLK
- active-low reset (RST#)
- active-low chip enable (CE#)
- active-low output enable (OE#)
- active-low address valid (ADV#)
- active-low write enable (WE#)

The supported parallel flash memories output a control signal (WAIT) to Cyclone IV E devices to indicate when synchronous data is ready on the data bus. Cyclone IV E devices have a 24-bit address bus connecting to the address bus (A[24:1]) of the flash memory. A 16-bit bidirectional data bus (DATA[15:0]) provides data transfer between the Cyclone IV E device and the flash memory.

The following control signals are from the Cyclone IV E device to flash memory:

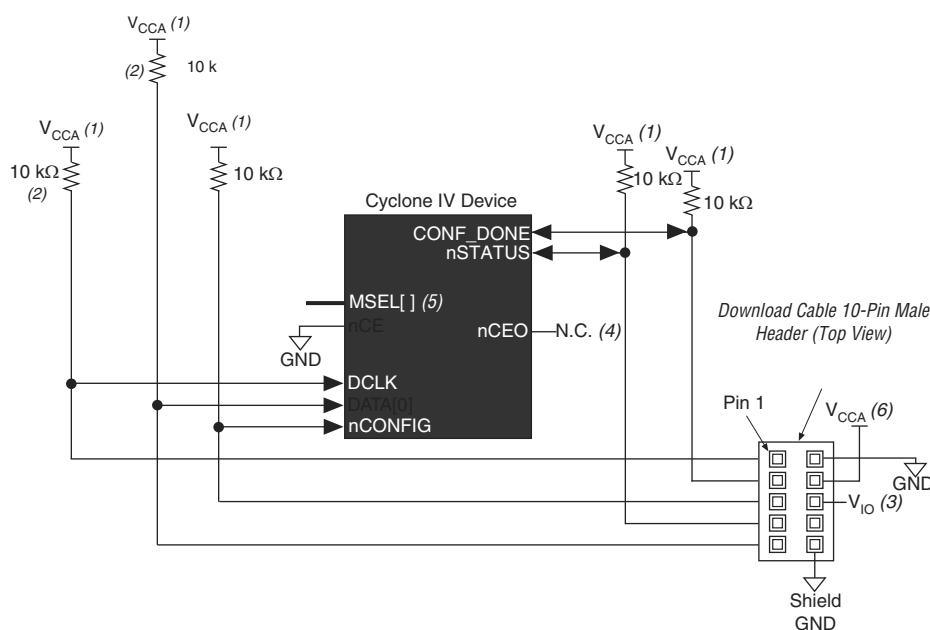
- DCLK
- active-low hard reset (nRESET)
- active-low chip enable (FLASH_nCE)
- active-low output enable for the DATA[15:0] bus and WAIT pin (nOE)
- active-low address valid signal and is used to write data into the flash (nAVD)
- active-low write enable and is used to write data into the flash (nWE)

The programming hardware or download cable then places the configuration data one bit at a time on the DATA[0] pin of the device. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-k Ω pull-up resistor for the device to initialize.

When you use a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software if an error occurs. Additionally, the **Enable user-supplied start-up clock (CLKUSR)** option has no effect on device initialization, because this option is disabled in the .sof when programming the device with the Quartus II Programmer and download cable. Therefore, if you turn on the CLKUSR option, you do not have to provide a clock on CLKUSR when you configure the device with the Quartus II Programmer and a download cable.

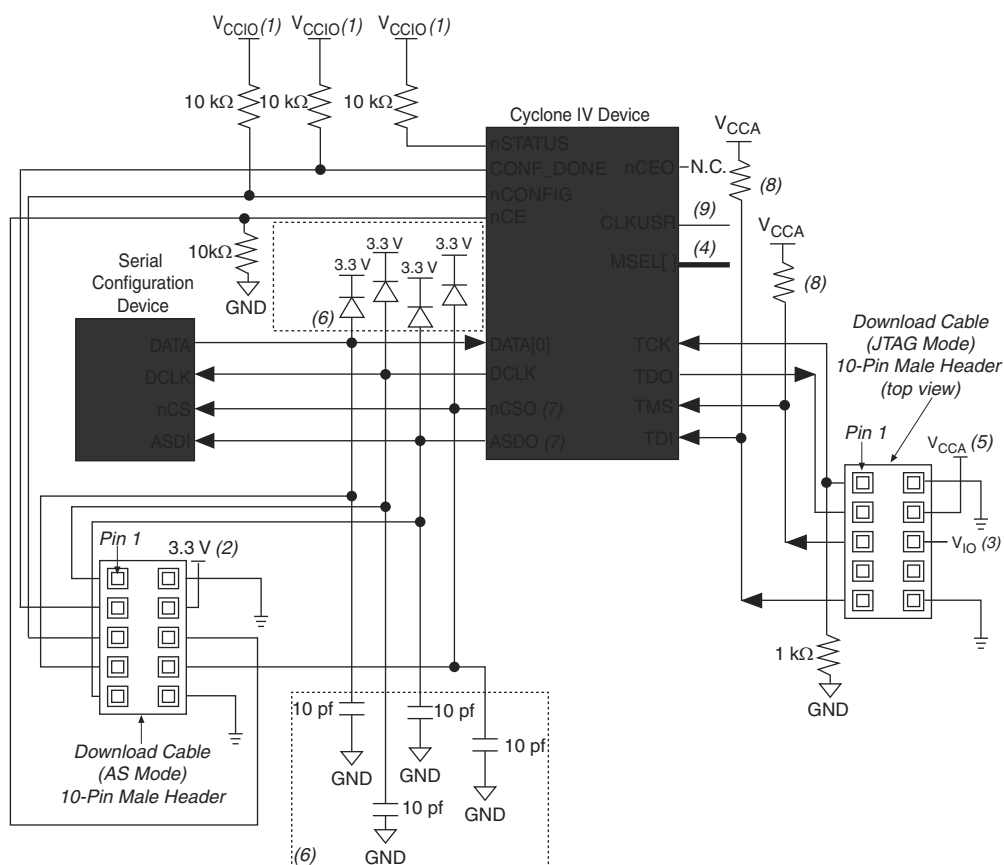
Figure 8-17 shows PS configuration for Cyclone IV devices with a download cable.

Figure 8-17. PS Configuration Using a Download Cable



Notes to Figure 8-17:

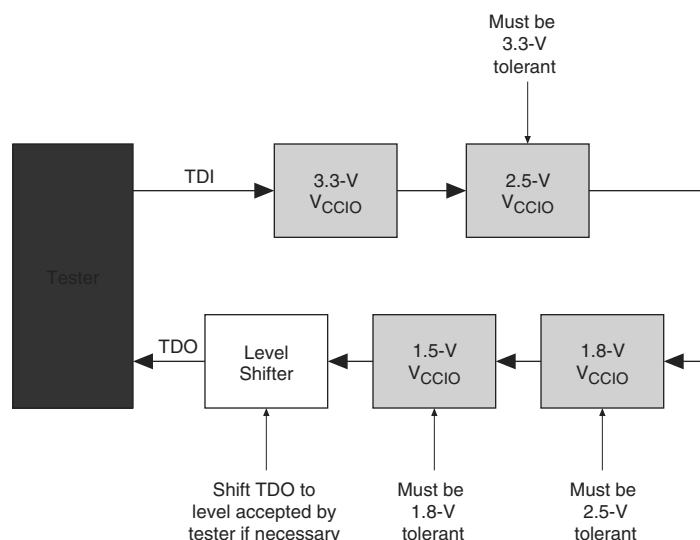
- (1) You must connect the pull-up resistor to the same supply voltage as the V_{CCA} supply.
- (2) The pull-up resistors on DATA[0] and DCLK are only required if the download cable is the only configuration scheme used on your board. This is to ensure that DATA[0] and DCLK are not left floating after configuration. For example, if you also use a configuration device, the pull-up resistors on DATA[0] and DCLK are not required.
- (3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. With the USB-Blaster, ByteBlaster II, ByteBlaster MV, and EthernetBlaster, this pin is a no connect.
- (4) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (5) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8-3 on page 8-8, Table 8-4 on page 8-8, and Table 8-5 on page 8-9 for PS configuration schemes. Connect the MSEL pins directly to V_{CCA} or GND.
- (6) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA} . Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

Figure 8–28. Combining JTAG and AS Configuration Schemes**Notes to Figure 8–28:**

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, or USB-Blaster cable with the 3.3-V supply.
- (3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. The V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the ByteBlasterMV download cable, this pin is a no connect. When using the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for AS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND .
- (5) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V V_{CCA} supply. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) You must place the diodes and capacitors as close as possible to the Cyclone IV device. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.
- (7) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as $\text{DATA}[1]$ pin in AP and FPP modes.
- (8) Resistor value can vary from 1 k Ω to 10 k Ω .
- (9) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK .

Figure 10-3 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 10-3. JTAG Chain of Mixed Voltages



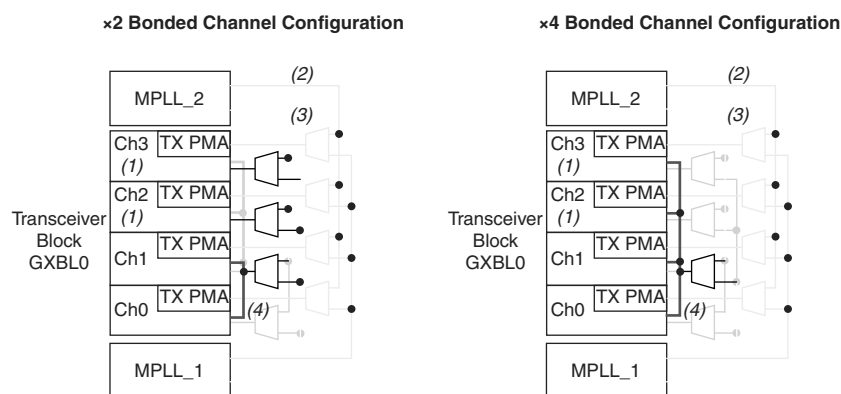
Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1/IEEE Std. 1149.6 BST-capable device that can be tested.

- For more information about how to download BSDL files for IEEE Std. 1149.1-compliant Cyclone IV E devices, refer to *IEEE Std. 1149.1 BSDL Files*.
- For more information about how to download BSDL files for IEEE Std. 1149.6-compliant Cyclone IV GX devices, refer to *IEEE Std. 1149.6 BSDL Files*.
- You can also generate BSDL files (pre-configuration and post-configuration) for IEEE Std. 1149.1/IEEE Std. 1149.6-compliant Cyclone IV devices with the Quartus® II software version 9.1 SP1 and later. For more information about the procedure to generate BSDL files using the Quartus II software, refer to *BSDL Files Generation in Quartus II*.

Figure 1-36 and Figure 1-37 show the independent high-speed clock and bonded low-speed clock distributions for transceivers in F324 and smaller packages, and in F484 and larger packages in bonded ($\times 2$ and $\times 4$) channel configuration.

Figure 1-36. Clock Distribution in Bonded ($\times 2$ and $\times 4$) Channel Configuration for Transceivers in F324 and Smaller Packages.



Notes to Figure 1-36:

- (1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
- (2) High-speed clock.
- (3) Low-speed clock.
- (4) Bonded common low-speed clock path.

Table 1-13. Automatic RX Phase Compensation FIFO Read Clock Selection (Part 2 of 2)

Channel Configuration		Quartus II Selection
Bonded	With rate match FIFO ⁽¹⁾	coreclkout clock feeds the FIFO read clock for the bonded channels. coreclkout clock is the common bonded low-speed clock, which also feeds the FIFO read clock and transmitter PCS in the bonded channels.
	Without rate match FIFO	rx_clkout clock feeds the FIFO read clock. rx_clkout is forwarded through the receiver channel from low-speed recovered clock, which also feeds the FIFO write clock.

Note to Table 1-13:

(1) Configuration with rate match FIFO is supported in transmitter and receiver operation.

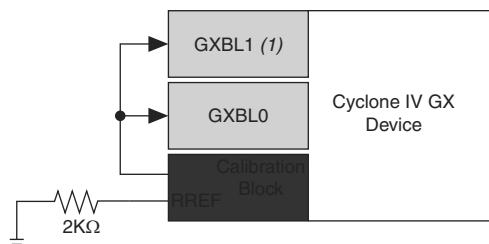
When using user-specified clock option, ensure that the clock feeding rx_coreclk port has 0 ppm difference with the RX phase compensation FIFO write clock.

Calibration Block

This block calibrates the OCT resistors and the analog portions of the transceiver blocks to ensure that the functionality is independent of process, voltage, and temperature (PVT) variations.

Figure 1-40 shows the location of the calibration block and how it is connected to the transceiver blocks.

Figure 1-40. Transceiver Calibration Blocks Location and Connection



Note to Figure 1-40:

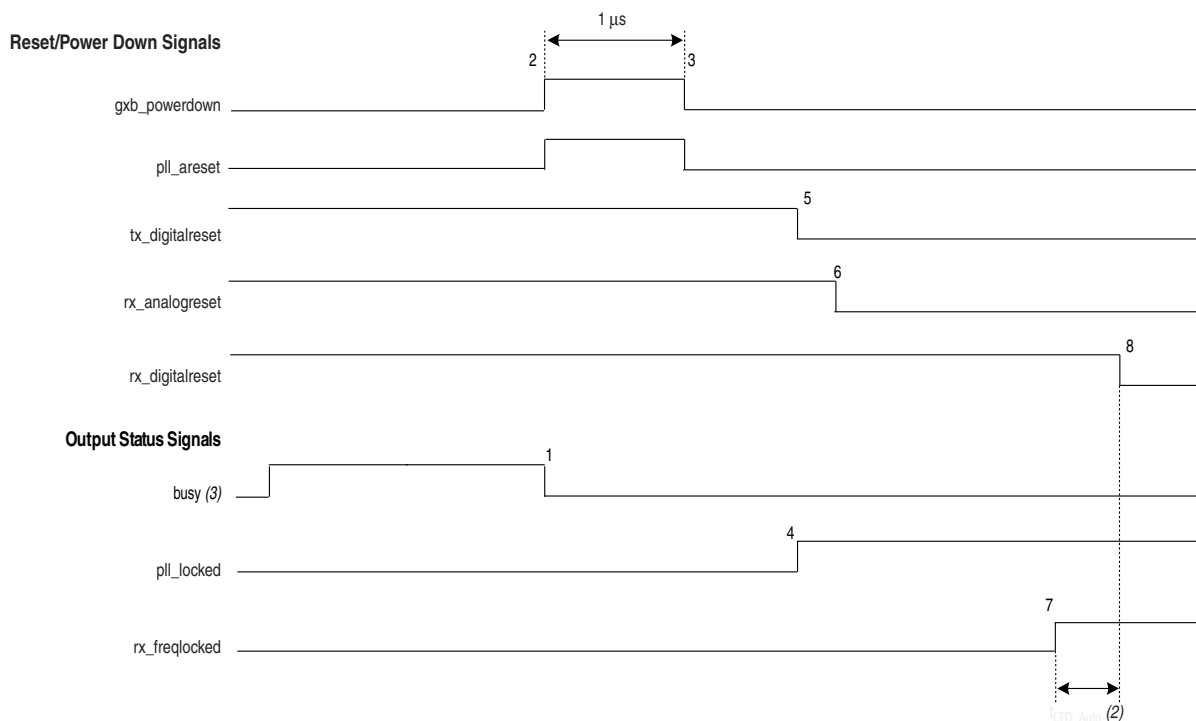
(1) Transceiver block GXBL1 is only available for devices in F484 and larger packages.

Table 1–29. Multipurpose PLL, General Purpose PLL and Miscellaneous Ports in ALTGX Megafunction for Cyclone IV GX (Part 2 of 2)

Block	Port Name	Input/Output	Clock Domain	Description
Reset & Power Down	gxb_powerdown	Input	Asynchronous signal	Transceiver block power down. <ul style="list-style-type: none"> When asserted, all digital and analog circuitry in the PCS, HSSI, CDR, and PCIe modules are powered down. Asserting the <code>gxb_powerdown</code> signal does not power down the <code>refclk</code> buffers.
	tx_digitalreset	Input	Asynchronous signal. The minimum pulse width is two parallel clock cycles.	Transmitter PCS reset. <ul style="list-style-type: none"> When asserted, the transmitter PCS blocks are reset.
	rx_analogreset	Input	Asynchronous signal. The minimum pulse width is two parallel clock cycles.	Receiver PMA reset. <ul style="list-style-type: none"> When asserted, analog circuitry in the receiver PMA block is reset.
	rx_digitalreset	Input	Asynchronous signal. The minimum pulse width is two parallel clock cycles.	Receiver PCS reset. <ul style="list-style-type: none"> When asserted, the receiver PCS blocks are reset.
Reconfiguration	reconfig_clk	Input	Clock signal	Dynamic reconfiguration clock. <ul style="list-style-type: none"> Also used for offset cancellation except in PIPE mode. For the supported frequency range for this clock, refer to the <i>Cyclone IV Device Data Sheet</i> chapter.
	reconfig_togxb	Input	Asynchronous signal	From the dynamic reconfiguration controller.
	reconfig_fromgxb	Output	Asynchronous signal	To the dynamic reconfiguration controller.
Calibration Block	cal_blk_clk	Input	Clock signal	Clock for the transceiver calibration block.
	cal_blk_powerdown	Input	Asynchronous signal	Calibration block power down control.
Test Mode	rx_bistdone	Output	Asynchronous signal	BIST or PRBS test completion indicator. <ul style="list-style-type: none"> A high level during BIST test mode indicates the verifier either receives complete pattern cycle or detects an error and stays asserted until being reset using the <code>rx_digitalreset</code> port. A high level during PRBS test mode indicates the verifier receives complete pattern cycle and stays asserted until being reset using the <code>rx_digitalreset</code> port.
	rx_bisterr	Output	Asynchronous signal	BIST or PRBS verifier error indicator <ul style="list-style-type: none"> In BIST test mode, the signal stays asserted upon detecting an error until being reset using the <code>rx_digitalreset</code> port. In PRBS test mode, the signal asserts for a minimum of 3 <code>rx_clkout</code> clock cycles upon detecting an error and deasserts if the following PRBS sequence contains no error.

The deassertion of the busy signal indicates proper completion of the offset cancellation process on the receiver channel.

Figure 2–13. Sample Reset Sequence of a Receiver and Transmitter Channels-Receiver CDR in Automatic Lock Mode with the Optional gxb_powerdown Signal ⁽¹⁾



Notes to Figure 2–13:

- (1) The gxb_powerdown signal must not be asserted during the offset cancellation sequence.
- (2) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.
- (3) The busy signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the busy signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

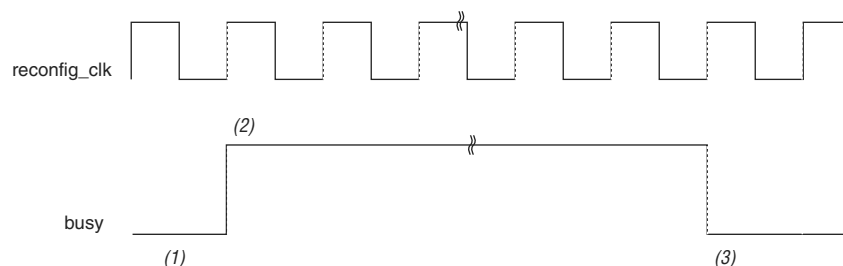
Simulation Requirements

The following are simulation requirements:

- The gxb_powerdown port is optional. In simulation, if the gxb_powerdown port is not instantiated, you must assert the tx_digitalreset, rx_digitalreset, and rx_analogreset signals appropriately for correct simulation behavior.
- If the gxb_powerdown port is instantiated, and the other reset signals are not used, you must assert the gxb_powerdown signal for at least 1 μ s for correct simulation behavior.
- You can deassert the rx_digitalreset signal immediately after the rx_freqlocked signal goes high to reduce the simulation run time. It is not necessary to wait for t_{LTD_Auto} (as suggested in the actual reset sequence).
- The busy signal is deasserted after about 20 parallel reconfig_clk clock cycles in order to reduce simulation run time. For silicon behavior in hardware, you can follow the reset sequences described in the previous pages.

Figure 3-3 shows the timing diagram for a offset cancellation process.

Figure 3-3. Dynamic Reconfiguration Signals Transition during Offset Cancellation



Notes to Figure 3-3:

- (1) After device power up, the `busy` signal remains low for the first `reconfig_clk` cycle.
- (2) The `busy` signal then gets asserted for the second `reconfig_clk` cycle, when the dynamic reconfiguration controller initiates the offset cancellation process.
- (3) The deassertion of the `busy` signal indicates the successful completion of the offset cancellation process.

Functional Simulation of the Offset Cancellation Process

You must connect the `ALTGX_RECONFIG` instances to the `ALTGX` instances in your design for functional simulation. Functional simulation uses a reduced timing model of the dynamic reconfiguration controller. Therefore, the duration of the offset cancellation process is 16 `reconfig_clk` clock cycles for functional simulation only. The `gxb_powerdown` signal must not be asserted during the offset cancellation sequence (for functional simulation and silicon).

Dynamic Reconfiguration Modes

When you enable the dynamic reconfiguration feature, you can reconfigure the following portions of each transceiver channel dynamically, without powering down the other transceiver channels or the FPGA fabric of the device:

- Analog (PMA) controls reconfiguration
- Channel reconfiguration
- PLL reconfiguration

Table 3-3 lists the supported dynamic reconfiguration modes for Cyclone IV GX devices.

Table 3-3. Cyclone IV GX Supported Dynamic Reconfiguration Mode (Part 1 of 2)

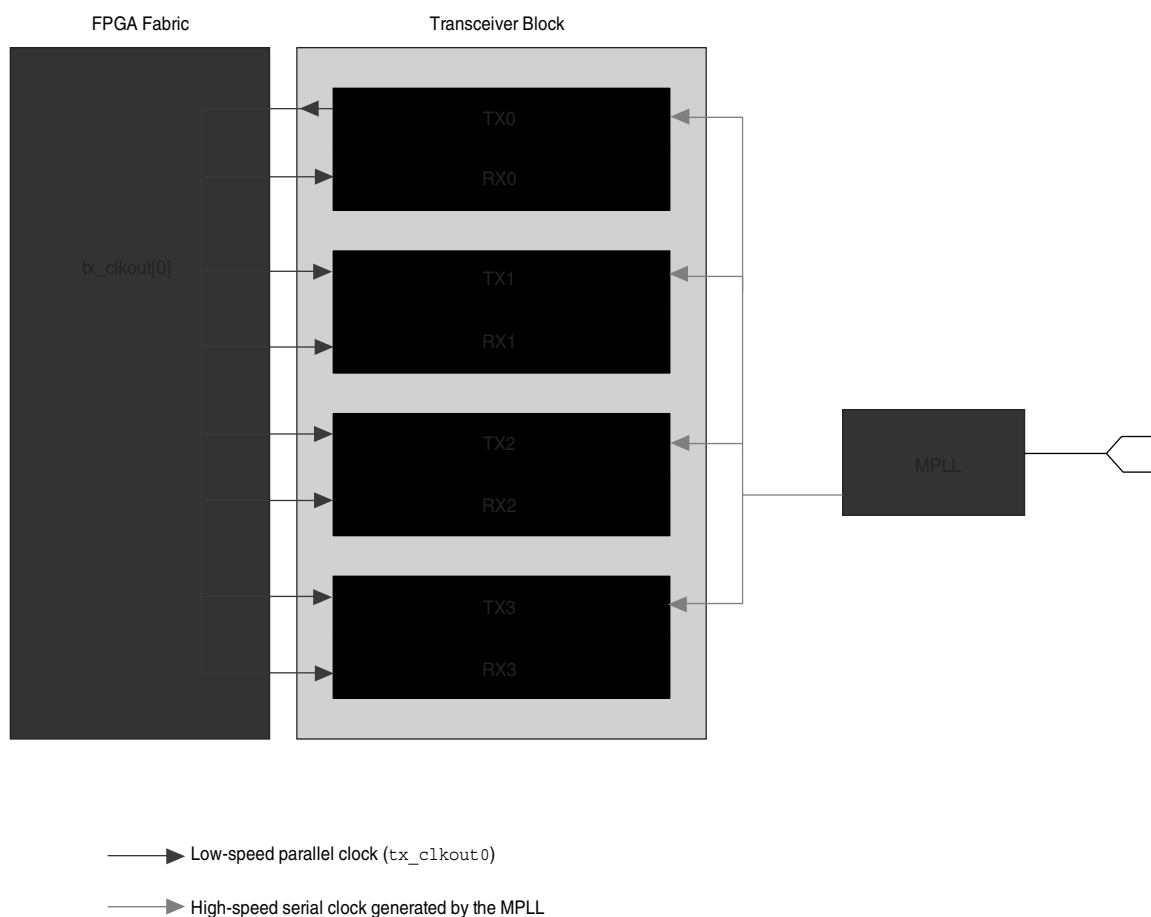
Dynamic Reconfiguration Supported Mode	Operational Mode			Quartus II Instances			.mif Requirements
	Transmitter Only	Receiver Only	Transmitter and Receiver Only	ALTGX	ALTGX_RECONFIG	ALTPLL_RECONFIG	
Offset Cancellation	—	✓	✓	✓	✓	—	—
Analog (PMA) Controls Reconfiguration	✓	✓	✓	✓	✓	—	—

Option 1: Share a Single Transmitter Core Clock Between Receivers

- Enable this option if you want tx_clkout of the first channel (channel 0) of the transceiver block to provide the read clock to the Receive Phase Compensation FIFOs of the remaining receiver channels in the transceiver block.
- This option is typically enabled when all the channels of a transceiver block are in a Basic or Protocol configuration with rate matching enabled and are reconfigured to another Basic or Protocol configuration with rate matching enabled.

Figure 3–13 shows the sharing of channel 0's tx_clkout between all four channels of a transceiver block.

Figure 3–13. Option 1 for Receiver Core Clocking (Channel Reconfiguration Mode)



This chapter provides additional information about the document and Altera.

About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® IV family of devices.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact ⁽¹⁾	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general) (software licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, D: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .
<i>italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pdf file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1-10 and Equation 1-1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1-10 lists the change percentage of the OCT resistance with voltage and temperature.

Table 1-10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices ⁽¹⁾

Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	-0.026
2.5	0.234	-0.039
1.8	0.219	-0.086
1.5	0.199	-0.136
1.2	0.161	-0.288

Note to Table 1-10:

(1) This specification is not applicable to EP4CGX15, EP4CGX22, and EP4CGX30 devices.

Equation 1-1. Final OCT Resistance ^{(1), (2), (3), (4), (5), (6)}

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV \text{ ——— (7)}$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \text{ ——— (8)}$$

$$\text{For } \Delta R_x < 0; MF_x = 1 / (|\Delta R_x|/100 + 1) \text{ ——— (9)}$$

$$\text{For } \Delta R_x > 0; MF_x = \Delta R_x/100 + 1 \text{ ——— (10)}$$

$$MF = MF_V \times MF_T \text{ ——— (11)}$$

$$R_{\text{final}} = R_{\text{initial}} \times MF \text{ ——— (12)}$$

Notes to Equation 1-1:

- (1) T_2 is the final temperature.
- (2) T_1 is the initial temperature.
- (3) MF is multiplication factor.
- (4) R_{final} is final resistance.
- (5) R_{initial} is initial resistance.
- (6) Subscript x refers to both V and T .
- (7) ΔR_V is a variation of resistance with voltage.
- (8) ΔR_T is a variation of resistance with temperature.
- (9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- (10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- (11) V_2 is final voltage.
- (12) V_1 is the initial voltage.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1-12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1-12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	V _{CCIO} = 3.3 V ± 5% ^{(2), (3)}	7	25	41	kΩ
		V _{CCIO} = 3.0 V ± 5% ^{(2), (3)}	7	28	47	kΩ
		V _{CCIO} = 2.5 V ± 5% ^{(2), (3)}	8	35	61	kΩ
		V _{CCIO} = 1.8 V ± 5% ^{(2), (3)}	10	57	108	kΩ
		V _{CCIO} = 1.5 V ± 5% ^{(2), (3)}	13	82	163	kΩ
		V _{CCIO} = 1.2 V ± 5% ^{(2), (3)}	19	143	351	kΩ
R _{PD}	Value of the I/O pin pull-down resistor before and during configuration	V _{CCIO} = 3.3 V ± 5% ⁽⁴⁾	6	19	30	kΩ
		V _{CCIO} = 3.0 V ± 5% ⁽⁴⁾	6	22	36	kΩ
		V _{CCIO} = 2.5 V ± 5% ⁽⁴⁾	6	25	43	kΩ
		V _{CCIO} = 1.8 V ± 5% ⁽⁴⁾	7	35	71	kΩ
		V _{CCIO} = 1.5 V ± 5% ⁽⁴⁾	8	50	112	kΩ

Notes to Table 1-12:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (3) $R_{PU} = (V_{CCIO} - V_I) / I_{R_{PU}}$
Minimum condition: -40°C; V_{CCIO} = V_{CC} + 5%, V_I = V_{CC} + 5% - 50 mV;
Typical condition: 25°C; V_{CCIO} = V_{CC}, V_I = 0 V;
Maximum condition: 100°C; V_{CCIO} = V_{CC} - 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.
- (4) $R_{PD} = V_I / I_{R_{PD}}$
Minimum condition: -40°C; V_{CCIO} = V_{CC} + 5%, V_I = 50 mV;
Typical condition: 25°C; V_{CCIO} = V_{CC}, V_I = V_{CC} - 5%;
Maximum condition: 100°C; V_{CCIO} = V_{CC} - 5%, V_I = V_{CC} - 5%; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 1-13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1-13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Parameter	Maximum
I _{IOPIN(DC)}	DC current per I/O pin	300 μA
I _{IOPIN(AC)}	AC current per I/O pin	8 mA ⁽¹⁾
I _{XCVRTX(DC)}	DC current per transceiver TX pin	100 mA
I _{XCVRRX(DC)}	DC current per transceiver RX pin	50 mA

Note to Table 1-13:

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.



During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 2 of 2)

Device	Performance								Unit
	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	I7	I8L ⁽¹⁾	A7	
EP4CE55	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE75	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE115	—	437.5	402	362	265	437.5	362	—	MHz
EP4CGX15	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX22	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX30	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX50	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX75	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX110	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX150	500	437.5	402	—	—	437.5	—	—	MHz

Note to Table 1–24:

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

PLL Specifications

Table 1–25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C). For more information about the PLL block, refer to “Glossary” on page 1–37.

Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(3)}$	Input clock frequency (–6, –7, –8 speed grades)	5	—	472.5	MHz
	Input clock frequency (–8L speed grade)	5	—	362	MHz
	Input clock frequency (–9L speed grade)	5	—	265	MHz
f_{INPFD}	PFD input frequency	5	—	325	MHz
$f_{VCO}^{(4)}$	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER_CCJ}^{(5)}$	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	—	—	0.15	UI
	$F_{REF} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} (external clock output) ⁽³⁾	PLL output frequency	—	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	—	—	472.5	MHz
	PLL output frequency (–7 speed grade)	—	—	450	MHz
	PLL output frequency (–8 speed grade)	—	—	402.5	MHz
	PLL output frequency (–8L speed grade)	—	—	362	MHz
	PLL output frequency (–9L speed grade)	—	—	265	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms

Table 1-46. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage.
	$V_{IL(DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX(AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF(AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
	$V_{REF(DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING(AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING(DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V_{TT}	Termination voltage for the SSTL and HSTL I/O standards.
	$V_X(AC)$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—