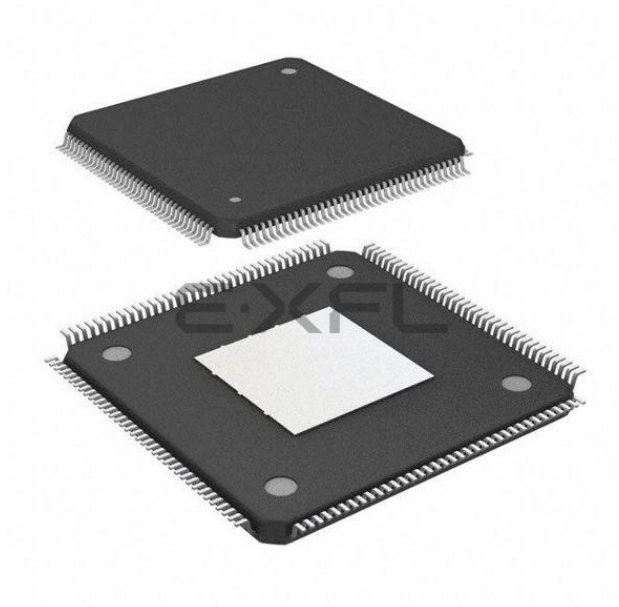


**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 963 |
| Number of Logic Elements/Cells | 15408 |
| Total RAM Bits | 516096 |
| Number of I/O | 81 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | 144-EQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4ce15e22c6 |

- Up to 532 user I/Os
  - LVDS interfaces up to 840 Mbps transmitter (Tx), 875 Mbps Rx
  - Support for DDR2 SDRAM interfaces up to 200 MHz
  - Support for QDRII SRAM and DDR SDRAM up to 167 MHz
- Up to eight phase-locked loops (PLLs) per device
- Offered in commercial and industrial temperature grades

# Device Resources

Table 1–1 lists Cyclone IV E device resources.

**Table 1–1. Resources for the Cyclone IV E Device Family**

| Resources | EP4CE6 | EP4CE10 | EP4CE15 | EP4CE22 | EP4CE30 | EP4CE40 | EP4CE55 | EP4CE75 | EP4CE115 |
|---|---|---|---|---|---|---|---|---|---|
| Logic elements (LEs) | 6,272 | 10,320 | 15,408 | 22,320 | 28,848 | 39,600 | 55,856 | 75,408 | 114,480 |
| Embedded memory (Kbits) | 270 | 414 | 504 | 594 | 594 | 1,134 | 2,340 | 2,745 | 3,888 |
| Embedded 18 × 18 multipliers | 15 | 23 | 56 | 66 | 66 | 116 | 154 | 200 | 266 |
| General-purpose PLLs | 2 | 2 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Global Clock Networks | 10 | 10 | 20 | 20 | 20 | 20 | 20 | 20 | 20 |
| User I/O Banks | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Maximum user I/O (1) | 179 | 179 | 343 | 153 | 532 | 532 | 374 | 426 | 528 |

**Note to Table 1–1:**

(1) The user I/Os count from pin-out files includes all general purpose I/O, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

# Cyclone IV Device Family Speed Grades

Table 1–5 lists the Cyclone IV GX devices speed grades.

**Table 1–5. Speed Grades for the Cyclone IV GX Device Family**

| Device | F169 | F324 | F484 | F672 | F896 |
|---|---|---|---|---|---|
| EP4CGX15 | C6, C7, C8, I7 | — | — | — | — |
| EP4CGX22 | C6, C7, C8, I7 | C6, C7, C8, I7 | — | — | — |
| EP4CGX30 | C6, C7, C8, I7 | C6, C7, C8, I7 | C6, C7, C8, I7 | — | — |
| EP4CGX50 | — | — | C6, C7, C8, I7 | C6, C7, C8, I7 | — |
| EP4CGX75 | — | — | C6, C7, C8, I7 | C6, C7, C8, I7 | — |
| EP4CGX110 | — | — | C7, C8, I7 | C7, C8, I7 | C7, C8, I7 |
| EP4CGX150 | — | — | C7, C8, I7 | C7, C8, I7 | C7, C8, I7 |

Table 1–6 lists the Cyclone IV E devices speed grades.

**Table 1–6. Speed Grades for the Cyclone IV E Device Family** *(1), (2)*

| Device | E144 | M164 | M256 | U256 | F256 | F324 | U484 | F484 | F780 |
|---|---|---|---|---|---|---|---|---|---|
| EP4CE6 | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | — | — |
| EP4CE10 | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | — | — |
| EP4CE15 | C8L, C9L, I8L C6, C7, C8, I7 | I7N | C7N, I7N | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | C8L, C9L, I8L C6, C7, C8, I7, A7 | — |
| EP4CE22 | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | — | — |
| EP4CE30 | — | — | — | — | — | A7N | — | C8L, C9L, I8L C6, C7, C8, I7, A7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE40 | — | — | — | — | — | A7N | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE55 | — | — | — | — | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE75 | — | — | — | — | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE115 | — | — | — | — | — | — | — | C8L, C9L, I8L C7, C8, I7 | C8L, C9L, I8L C7, C8, I7 |

**Notes to Table 1–6:**

(1) C8L, C9L, and I8L speed grades are applicable for the 1.0-V core voltage.

(2) C6, C7, C8, I7, and A7 speed grades are applicable for the 1.2-V core voltage.

## I/O Features

Cyclone IV device I/O supports programmable bus hold, programmable pull-up resistors, programmable delay, programmable drive strength, programmable slew-rate control to optimize signal integrity, and hot socketing. Cyclone IV devices support calibrated on-chip series termination (Rs OCT) or driver impedance matching (Rs) for single-ended I/O standards. In Cyclone IV GX devices, the high-speed transceiver I/Os are located on the left side of the device. The top, bottom, and right sides can implement general-purpose user I/Os.

Table 1–8 lists the I/O standards that Cyclone IV devices support.

**Table 1–8. I/O Standards Support for the Cyclone IV Device Family**

| Type | I/O Standard |
|---|---|
| Single-Ended I/O | LVTTL, LVCMOS, SSTL, HSTL, PCI, and PCI-X |
| Differential I/O | SSTL, HSTL, LVPECL, BLVDS, LVDS, mini-LVDS, RSDS, and PPDS |

The LVDS SERDES is implemented in the core of the device using logic elements.

For more information, refer to the *I/O Features in Cyclone IV Devices* chapter.

## Clock Management

Cyclone IV devices include up to 30 global clock (GCLK) networks and up to eight PLLs with five outputs per PLL to provide robust clock management and synthesis. You can dynamically reconfigure Cyclone IV device PLLs in user mode to change the clock frequency or phase.

Cyclone IV GX devices support two types of PLLs: multipurpose PLLs and general-purpose PLLs:

- Use multipurpose PLLs for clocking the transceiver blocks. You can also use them for general-purpose clocking when they are not used for transceiver clocking.
- Use general purpose PLLs for general-purpose applications in the fabric and periphery, such as external memory interfaces. Some of the general purpose PLLs can support transceiver clocking.

For more information, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.

## External Memory Interfaces

Cyclone IV devices support SDR, DDR, DDR2 SDRAM, and QDRII SRAM interfaces on the top, bottom, and right sides of the device. Cyclone IV E devices also support these interfaces on the left side of the device. Interfaces may span two or more sides of the device to allow more flexible board design. The Altera® DDR SDRAM memory interface solution consists of a PHY interface and a memory controller. Altera supplies the PHY IP and you can use it in conjunction with your own custom memory controller or an Altera-provided memory controller. Cyclone IV devices support the use of error correction coding (ECC) bits on DDR and DDR2 SDRAM interfaces.

**Table 3–3. Cyclone IV Devices M9K Block Mixed-Width Configurations (Simple Dual-Port Mode) *(Part 2 of 2)***

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 8192 × 1 | 4096 × 2 | 2048 × 4 | 1024 × 8 | 512 × 16 | 256 × 32 | 1024 × 9 | 512 × 18 | 256 × 36 |
| 512 × 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 256 × 32 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | — |
| 1024 × 9 | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| 512 × 18 | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| 256 × 36 | — | — | — | — | — | — | ✓ | ✓ | ✓ |

In simple dual-port mode, M9K memory blocks support separate `wren` and `rden` signals. You can save power by keeping the `rden` signal low (inactive) when not reading. Read-during-write operations to the same address can either output "Don't Care" data at that location or output "Old Data". To choose the desired behavior, set the **Read-During-Write** option to either **Don't Care** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to "Read-During-Write Operations" on page 3–15.

Figure 3–9 shows the timing waveform for read and write operations in simple dual-port mode with unregistered outputs. Registering the outputs of the RAM simply delays the `q` output by one clock cycle.

**Figure 3–9. Cyclone IV Devices Simple Dual-Port Timing Waveform**

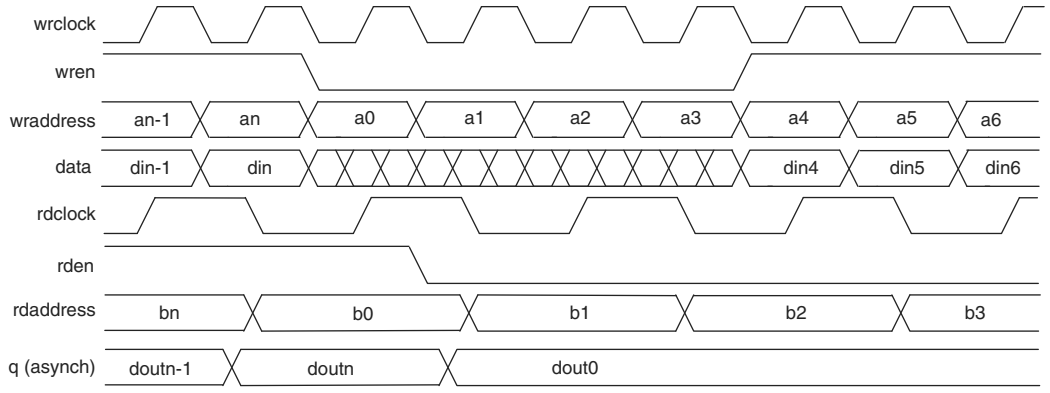


Table 4–2 lists the sign of the multiplication results for the various operand sign representations. The results of the multiplication are signed if any one of the operands is a signed value.

**Table 4–2. Multiplier Sign Representation**

| Data A | | Data B | | Result |
|---|---|---|---|---|
| signa Value | Logic Level | signb Value | Logic Level | |
| Unsigned | Low | Unsigned | Low | Unsigned |
| Unsigned | Low | Signed | High | Signed |
| Signed | High | Unsigned | Low | Signed |
| Signed | High | Signed | High | Signed |

Each embedded multiplier block has only one `signa` and one `signb` signal to control the sign representation of the input data to the block. If the embedded multiplier block has two 9 × 9 multipliers, the `Data A` input of both multipliers share the same `signa` signal, and the `Data B` input of both multipliers share the same `signb` signal. You can dynamically change the `signa` and `signb` signals to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision, regardless of the sign representation.

☞ When the `signa` and `signb` signals are unused, the Quartus II software sets the multiplier to perform unsigned multiplication by default.

## Output Registers

You can register the embedded multiplier output with output registers in either 18- or 36-bit sections, depending on the operational mode of the multiplier. The following control signals are available for each output register in the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers in a single embedded multiplier are fed by the same clock, clock enable, and asynchronous clear signals.

# Operational Modes

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

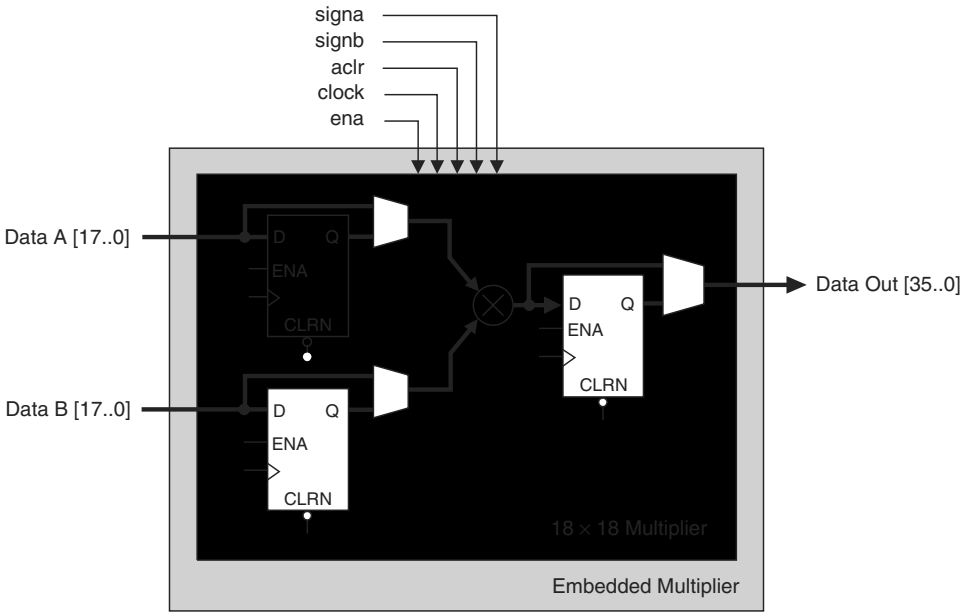
☞ You can also use embedded multipliers of Cyclone IV devices to implement multiplier adder and multiplier accumulator functions, in which the multiplier portion of the function is implemented with embedded multipliers, and the adder or accumulator function is implemented in logic elements (LEs).

## 18-Bit Multipliers

You can configure each embedded multiplier to support a single 18 × 18 multiplier for input widths of 10 to 18 bits.

Figure 4–3 shows the embedded multiplier configured to support an 18-bit multiplier.

**Figure 4–3. 18-Bit Multiplier Mode**




All 18-bit multiplier inputs and results are independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Also, you can dynamically change the `signa` and `signb` signals and send these signals through dedicated input registers.

**Table 6–2. Cyclone IV Device I/O Features Support (Part 2 of 2)**

| I/O Standard | IOH/IOL Current Strength Setting (mA) (1), (9) | | $R_S$ OCT with Calibration Setting, Ohm (Ω) | | $R_S$ OCT Without Calibration Setting, Ohm (Ω) | | Cyclone IV E I/O Banks Support | Cyclone IV GX I/O Banks Support | Slew Rate Option (6) | PCI-clamp Diode Support |
|---|---|---|---|---|---|---|---|---|---|---|
| | Column I/O | Row I/O | Column I/O | Row I/O (8) | Column I/O | Row I/O (8) | | | | |
| BLVDS | 8,12,16 | 8,12,16 | — | — | — | — | 1,2,3,4, 5,6,7,8 | 3,4,5,6, 7,8 | 0,1,**2** | — |
| LVDS (3) | — | — | — | — | — | — | | 5,6 | — | — |
| PPDS (3), (4) | — | — | — | — | — | — | | | — | — |
| RSDS and mini-LVDS (3), (4) | — | — | — | — | — | — | | | — | — |
| Differential LVPECL (5) | — | — | — | — | — | — | | 3,4,5,6, 7,8 | — | — |

**Notes to Table 6–2:**

(1) The default current strength setting in the Quartus II software is 50-Ω OCT without calibration for all non-voltage reference and HSTL/SSTL Class I I/O standards. The default setting is 25-Ω OCT without calibration for HSTL/SSTL Class II I/O standards.

(2) The differential SSTL-18 and SSTL-2, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards are supported only on clock input pins and PLL output clock pins.

(3) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only for Cyclone IV E devices and right I/O banks 5 and 6 only for Cyclone IV GX devices. Differential outputs in column I/O banks require an external resistor network.

(4) This I/O standard is supported for outputs only.

(5) This I/O standard is supported for clock inputs only

(6) The default Quartus II slew rate setting is in bold; **2** for all I/O standards that supports slew rate option.

(7) Differential SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards do not support Class II output.

(8) Cyclone IV GX devices only support right I/O pins.

(9) Altera not only offers current strength that meets the industrial standard specification but also other additional current strengths.

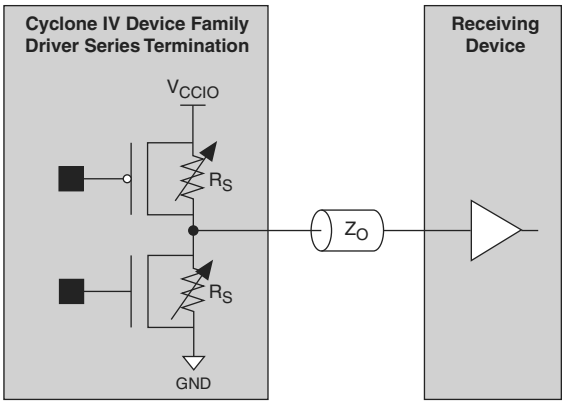
☞ For more details about the differential I/O standards supported in Cyclone IV I/O banks, refer to "High-Speed I/O Interface" on page 6–24.

## On-Chip Series Termination with Calibration

Cyclone IV devices support $R_S$ OCT with calibration in the top, bottom, and right I/O banks. The $R_S$ OCT calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the I/O buffer impedance until they match (as shown in Figure 6–2).

The $R_S$ shown in Figure 6–2 is the intrinsic impedance of the transistors that make up the I/O buffer.

**Figure 6–2. Cyclone IV Devices $R_S$ OCT with Calibration**




OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in each of I/O banks 2, 4, 5, and 7 for Cyclone IV E devices and I/O banks 4, 5, and 7 for Cyclone IV GX devices. Each calibration block supports each side of the I/O banks. Because there are two I/O banks sharing the same calibration block, both banks must have the same $V_{CCIO}$ if both banks enable OCT calibration. If two related banks have different $V_{CCIO}$, only the bank in which the calibration block resides can enable OCT calibration.

Figure 6–10 on page 6–18 shows the top-level view of the OCT calibration blocks placement.

Each calibration block comes with a pair of RUP and RDN pins. When used for calibration, the RUP pin is connected to $V_{CCIO}$ through an external 25-Ω ±1% or 50-Ω ±1% resistor for an $R_S$ OCT value of 25 Ω or 50 Ω, respectively. The RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an $R_S$ OCT value of 25 Ω or 50 Ω, respectively. The external resistors are compared with the internal resistance using comparators. The resultant outputs of the comparators are used by the OCT calibration block to dynamically adjust buffer impedance.

☞ During calibration, the resistance of the RUP and RDN pins varies.

**Table 8–4. Configuration Schemes for Cyclone IV GX Devices (EP4CGX30 [only for F484 package], EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150) (Part 2 of 2)**

| Configuration Scheme | MSEL3 | MSEL2 | MSEL1 | MSEL0 | POR Delay | Configuration Voltage Standard (V) (1) |
|---|---|---|---|---|---|---|
| JTAG-based configuration (2) | (3) | (3) | (3) | (3) | — | — |

**Notes to Table 8–4:**

(1) Configuration voltage standard applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating. Connect them to $V_{CCA}$ or GND. These pins support the non-JTAG configuration scheme used in production. Altera recommends connecting the MSEL pins to GND if your device is only using JTAG configuration.

Smaller Cyclone IV E devices or package options (E144 and F256 packages) do not have the MSEL[3] pin. The AS Fast POR configuration scheme at 3.0- or 2.5-V configuration voltage standard and the AP configuration scheme are not supported in Cyclone IV E devices without the MSEL[3] pin. To configure these devices with other supported configuration schemes, select MSEL[2..0] pins according to the MSEL settings in Table 8–5.

**Table 8–5. Configuration Schemes for Cyclone IV E Devices**

| Configuration Scheme | MSEL3 | MSEL2 | MSEL1 | MSEL0 | POR Delay | Configuration Voltage Standard (V) (1) |
|---|---|---|---|---|---|---|
| AS | 1 | 1 | 0 | 1 | Fast | 3.3 |
| | 0 | 1 | 0 | 0 | Fast | 3.0, 2.5 |
| | 0 | 0 | 1 | 0 | Standard | 3.3 |
| | 0 | 0 | 1 | 1 | Standard | 3.0, 2.5 |
| AP | 0 | 1 | 0 | 1 | Fast | 3.3 |
| | 0 | 1 | 1 | 0 | Fast | 1.8 |
| | 0 | 1 | 1 | 1 | Standard | 3.3 |
| | 1 | 0 | 1 | 1 | Standard | 3.0, 2.5 |
| | 1 | 0 | 0 | 0 | Standard | 1.8 |
| PS | 1 | 1 | 0 | 0 | Fast | 3.3, 3.0, 2.5 |
| | 0 | 0 | 0 | 0 | Standard | 3.3, 3.0, 2.5 |
| FPP | 1 | 1 | 1 | 0 | Fast | 3.3, 3.0, 2.5 |
| | 1 | 1 | 1 | 1 | Fast | 1.8, 1.5 |
| JTAG-based configuration (2) | (3) | (3) | (3) | (3) | — | — |

**Notes to Table 8–5:**

(1) Configuration voltage standard applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating. Connect them to $V_{CCA}$ or GND. These pins support the non-JTAG configuration scheme used in production. Altera recommends connecting the MSEL pins to GND if your device is only using JTAG configuration.

The nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

## Guidelines for Connecting Parallel Flash to Cyclone IV E Devices for an AP Interface

For single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and Cyclone IV E devices must follow the recommendations listed in Table 8–11. These recommendations also apply to an AP configuration with multiple bus masters.

**Table 8–11. Maximum Trace Length and Loading for AP Configuration**

| Cyclone IV E AP Pins | Maximum Board Trace Length from Cyclone IV E Device to Flash Device (inches) | Maximum Board Load (pF) |
|---|---|---|
| DCLK | 6 | 15 |
| DATA[15..0] | 6 | 30 |
| PADD[23..0] | 6 | 30 |
| nRESET | 6 | 30 |
| Flash_nCE | 6 | 30 |
| nOE | 6 | 30 |
| nAVD | 6 | 30 |
| nWE | 6 | 30 |
| I/O (1) | 6 | 30 |

**Note to Table 8–11:**

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

## Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, the master must assert nCONFIG low for at least 500 ns to reset the master Cyclone IV E device and override the weak 10-kΩ pull-down resistor on the nCE pin. This resets the master Cyclone IV E device and causes it to tri-state its AP configuration bus. The other master device then takes control of the AP configuration bus. After the other master device is done, it releases the AP configuration bus, then releases the nCE pin, and finally pulses nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

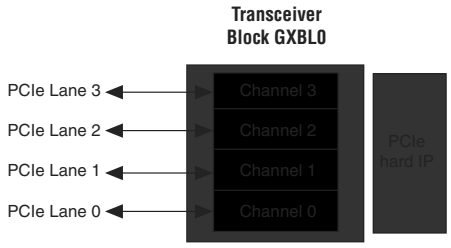
When Cyclone IV devices successfully load the application configuration, they enter user mode. In user mode, the soft logic (the Nios II processor or state machine and the remote communication interface) assists the Cyclone IV device in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and starts system reconfiguration.

The hard IP block supports 1, 2, or 4 initial lane configurations with a maximum payload of 256 bytes at Gen1 frequency. The application interface is 64 bits with a data width of 16 bits per channel running at up to 125 MHz. As a hard macro and a verified block, it uses very few FPGA resources, while significantly reducing design risk and the time required to achieve timing closure. It is compliant with the PCI Express Base Specification 1.1. You do not have to pay a licensing fee to use this module. Configuring the hard IP block requires using the PCI Express Compiler.

For more information about the hard IP block, refer to the *PCI Express Compiler User Guide*.

Figure 1–43 shows the lane placement requirements when implementing PCIe with hard IP block.

**Figure 1–43. PCIe with Hard IP Block Lane Placement Requirements (1)**




**Note to Figure 1–43:**

(1) Applicable for PCIe ×1, ×2, and ×4 implementations with hard IP blocks only.

# Transceiver Functional Modes

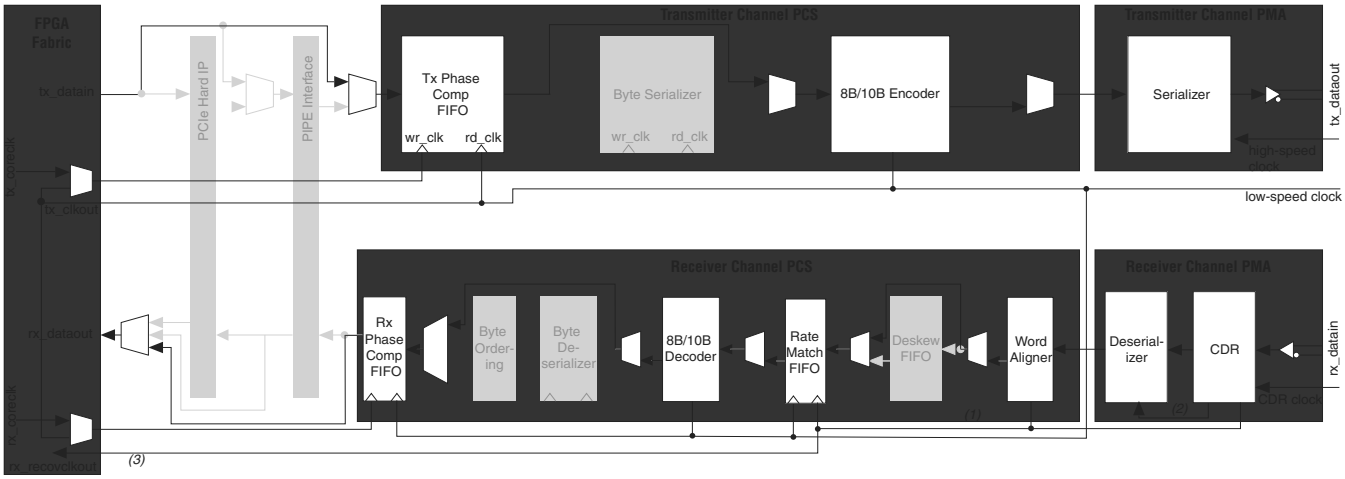
The Cyclone IV GX transceiver supports the functional modes as listed in Table 1–14 for protocol implementation.

**Table 1–14. Transceiver Functional Modes for Protocol Implementation (Part 1 of 2)**

| Functional Mode | Protocol | Key Feature | Reference |
|---|---|---|---|
| Basic | Proprietary, SATA, V-by-One, Display Port | Low latency PCS, transmitter in electrical idle, signal detect at receiver, wider spread asynchronous SSC | "Basic Mode" on page 1–48 |
| PCI Express (PIPE) | PCIe Gen1 with PIPE Interface | PIPE ports, receiver detect, transmitter in electrical idle, electrical idle inference, signal detect at receiver, fast recovery, protocol-compliant word aligner and rate match FIFO, synchronous SSC | "PCI Express (PIPE) Mode" on page 1–52 |
| GIGE | GbE | Running disparity preservation, protocol-compliant word aligner, recovered clock port for applications such as Synchronous Ethernet | "GIGE Mode" on page 1–59 |
| Serial RapidIO | SRIO | Protocol-compliant word aligner | "Serial RapidIO Mode" on page 1–64 |
| XAUI | XAUI | Deskew FIFO, protocol-compliant word aligner and rate match FIFO | "XAUI Mode" on page 1–67 |

Figure 1–55 shows the transceiver channel datapath and clocking when configured in GIGE mode.

**Figure 1–55. Transceiver Channel Datapath and Clocking when Configured in GIGE Mode**




**Notes to Figure 1–55:**

(1) Low-speed recovered clock.

(2) High-speed recovered clock.

(3) Optional `rx_recovclkout` port from CDR low-speed recovered clock is available for applications such as Synchronous Ethernet.

**Table 1–21. XGMII Character to PCS Code Groups Mapping (Part 2 of 2)**

| XGMII TXC (1) | XGMII TXD (2), (3) | PCS Code Group | Description |
|---|---|---|---|
| 1 | Any other value | K30.7 | Invalid XGMII character |

**Notes to Table 1–21:**

(1) Equivalent to `tx_ctrlenable` port.
(2) Equivalent to 8-bit input data to 8B/10B encoder.
(3) The values in XGMII TXD column are in hexadecimal.

8B/10B decoder in the receiver datapath maps received PCS code groups into specific 8-bit XGMII codes as listed in Table 1–22.

**Table 1–22. PCS Code Groups to XGMII Character Mapping**

| XGMII RXC (1) | XGMII RXD (2), (3) | PCS Code Group | Description |
|---|---|---|---|
| 0 | 00 through FF | Dxx,y | Normal data transmission |
| 1 | 07 | K28.0, K28.3, or K28.5 | Idle in \|\|I\|\| |
| 1 | 07 | K28.5 | Idle in \|\|T\|\| |
| 1 | 9C | K28.4 | Sequence |
| 1 | FB | K27.7 | Start |
| 1 | FD | K29.7 | Terminate |
| 1 | FE | K30.7 | Error |
| 1 | FE | Invalid code group | Received code group |

**Notes to Table 1–22:**

(1) Equivalent to `rx_ctrlenable` port.
(2) Equivalent to 8-bit input data to 8B/10B encoder.
(3) The values in XGMII RXD column are in hexadecimal.

## Channel Deskewing

The deskew FIFO in each of the four lanes expects to receive /A/ code group simultaneously on all four channels during the inter-packet gap, as required by XAUI protocol. The skew introduced in the physical medium and the receiver channels might cause the /A/ code group to be received misaligned with respect to each other.

The deskew FIFO works to align the /A/ code group across the four channels, which operation is compliant to the PCS deskew state machine diagram specified in clause 48 of the IEEE P802.3ae specification. The deskew operation begins after link synchronization is achieved on all four channels as indicated by the word aligner in each channel. The following are the deskew FIFO operations:

- Until the first /A/ code group is received, the deskew FIFO read and write pointers in each channel are not incremented.
- After the first /A/ code group is received, the write pointer starts incrementing for each word received but the read pointer is frozen.
- When all the four channels received the /A/ code group within 10 recovered clock cycles of each other, the read pointer of all four deskew FIFOs is released simultaneously, aligning the /A/ code group of all four channels in a column.

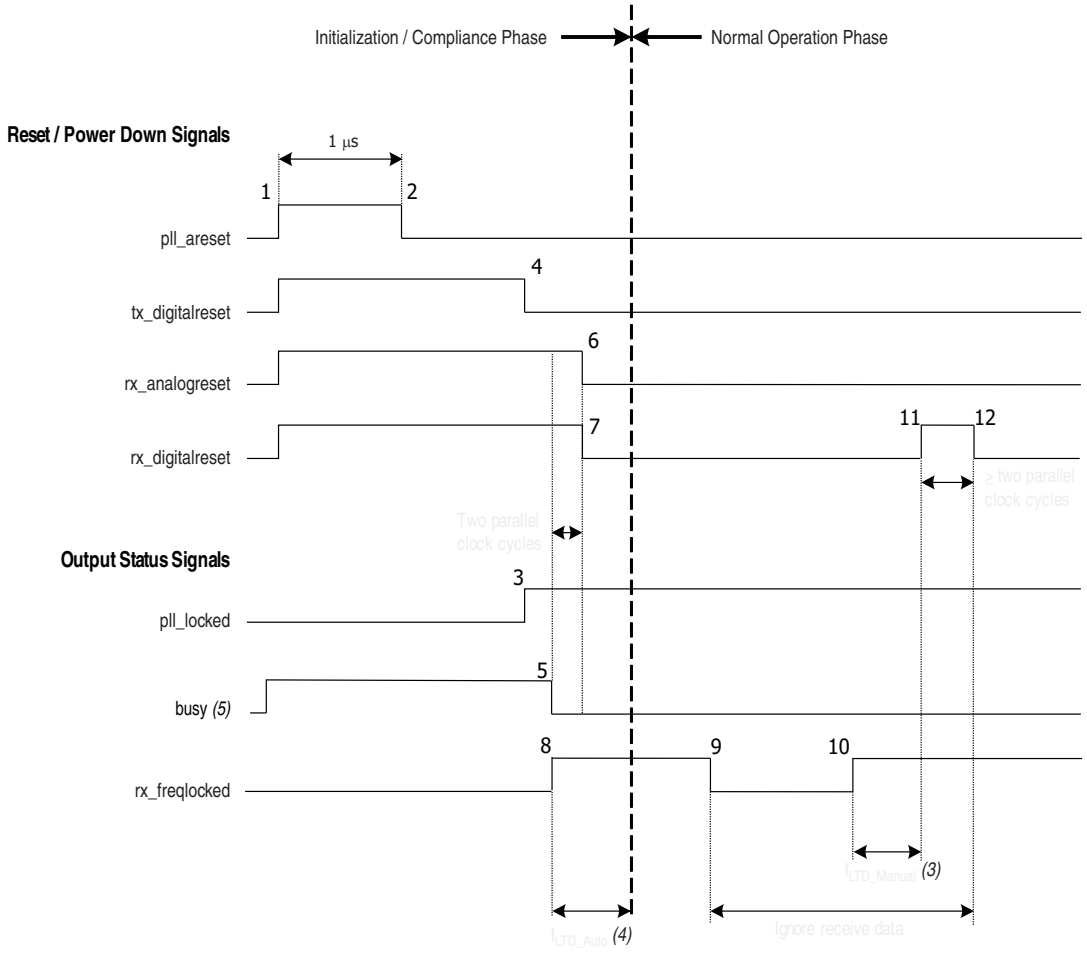
# PCIe Functional Mode

You can configure PCIe functional mode with or without the receiver clock rate compensation FIFO in the Cyclone IV GX device. The reset sequence remains the same whether or not you use the receiver clock rate compensation FIFO.

## PCIe Reset Sequence

The PCIe protocol consists of an initialization/compliance phase and a normal operation phase. The reset sequences for these two phases are described based on the timing diagram in Figure 2–10.

**Figure 2–10. Reset Sequence of PCIe Functional Mode (1), (2)**




**Notes to Figure 2–10:**

(1) This timing diagram is drawn based on the PCIe Gen 1 ×1 mode.

(2) For bonded PCIe Gen 1 ×2 and ×4 modes, there will be additional `rx_freqlocked[n]` signal. n=number of channels.

(3) For $t_{LTD\_Manual}$ duration, refer to the *Cyclone IV Device Datasheet* chapter.

(4) For $t_{LTD\_Auto}$ duration, refer to the *Cyclone IV Device Datasheet* chapter.

(5) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

Table 3–5 describes the rx_dataoutfull[31..0] FPGA fabric-Transceiver channel interface signals.

**Table 3–5. rx_dataoutfull[31..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions (Part 1 of 3)**

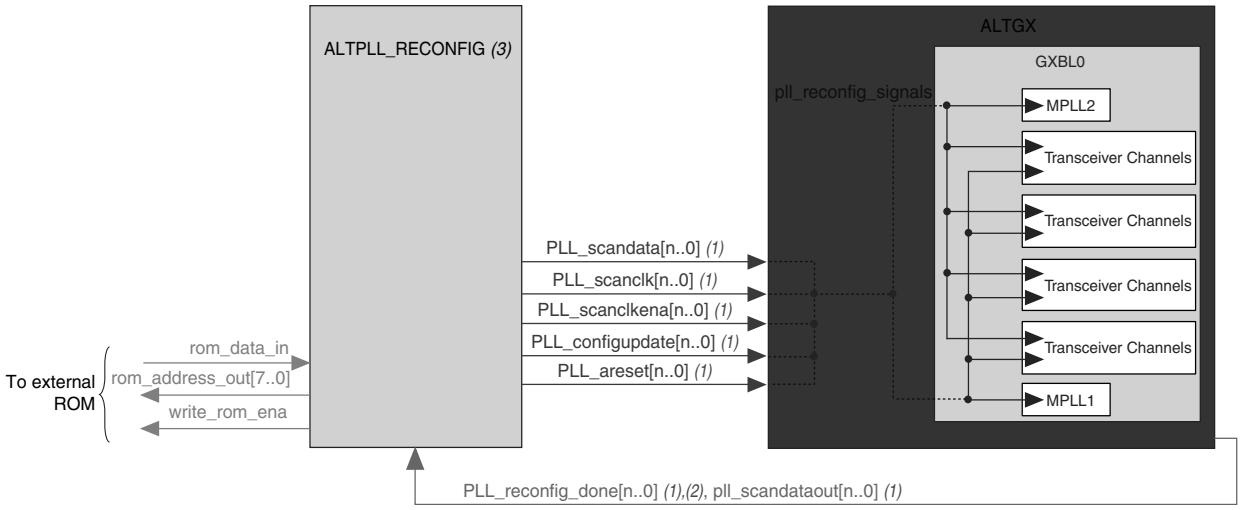
| FPGA Fabric-Transceiver Channel Interface Description | Receive Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths) |
|---|---|
| 8-bit FPGA fabric-Transceiver Channel Interface | **The following signals are used in 8-bit 8B/10B modes:** |
| | rx_dataoutfull[7:0]: 8-bit decoded data (rx_dataout) |
| | rx_dataoutfull[8]: Control bit (rx_ctrldetect) |
| | rx_dataoutfull[9]: Code violation status signal (rx_errdetect) |
| | rx_dataoutfull[10]: rx_syncstatus |
| | rx_dataoutfull[11]: Disparity error status signal (rx_disperr) |
| | rx_dataoutfull[12]: Pattern detect status signal (rx_patterndetect) |
| | rx_dataoutfull[13]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes. |
| | rx_dataoutfull[14]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes. |
| | rx_dataoutfull[14:13]: PCI Express (PIPE) functional mode (rx_pipestatus) |
| | rx_dataoutfull[15]: 8B/10B running disparity indicator (rx_runningdisp) |
| 10-bit FPGA fabric-Transceiver Channel Interface | rx_dataoutfull[9:0]: 10-bit un-encoded data (rx_dataout) |
| | rx_dataoutfull[10]: rx_syncstatus |
| | rx_dataoutfull[11]: 8B/10B disparity error indicator (rx_disperr) |
| | rx_dataoutfull[12]: rx_patterndetect |
| | rx_dataoutfull[13]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes |
| | rx_dataoutfull[14]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes |
| | rx_dataoutfull[15]: 8B/10B running disparity indicator (rx_runningdisp) |

The .**mif** files carries the reconfiguration information that will be used to reconfigure the multipurpose PLL or general purpose PLL dynamically. The .**mif** contents is generated automatically when you select the **Enable PLL Reconfiguration** option in the **Reconfiguration Setting** in ALTGX instances. The **.mif** files will be generated based on the data rate and input reference clock setting in the ALTGX MegaWizard. You must use the external ROM and feed its content to the ALTPLL_RECONFIG megafunction to reconfigure the multipurpose PLL setting.

For more information about instantiating the ALTPLL_Reconfig, refer to the *AN 609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices*.

Figure 3–16 shows the connection for PLL reconfiguration mode.

**Figure 3–16. ALTGX and ALTPLL_RECONFIG Connection for PLL Reconfiguration Mode**




**Notes to Figure 3–16:**

(1) *<n>* = (number of transceiver PLLs configured in the ALTGX MegaWizard) - 1.

(2) You must connect the `pll_reconfig_done` signal from the ALTGX to the `pll_scandone` port from ALTPLL_RECONFIG.

(3) You need two ALTPLL_RECONFIG controllers if you have two separate ALTGX instances with transceiver PLL instantiated in each ALTGX instance.

For more information about connecting the ALTPLL_RECONFIG and ALTGX instances, refer to the *AN 609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices*.

# Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Cyclone IV Device Datasheet
Revised: *December 2016*
Part Number: *CYIV-53001-2.1*

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

**Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.211 | 1.211 | 2.177 | 2.340 | 2.433 | 2.388 | 2.508 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.307 | 1.203 | 1.203 | 2.19 | 2.387 | 2.540 | 2.430 | 2.545 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.437 | 0.402 | 0.402 | 0.747 | 0.820 | 0.880 | 0.834 | 0.873 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.693 | 0.665 | 0.665 | 1.200 | 1.379 | 1.532 | 1.393 | 1.441 | ns |

**Notes to Table 1–42:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.209 | 1.209 | 2.201 | 2.386 | 2.510 | 2.429 | 2.548 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.207 | 1.207 | 2.202 | 2.402 | 2.558 | 2.447 | 2.557 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.458 | 0.419 | 0.419 | 0.783 | 0.861 | 0.924 | 0.875 | 0.915 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.686 | 0.657 | 0.657 | 1.185 | 1.360 | 1.506 | 1.376 | 1.422 | ns |

**Notes to Table 1–43:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–47. Document Revision History**

| Date | Version | Changes |
|---|---|---|
| February 2010 | 1.1 | ■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.<br>■ Minor text edits. |
| November 2009 | 1.0 | Initial release. |