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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	81
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce15e22c7

- Cyclone IV GX devices offer up to eight high-speed transceivers that provide:
 - Data rates up to 3.125 Gbps
 - 8B/10B encoder/decoder
 - 8-bit or 10-bit physical media attachment (PMA) to physical coding sublayer (PCS) interface
 - Byte serializer/deserializer (SERDES)
 - Word aligner
 - Rate matching FIFO
 - TX bit slipper for Common Public Radio Interface (CPRI)
 - Electrical idle
 - Dynamic channel reconfiguration allowing you to change data rates and protocols on-the-fly
 - Static equalization and pre-emphasis for superior signal integrity
 - 150 mW per channel power consumption
 - Flexible clocking structure to support multiple protocols in a single transceiver block
- Cyclone IV GX devices offer dedicated hard IP for PCI Express (PIPE) (PCIe) Gen 1:
 - $\times 1$, $\times 2$, and $\times 4$ lane configurations
 - End-point and root-port configurations
 - Up to 256-byte payload
 - One virtual channel
 - 2 KB retry buffer
 - 4 KB receiver (Rx) buffer
- Cyclone IV GX devices offer a wide range of protocol support:
 - PCIe (PIPE) Gen 1 $\times 1$, $\times 2$, and $\times 4$ (2.5 Gbps)
 - Gigabit Ethernet (1.25 Gbps)
 - CPRI (up to 3.072 Gbps)
 - XAUI (3.125 Gbps)
 - Triple rate serial digital interface (SDI) (up to 2.97 Gbps)
 - Serial RapidIO (3.125 Gbps)
 - Basic mode (up to 3.125 Gbps)
 - V-by-One (up to 3.0 Gbps)
 - DisplayPort (2.7 Gbps)
 - Serial Advanced Technology Attachment (SATA) (up to 3.0 Gbps)
 - OBSAI (up to 3.072 Gbps)

 For more information, refer to the *External Memory Interfaces in Cyclone IV Devices* chapter.

Configuration

Cyclone IV devices use SRAM cells to store configuration data. Configuration data is downloaded to the Cyclone IV device each time the device powers up. Low-cost configuration options include the Altera EPCS family serial flash devices and commodity parallel flash configuration options. These options provide the flexibility for general-purpose applications and the ability to meet specific configuration and wake-up time requirements of the applications.

Table 1–9 lists which configuration schemes are supported by Cyclone IV devices.

Table 1–9. Configuration Schemes for Cyclone IV Device Family

Devices	Supported Configuration Scheme
Cyclone IV GX	AS, PS, JTAG, and FPP ⁽¹⁾
Cyclone IV E	AS, AP, PS, FPP, and JTAG


Note to Table 1–9:

(1) The FPP configuration scheme is only supported by the EP4CGX30F484 and EP4CGX50/75/110/150 devices.


IEEE 1149.6 (AC JTAG) is supported on all transceiver I/O pins. All other pins support IEEE 1149.1 (JTAG) for boundary scan testing.

 For more information, refer to the *JTAG Boundary-Scan Testing for Cyclone IV Devices* chapter.

For Cyclone IV GX devices to meet the PCIe 100 ms wake-up time requirement, you must use passive serial (PS) configuration mode for the EP4CGX15/22/30 devices and use fast passive parallel (FPP) configuration mode for the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

 For more information, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

The cyclical redundancy check (CRC) error detection feature during user mode is supported in all Cyclone IV GX devices. For Cyclone IV E devices, this feature is only supported for the devices with the core voltage of 1.2 V.

 For more information about CRC error detection, refer to the *SEU Mitigation in Cyclone IV Devices* chapter.

High-Speed Transceivers (Cyclone IV GX Devices Only)

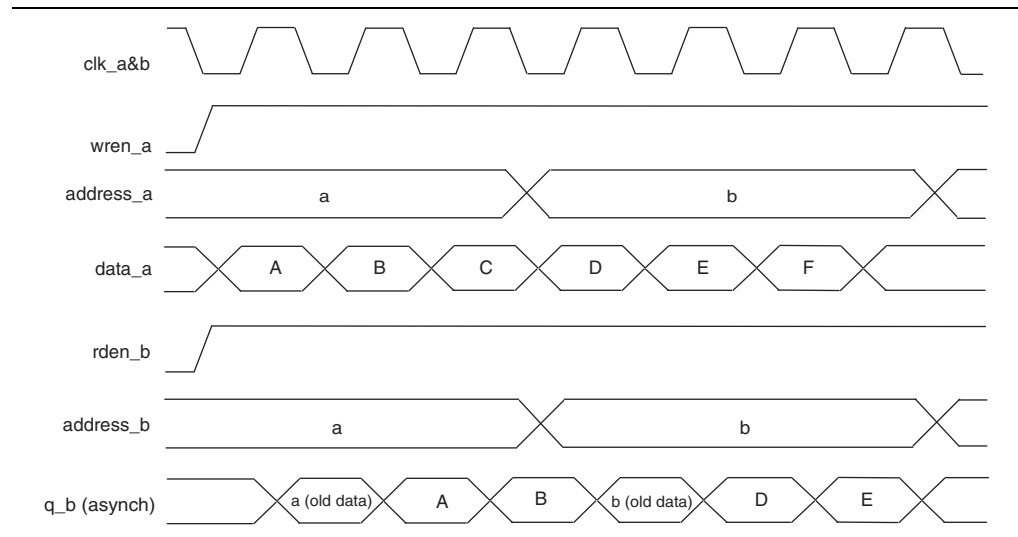
Cyclone IV GX devices contain up to eight full duplex high-speed transceivers that can operate independently. These blocks support multiple industry-standard communication protocols, as well as Basic mode, which you can use to implement your own proprietary protocols. Each transceiver channel has its own pre-emphasis and equalization circuitry, which you can set at compile time to optimize signal integrity and reduce bit error rates. Transceiver blocks also support dynamic reconfiguration, allowing you to change data rates and protocols on-the-fly.

In this mode, you also have two output choices: **Old Data** mode or **Don't Care** mode. In **Old Data** mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In **Don't Care** mode, the same operation results in a “Don't Care” or unknown value on the RAM outputs.

For more information about how to implement the desired behavior, refer to the *RAM Megafunction User Guide*.

Figure 3-16 shows a sample functional waveform of mixed port read-during-write behavior for **Old Data** mode. In **Don't Care** mode, the old data is replaced with “Don't Care”.

Figure 3-16. Mixed Port Read-During-Write: Old Data Mode



For mixed-port read-during-write operation with dual clocks, the relationship between the clocks determines the output behavior of the memory. If you use the same clock for the two clocks, the output is the old data from the address location. However, if you use different clocks, the output is unknown during the mixed-port read-during-write operation. This unknown value may be the old or new data at the address location, depending on whether the read happens before or after the write.

Conflict Resolution

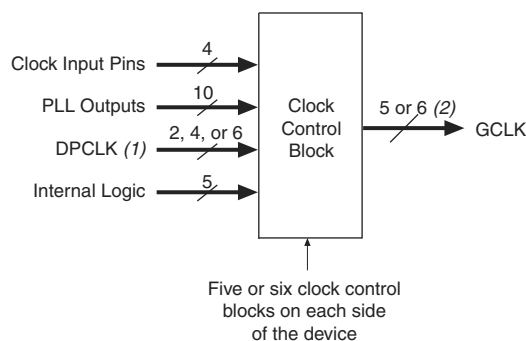
When you are using M9K memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Because there is no conflict resolution circuitry built into M9K memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict-resolution logic external to the M9K memory block.

From the clock sources listed above, only two clock input pins, two out of four PLL clock outputs (two clock outputs from either adjacent PLLs), one DPCLK pin, and one source from internal logic can drive into any given clock control block, as shown in Figure 5-1 on page 5-11.

Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs are dynamically selected to feed a GCLK. The clock control block supports static selection of the signal from internal logic.

Figure 5-5 shows a simplified version of the clock control blocks on each side of the Cyclone IV GX device periphery.

Figure 5-5. Clock Control Blocks on Each Side of Cyclone IV GX Device



Notes to Figure 5-5:

- (1) The EP4CGX15 device has two DPCLK pins; the EP4CGX22 and EP4CGX30 devices have four DPCLK pins; the EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have six DPCLK pins.
- (2) Each clock control block in the EP4CGX15, EP4CGX22, and EP4CGX30 devices can drive five GCLK networks. Each clock control block in the EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices can drive six GCLK networks.

The inputs to the five clock control blocks on each side of the Cyclone IV E device must be chosen from among the following clock sources:

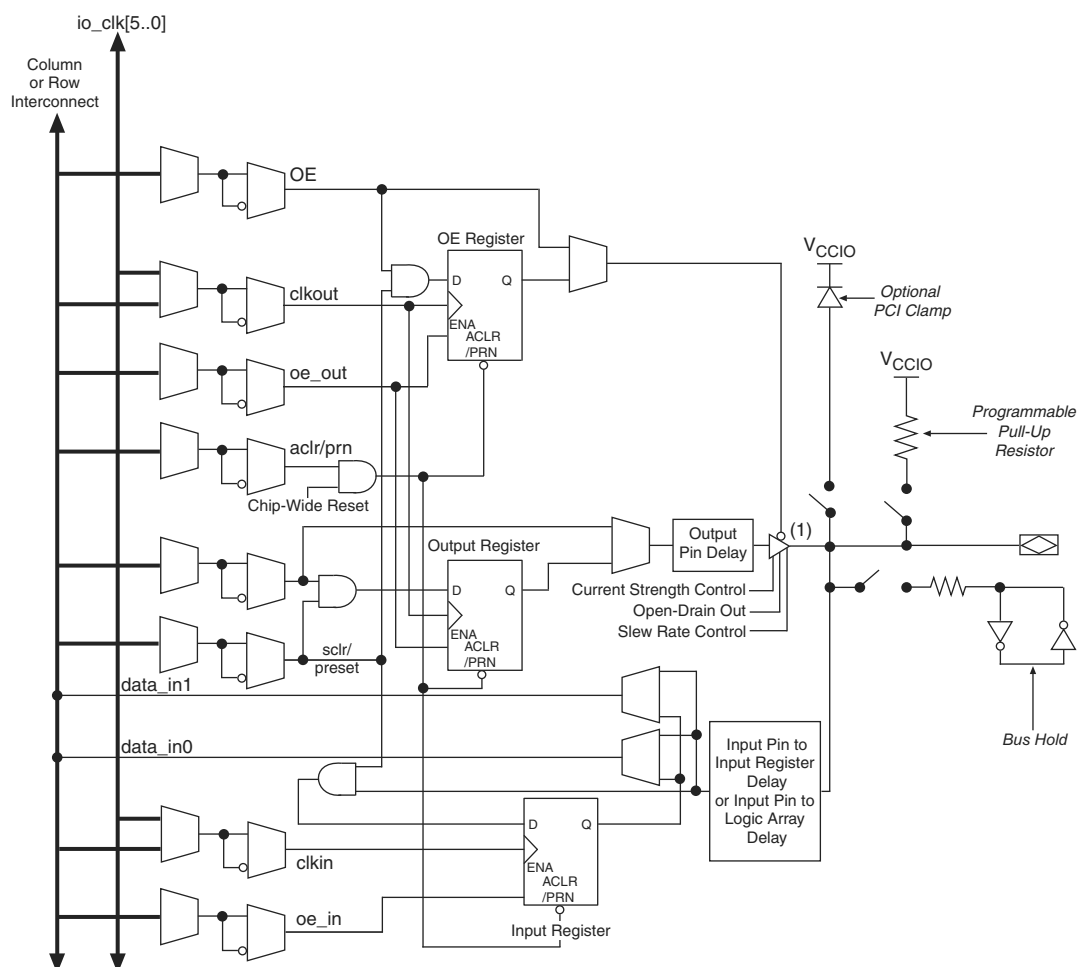
- Three or four clock input pins, depending on the specific device
- Five PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins from both the top and bottom
- Five signals from internal logic

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control block, as shown in Figure 5-1 on page 5-11.

Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs are dynamically selected to feed a GCLK. The clock control block supports static selection of the signal from internal logic.

Figure 6–1 shows the Cyclone IV devices IOE structure for single data rate (SDR) operation.

Figure 6–1. Cyclone IV IOEs in a Bidirectional I/O Configuration for SDR Mode



Note to Figure 6–1:

(1) Tri-state control is not available for outputs configured with true differential I/O standards.

I/O Element Features

The Cyclone IV IOE offers a range of programmable features for an I/O pin. These features increase the flexibility of I/O utilization and provide a way to reduce the usage of external discrete components, such as pull-up resistors and diodes.

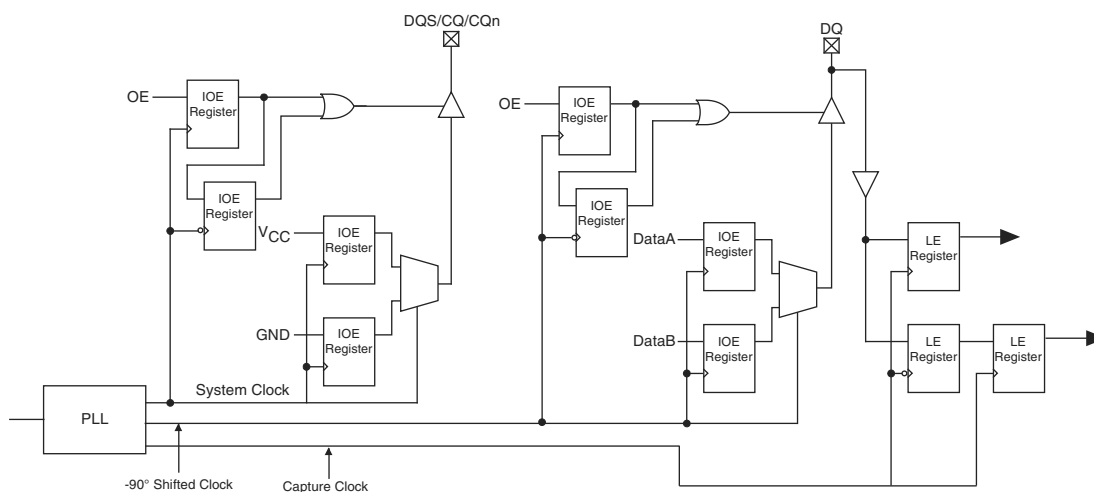
Programmable Current Strength

The output buffer for each Cyclone IV I/O pin has a programmable current strength control for certain I/O standards.

The LVTTTL, LVCMOS, SSTL-2 Class I and II, SSTL-18 Class I and II, HSTL-18 Class I and II, HSTL-15 Class I and II, and HSTL-12 Class I and II I/O standards have several levels of current strength that you can control.

Figure 7-1 shows the block diagram of a typical external memory interface data path in Cyclone IV devices.

Figure 7-1. Cyclone IV Devices External Memory Data Path ⁽¹⁾



Note to Figure 7-1:

(1) All clocks shown here are global clocks.

For more information about implementing complete external memory interfaces, refer to the *External Memory Interface Handbook*.

Cyclone IV Devices Memory Interfaces Pin Support

Cyclone IV devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory. Some memory interfaces use the data mask (DM) or byte write select (BWS#) pins to enable data masking. This section describes how Cyclone IV devices support all these different pins.

For more information about pin utilization, refer to *Volume 2: Device, Pin, and Board Layout Guidelines* of the *External Memory Interface Handbook*.

Data and Data Clock/Strobe Pins

Cyclone IV data pins for external memory interfaces are called D for write data, Q for read data, or DQ for shared read and write data pins. The read-data strobes or read clocks are called DQS pins. Cyclone IV devices support both bidirectional data strobes and unidirectional read clocks. Depending on the external memory standard, the DQ and DQS are bidirectional signals (in DDR2 and DDR SDRAM) or unidirectional signals (in QDR II SRAM). Connect the bidirectional DQ data signals to the same Cyclone IV devices DQ pins. For unidirectional D or Q signals, connect the read-data signals to a group of DQ pins and the write-data signals to a different group of DQ pins.

In QDR II SRAM, the Q read-data group must be placed at a different V_{REF} bank location from the D write-data group, command, or address pins.

During device configuration, Cyclone IV E devices read configuration data using the parallel interface and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where an external host controls the interface.

AP Configuration Supported Flash Memories

The AP configuration controller in Cyclone IV E devices is designed to interface with two industry-standard flash families—the Micron P30 Parallel NOR flash family and the Micron P33 Parallel NOR flash family. Unlike serial configuration devices, both of the flash families supported in AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash after entering user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Micron P30 flash family and the P33 flash family support a continuous synchronous burst read mode at 40 MHz DCLK frequency for reading data from the flash. Additionally, the Micron P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.



Cyclone IV E devices use a 40-MHz oscillator for the AP configuration scheme. The oscillator is the same oscillator used in the Cyclone IV E AS configuration scheme.

Table 8–10 lists the supported families of the commodity parallel flash for the AP configuration scheme.

Table 8–10. Supported Commodity Flash for AP Configuration Scheme for Cyclone IV E Devices ⁽¹⁾

Flash Memory Density	Micron P30 Flash Family ⁽²⁾	Micron P33 Flash Family ⁽³⁾
64 Mbit	✓	✓
128 Mbit	✓	✓
256 Mbit	✓	✓

Notes to Table 8–10:

- (1) The AP configuration scheme only supports flash memory speed grades of 40 MHz and above.
- (2) 3.3-, 3.0-, 2.5-, and 1.8-V I/O options are supported for the Micron P30 flash family.
- (3) 3.3-, 3.0- and 2.5-V I/O options are supported for the Micron P33 flash family.

Configuring Cyclone IV E devices from the Micron P30 and P33 family 512-Mbit flash memory is possible, but you must properly drive the extra address and FLASH_nCE pins as required by these flash memories.



To check for supported speed grades and package options, refer to the respective flash datasheets.

The AP configuration scheme in Cyclone IV E devices supports flash speed grades of 40 MHz and above. However, AP configuration for all these speed grades must be capped at 40 MHz. The advantage of faster speed grades is realized when your design in the Cyclone IV E devices accesses flash memory in user mode.

Table 8–21 lists the optional configuration pins. If you do not enable these optional configuration pins in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 8–21. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	Optional user-supplied clock input synchronizes the initialization of one or more devices. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software. In AS configuration for Cyclone IV GX devices, you can use this pin as an external clock source to generate the <code>DCLK</code> by changing the clock source option in the Quartus II software in the Configuration tab of the Device and Pin Options dialog box.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Status pin is used to indicate when the device has initialized and is in user-mode. When <code>nCONFIG</code> is low, the <code>INIT_DONE</code> pin is tri-stated and pulled high due to an external 10-k Ω pull-up resistor during the beginning of configuration. After the option bit to enable <code>INIT_DONE</code> is programmed into the device (during the first frame of configuration data), the <code>INIT_DONE</code> pin goes low. When initialization is complete, the <code>INIT_DONE</code> pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software. The functionality of this pin changes if the Enable OCT_DONE option is enabled in the Quartus II software. This option controls whether the <code>INIT_DONE</code> signal is gated by the <code>OCT_DONE</code> signal, which indicates the power-up on-chip termination (OCT) calibration is complete. If this option is turned off, the <code>INIT_DONE</code> signal is not gated by the <code>OCT_DONE</code> signal.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. You can enable this pin by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.



The divisor value divides the frequency of the configuration oscillator output clock. This output clock is used as the clock source for the error detection process.

8. Click **OK**.

Figure 9–2. Enabling the Error Detection CRC Feature in the Quartus II Software

Accessing Error Detection Block Through User Logic

The error detection circuit stores the computed 32-bit CRC signature in a 32-bit register, which is read out by user logic from the core. The `cycloneiv_crcblock` primitive is a WYSIWYG component used to establish the interface from the user logic to the error detection circuit. The `cycloneiv_crcblock` primitive atom contains the input and output ports that must be included in the atom. To access the logic array, the `cycloneiv_crcblock` WYSIWYG atom must be inserted into your design.

This section provides a complete overview of all features relating to the Cyclone[®] IV device transceivers. This section includes the following chapters:

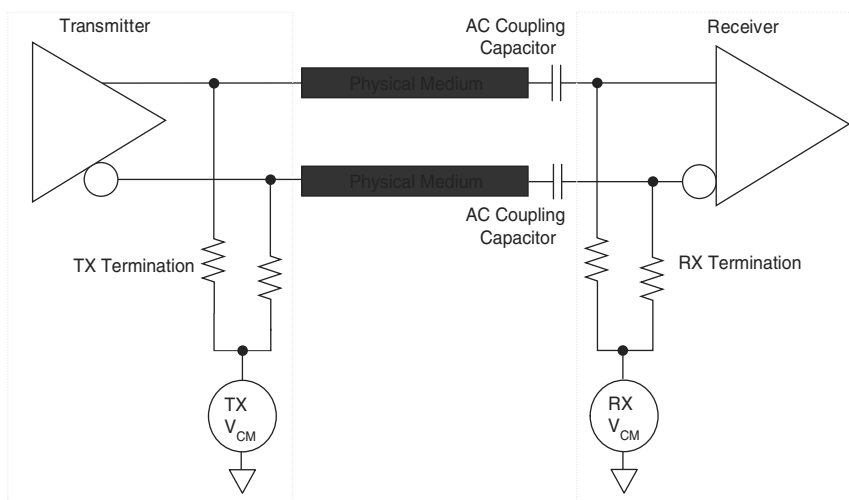
- Chapter 1, Cyclone IV Transceivers Architecture
- Chapter 2, Cyclone IV Reset Control and Power Down
- Chapter 3, Cyclone IV Dynamic Reconfiguration

Revision History

Refer to the chapter for its own specific revision history. For information about when the chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

The high-speed serial link can be AC- or DC-coupled, depending on the serial protocol implementation. In an AC-coupled link, the AC-coupling capacitor blocks the transmitter DC common mode voltage as shown in Figure 1-12. Receiver OCT and on-chip biasing circuitry automatically restores the common mode voltage. The biasing circuitry is also enabled by enabling OCT. If you disable the OCT, then you must externally terminate and bias the receiver. AC-coupled links are required for PCIe, GbE, Serial RapidIO, SDI, XAUI, SATA, V-by-One and Display Port protocols.

Figure 1-12. AC-Coupled Link with OCT



When the byte serializer is enabled, the low-speed clock frequency is halved before feeding into the read clock of TX phase compensation FIFO. The low-speed clock is available in the FPGA fabric as `tx_clkout` port, which can be used in the FPGA fabric to send transmitter data and control signals.

Figure 1-33. Transmitter Only Datapath Clocking in Non-Bonded Channel Configuration

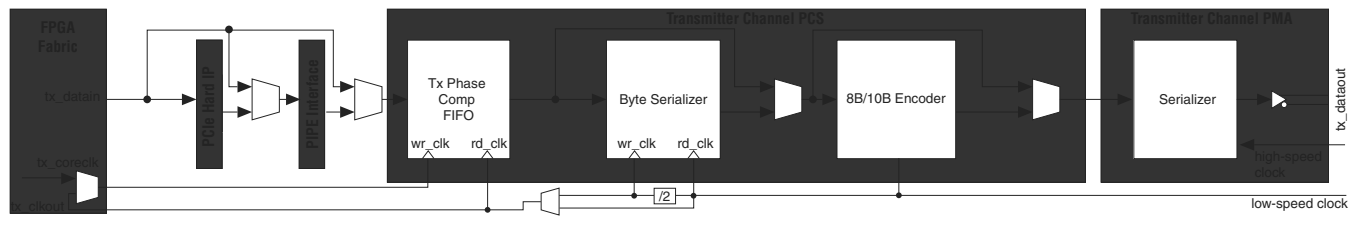
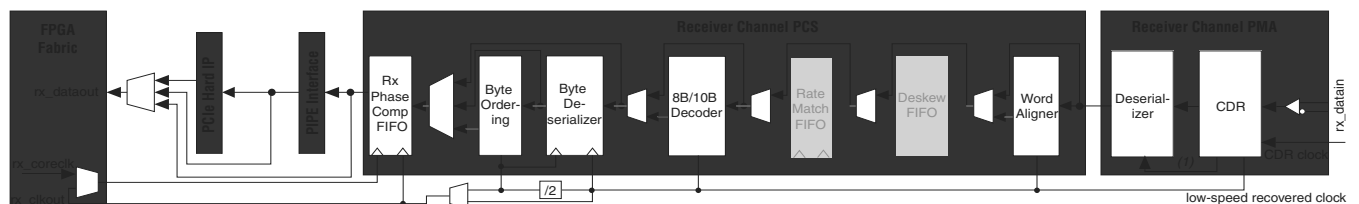


Figure 1-34 shows the datapath clocking in receiver only operation. In this mode, the receiver PCS supports configuration without the rate match FIFO. The CDR unit in the channel recovers the clock from the received serial data and generates the high-speed recovered clock for the deserializer, and low-speed recovered clock for forwarding to the receiver PCS. The low-speed recovered clock feeds to the following blocks in the receiver PCS:

- word aligner
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the low-speed recovered clock frequency is halved before feeding into the write clock of the RX phase compensation FIFO. The low-speed recovered clock is available in the FPGA fabric as `rx_clkout` port, which can be used in the FPGA fabric to capture receiver data and status signals.

Figure 1-34. Receiver Only Datapath Clocking without Rate Match FIFO in Non-Bonded Channel Configuration



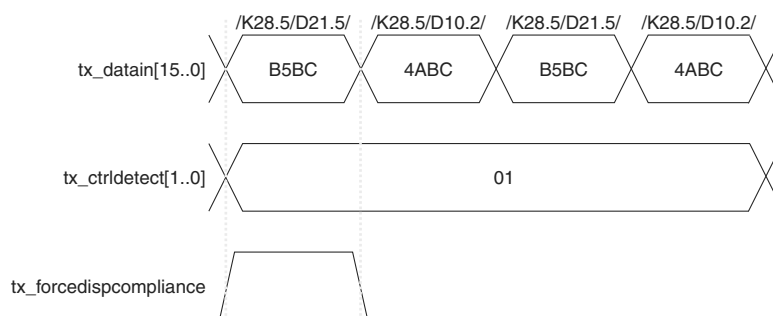
Note to Figure 1-34:

- (1) High-speed recovered clock.

When the transceiver is configured for transmitter and receiver operation in non-bonded channel configuration, the receiver PCS supports configuration with and without the rate match FIFO. The difference is only at the receiver datapath clocking. The transmitter datapath clocking is identical to transmitter only operation mode as shown in Figure 1-33.

The compliance pattern is a repeating sequence of the four code groups: /K28.5/; /D21.5/; /K28.5/; /D10.2/. Figure 1-53 shows the compliance pattern transmission where the tx_forcedispcompliance port must be asserted in the same parallel clock cycle as /K28.5/D21.5/ of the compliance pattern on tx_datain[15..0] port.

Figure 1-53. Compliance Pattern Transmission Support in PCI Express (PIPE) Mode



Reset Requirement

Cyclone IV GX devices meets the PCIe reset time requirement from device power up to the link active state with the configuration schemes listed in Table 1-17.

Table 1-18. Electrical Idle Inference Conditions

Device	Configuration Scheme	Configuration Time (ms)
EP4CGX15	Passive serial (PS)	51
EP4CGX22	PS	92
EP4CGX30 ⁽¹⁾	PS	92
EP4CGX50	Fast passive parallel (FPP)	41
EP4CGX75	FPP	41
EP4CGX110	FPP	70
EP4CGX150	FPP	70

Note to Table 1-18:

(1) EP4CGX30 device in F484 package fulfills the PCIe reset time requirement using FPP configuration scheme with configuration time of 41 ms.

GIGE Mode

GIGE mode provides the transceiver channel datapath configuration for GbE (specifically the 1000 Base-X physical layer device (PHY) standard) protocol implementation. The Cyclone IV GX transceiver provides the PMA and the following PCS functions as defined in the IEEE 802.3 specification for 1000 Base-X PHY:

- 8B/10B encoding and decoding
- synchronization

If you enabled the auto-negotiation state machine in the FPGA core with the rate match FIFO, refer to “Clock Frequency Compensation” on page 1-63.

Table 1–29. Multipurpose PLL, General Purpose PLL and Miscellaneous Ports in ALTGX Megafunction for Cyclone IV GX (Part 2 of 2)

Block	Port Name	Input/Output	Clock Domain	Description
Reset & Power Down	gxb_powerdown	Input	Asynchronous signal	Transceiver block power down. <ul style="list-style-type: none"> When asserted, all digital and analog circuitry in the PCS, HSSI, CDR, and PCIe modules are powered down. Asserting the <code>gxb_powerdown</code> signal does not power down the <code>refclk</code> buffers.
	tx_digitalreset	Input	Asynchronous signal. The minimum pulse width is two parallel clock cycles.	Transmitter PCS reset. <ul style="list-style-type: none"> When asserted, the transmitter PCS blocks are reset.
	rx_analogreset	Input	Asynchronous signal. The minimum pulse width is two parallel clock cycles.	Receiver PMA reset. <ul style="list-style-type: none"> When asserted, analog circuitry in the receiver PMA block is reset.
	rx_digitalreset	Input	Asynchronous signal. The minimum pulse width is two parallel clock cycles.	Receiver PCS reset. <ul style="list-style-type: none"> When asserted, the receiver PCS blocks are reset.
Reconfiguration	reconfig_clk	Input	Clock signal	Dynamic reconfiguration clock. <ul style="list-style-type: none"> Also used for offset cancellation except in PIPE mode. For the supported frequency range for this clock, refer to the <i>Cyclone IV Device Data Sheet</i> chapter.
	reconfig_togxb	Input	Asynchronous signal	From the dynamic reconfiguration controller.
	reconfig_fromgxb	Output	Asynchronous signal	To the dynamic reconfiguration controller.
Calibration Block	cal_blk_clk	Input	Clock signal	Clock for the transceiver calibration block.
	cal_blk_powerdown	Input	Asynchronous signal	Calibration block power down control.
Test Mode	rx_bistdone	Output	Asynchronous signal	BIST or PRBS test completion indicator. <ul style="list-style-type: none"> A high level during BIST test mode indicates the verifier either receives complete pattern cycle or detects an error and stays asserted until being reset using the <code>rx_digitalreset</code> port. A high level during PRBS test mode indicates the verifier receives complete pattern cycle and stays asserted until being reset using the <code>rx_digitalreset</code> port.
	rx_bisterr	Output	Asynchronous signal	BIST or PRBS verifier error indicator <ul style="list-style-type: none"> In BIST test mode, the signal stays asserted upon detecting an error until being reset using the <code>rx_digitalreset</code> port. In PRBS test mode, the signal asserts for a minimum of 3 <code>rx_clkout</code> clock cycles upon detecting an error and deasserts if the following PRBS sequence contains no error.

3. Cyclone IV Dynamic Reconfiguration

CYIV-52003-2.1

Cyclone® IV GX transceivers allow you to dynamically reconfigure different portions of the transceivers without powering down any part of the device. This chapter describes and provides examples about the different modes available for dynamic reconfiguration.

You can use the ALTGX_RECONFIG and ALTPLL_RECONFIG controller instance to reconfigure the physical medium attachment (PMA) controls, physical coding sublayer (PCS), multipurpose phase locked loops (PLLs), and general purpose PLLs.

This chapter contains the following sections:

- “Glossary of Terms” on page 3–1
- “Dynamic Reconfiguration Controller Architecture” on page 3–2
- “Dynamic Reconfiguration Modes” on page 3–12
- “Error Indication During Dynamic Reconfiguration” on page 3–36
- “Functional Simulation of the Dynamic Reconfiguration Process” on page 3–37

Glossary of Terms

Table 3–1 lists the terms used in this chapter:

Table 3–1. Glossary of Terms Used in this Chapter (Part 1 of 2)

Term	Description
ALTGX_RECONFIG Instance	Dynamic reconfiguration controller instance generated by the ALTGX_RECONFIG MegaWizard™ Plug-In Manager.
ALTGX Instance	Transceiver instance generated by the ALTGX MegaWizard Plug-In Manager.
ALTPLL_RECONFIG Instance	Dynamic PLL reconfiguration controller instance generated by the ALTPLL_RECONFIG Megawizard Plug-In Manager
Logical Channel Addressing	Used whenever the concept of logical channel addressing is explained. This term does not refer to the <code>logical_channel_address</code> port available in the ALTGX_RECONFIG MegaWizard Plug-In Manager.

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 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration

