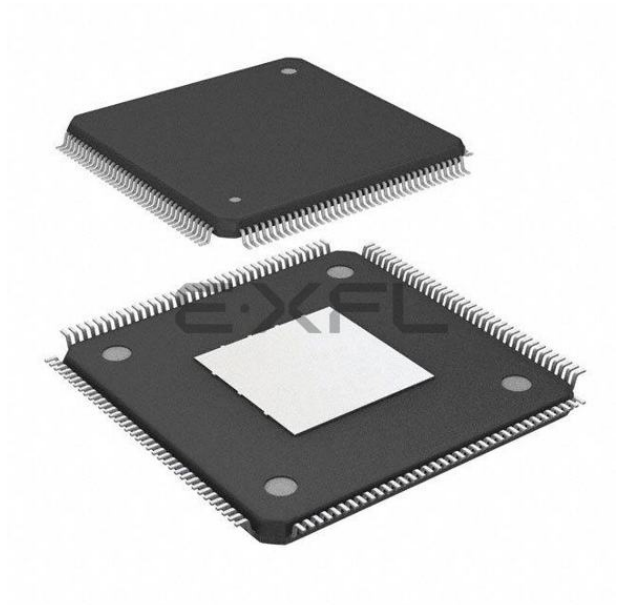

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	81
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce15e22c7n

Package Matrix

Table 1–3 lists Cyclone IV E device package offerings.

Table 1–3. Package Offerings for the Cyclone IV E Device Family *(1), (2)*

Package	E144		M164		M256		U256		F256		F324		U484		F484		F780	
Size (mm)	22 × 22		8 × 8		9 x 9		14 × 14		17 × 17		19 x 19		19 × 19		23 × 23		29 × 29	
Pitch (mm)	0.5		0.5		0.5		0.8		1.0		1.0		0.8		1.0		1.0	
Device	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*	User I/O	LVDS *(3)*
EP4CE6	91	21	—	—	—	—	179	66	179	66	—	—	—	—	—	—	—	—
EP4CE10	91	21	—	—	—	—	179	66	179	66	—	—	—	—	—	—	—	—
EP4CE15	81	18	89	21	165	53	165	53	165	53	—	—	—	—	343	137	—	—
EP4CE22	79	17	—	—	—	—	153	52	153	52	—	—	—	—	—	—	—	—
EP4CE30	—	—	—	—	—	—	—	—	—	—	193	68	—	—	328	124	532	224
EP4CE40	—	—	—	—	—	—	—	—	—	—	193	68	328	124	328	124	532	224
EP4CE55	—	—	—	—	—	—	—	—	—	—	—	—	324	132	324	132	374	160
EP4CE75	—	—	—	—	—	—	—	—	—	—	—	—	292	110	292	110	426	178
EP4CE115	—	—	—	—	—	—	—	—	—	—	—	—	—	—	280	103	528	230

Notes to Table 1–3:

(1) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane of your PCB. Use this exposed pad for electrical connectivity and not for thermal purposes.

(2) Use the Pin Migration View window in Pin Planner of the Quartus II software to verify the pin migration compatibility when you perform device migration. For more information, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

(3) This includes both dedicated and emulated LVDS pairs. For more information, refer to the *I/O Features in Cyclone IV Devices* chapter.

Figure 3–3 and Figure 3–4 show the address clock enable waveform during read and write cycles, respectively.

Figure 3–3. Cyclone IV Devices Address Clock Enable During Read Cycle Waveform

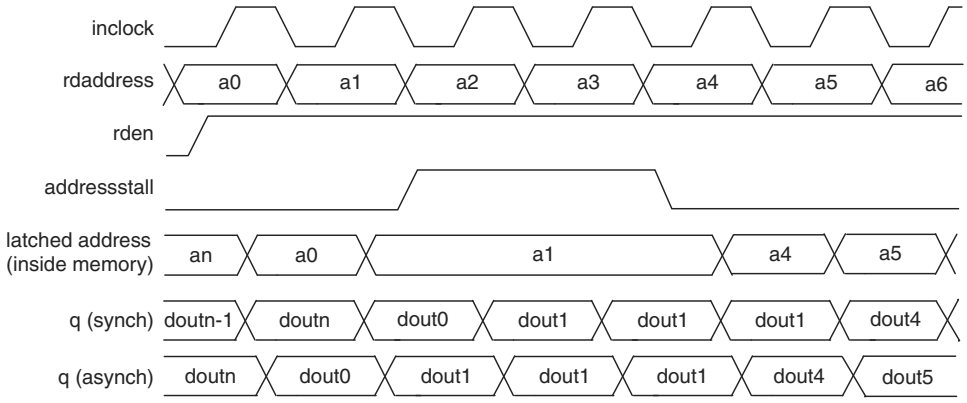
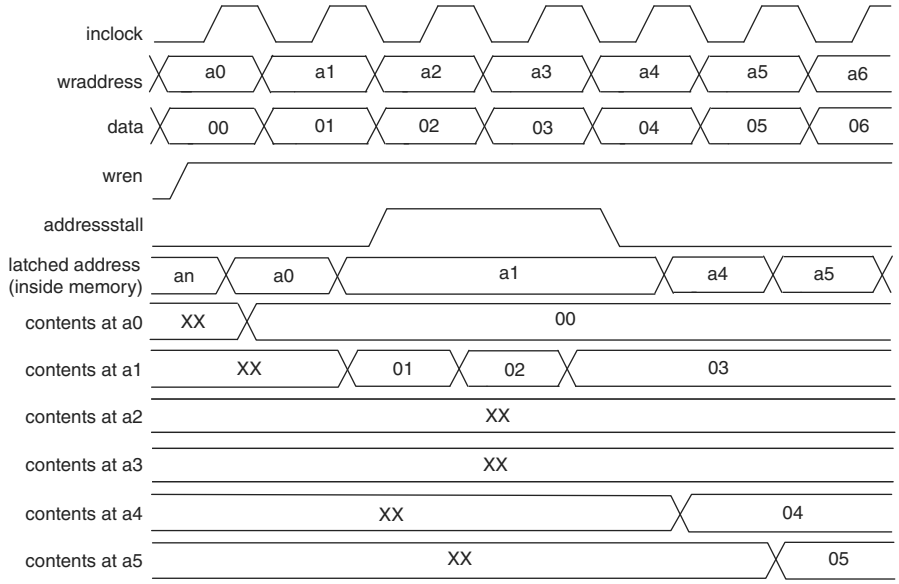


Figure 3–4. Cyclone IV Devices Address Clock Enable During Write Cycle Waveform



Mixed-Width Support

M9K memory blocks support mixed data widths. When using simple dual-port, true dual-port, or FIFO modes, mixed width support allows you to read and write different data widths to an M9K memory block. For more information about the different widths supported per memory mode, refer to "Memory Modes" on page 3–7.

5. Clock Networks and PLLs in Cyclone IV Devices

CYIV-51005-2.4

This chapter describes the hierarchical clock networks and phase-locked loops (PLLs) with advanced features in the Cyclone® IV device family. It includes details about the ability to reconfigure the PLL counter clock frequency and phase shift in real time, allowing you to sweep PLL output frequencies and dynamically adjust the output clock phase shift.

☞ The Quartus® II software enables the PLLs and their features without external devices.

This chapter contains the following sections:

Clock Networks

The Cyclone IV GX device provides up to 12 dedicated clock pins (`CLK[15..4]`) that can drive the global clocks (GCLKs). Cyclone IV GX devices support four dedicated clock pins on each side of the device except the left side. These clock pins can drive up to 30 GCLKs.

The Cyclone IV E device provides up to 15 dedicated clock pins (`CLK[15..1]`) that can drive up to 20 GCLKs. Cyclone IV E devices support three dedicated clock pins on the left side and four dedicated clock pins on the top, right, and bottom sides of the device except EP4CE6 and EP4CE10 devices. EP4CE6 and EP4CE10 devices only support three dedicated clock pins on the left side and four dedicated clock pins on the right side of the device.

Table 5–6. Cyclone IV E PLL Features (Part 2 of 2)

Hardware Features	Availability
Loss of lock detection	✓

Notes to Table 5–6:

(1) C counters range from 1 through 512 if the output clock uses a 50% duty cycle. For any output clocks using a non-50% duty cycle, the post-scale counters range from 1 through 256.

(2) Only applicable if the input clock jitter is in the input jitter tolerance specifications.

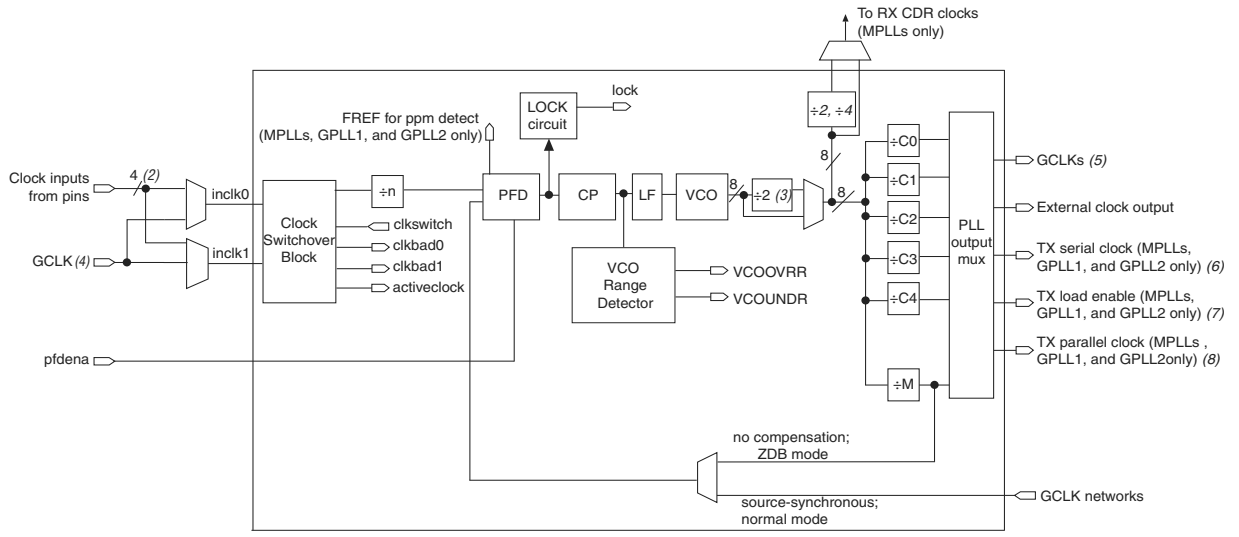
(3) The smallest phase shift is determined by the VCO period divided by eight. For degree increments, Cyclone IV E devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Cyclone IV PLL Hardware Overview

This section gives a hardware overview of the Cyclone IV PLL.

Figure 5–9 shows a simplified block diagram of the major components of the PLL of Cyclone IV GX devices.

Figure 5–9. Cyclone IV GX PLL Block Diagram (1)



Notes to Figure 5–9:

(1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.

(2) There are additional 4 pairs of dedicated differential clock inputs in EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices that can only drive general purpose PLLs and multipurpose PLLs on the left side of the device. `CLK[19..16]` can access `PLL_2`, `PLL_6`, `PLL_7`, and `PLL_8` while `CLK[23..20]` can access `PLL_1`, `PLL_5`, `PLL_6`, and `PLL_7`. For the location of these clock input pins, refer to Figure 5–3 on page 5–13.

(3) This is the VCO post-scale counter K.

(4) This input port is fed by a pin-driven dedicated GCLK, or through a clock control block if the clock control block is fed by an output from another PLL or a pin-driven dedicated GCLK. An internally generated global signal cannot drive the PLL.

(5) For the general purpose PLL and multipurpose PLL counter outputs connectivity to the GCLKs, refer to Table 5–1 on page 5–2 and Table 5–2 on page 5–4.

(6) Only the CI output counter can drive the TX serial clock.

(7) Only the C2 output counter can drive the TX load enable.

(8) Only the C3 output counter can drive the TX parallel clock.

Clock Feedback Modes

Cyclone IV PLLs support up to five different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes, refer to Table 5–5 on page 5–18 for Cyclone IV GX PLLs and Table 5–6 on page 5–19 for Cyclone IV E PLLs.

☞ Input and output delays are fully compensated by the PLL only if you are using the dedicated clock input pins associated with a given PLL as the clock sources.

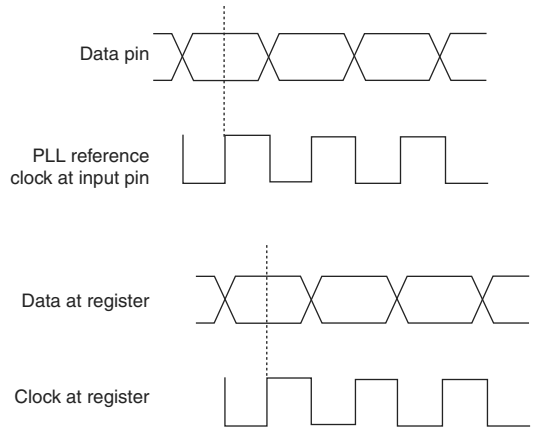
When driving the PLL using the GCLK network, the input and output delays may not be fully compensated in the Quartus II software.

Source-Synchronous Mode

If the data and clock arrive at the same time at the input pins, the phase relationship between the data and clock remains the same at the data and clock ports of any I/O element input register.

Figure 5–12 shows an example waveform of the data and clock in this mode. Use this mode for source-synchronous data transfers. Data and clock signals at the I/O element experience similar buffer delays as long as the same I/O standard is used.

Figure 5–12. Phase Relationship Between Data and Clock in Source-Synchronous Mode



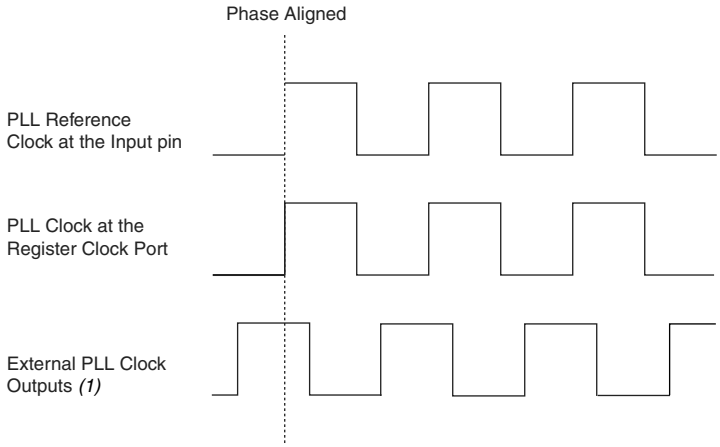
Source-synchronous mode compensates for delay of the clock network used, including any difference in the delay between the following two paths:

- Data pin to I/O element register input
- Clock input pin to the PLL phase frequency detector (PFD) input

☞ Set the input pin to the register delay chain in the I/O element to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL. Also, all data pins must use the **PLL COMPENSATED logic** option in the Quartus II software.

Figure 5–14 shows a waveform example of the phase relationship of the PLL clocks in this mode.

Figure 5–14. Phase Relationship Between PLL Clocks in Normal Mode



Note to Figure 5–14:

(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In zero delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Figure 5–15 shows an example waveform of the phase relationship of the PLL clocks in ZDB mode.

Figure 5–15. Phase Relationship Between PLL Clocks in ZDB Mode

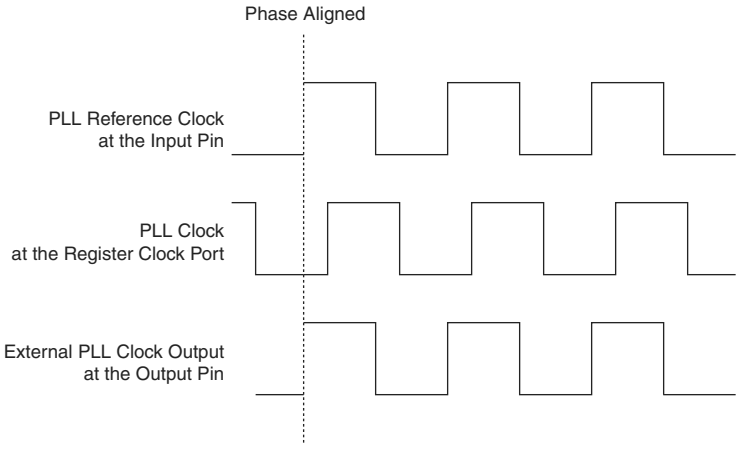
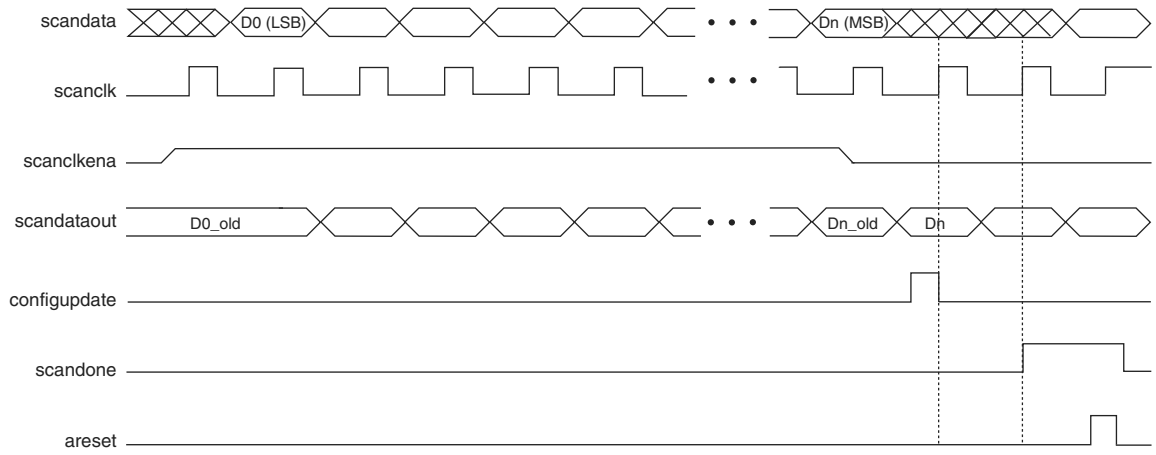


Figure 5–23 shows a functional simulation of the PLL reconfiguration feature.

Figure 5–23. PLL Reconfiguration Scan Chain



When reconfiguring the counter clock frequency, the corresponding counter phase shift settings cannot be reconfigured using the same interface. You can reconfigure phase shifts in real time using the dynamic phase shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase shift setting (for example, 90°) on the clock output, you must reconfigure the phase shift after reconfiguring the counter clock frequency.

Post-Scale Counters (C0 to C4)

You can configure multiply or divide values and duty cycle of post-scale counters in real time. Each counter has an 8-bit high time setting and an 8-bit low time setting. The duty cycle is the ratio of output high or low time to the total cycle time, that is the sum of the two. Additionally, these counters have two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.

When the `rbypass` bit is set to 1, it bypasses the counter, resulting in a divide by one. When this bit is set to 0, the PLL computes the effective division of the VCO output frequency based on the high and low time counters. For example, if the post-scale divide factor is 10, the high and low count values are set to 5 and 5, to achieve a 50–50% duty cycle. The PLL implements this duty cycle by transitioning the output clock from high-to-low on the rising edge of the VCO output clock. However, a 4 and 6 setting for the high and low count values, respectively, would produce an output clock with a 40–60% duty cycle.

The `rselodd` bit indicates an odd divide factor for the VCO output frequency with a 50% duty cycle. For example, if the post-scale divide factor is three, the high and low time count values are 2 and 1, respectively, to achieve this division. This implies a 67%–33% duty cycle. If you need a 50%–50% duty cycle, you must set the `rselodd` control bit to 1 to achieve this duty cycle despite an odd division factor. The PLL implements this duty cycle by transitioning the output clock from high-to-low on a falling edge of the VCO output clock. When you set `rselodd` = 1, subtract 0.5 cycles from the high time and add 0.5 cycles to the low time.

For example:

- High time count = 2 cycles

6. I/O Features in Cyclone IV Devices

CYIV-51006-2.7

This chapter describes the I/O and high speed I/O capabilities and features offered in Cyclone® IV devices.

The I/O capabilities of Cyclone IV devices are driven by the diversification of I/O standards in many low-cost applications, and the significant increase in required I/O performance. Altera's objective is to create a device that accommodates your key board design needs with ease and flexibility.

The I/O flexibility of Cyclone IV devices is increased from the previous generation low-cost FPGAs by allowing all I/O standards to be selected on all I/O banks. Improvements to on-chip termination (OCT) support and the addition of true differential buffers have eliminated the need for external resistors in many applications, such as display system interfaces.

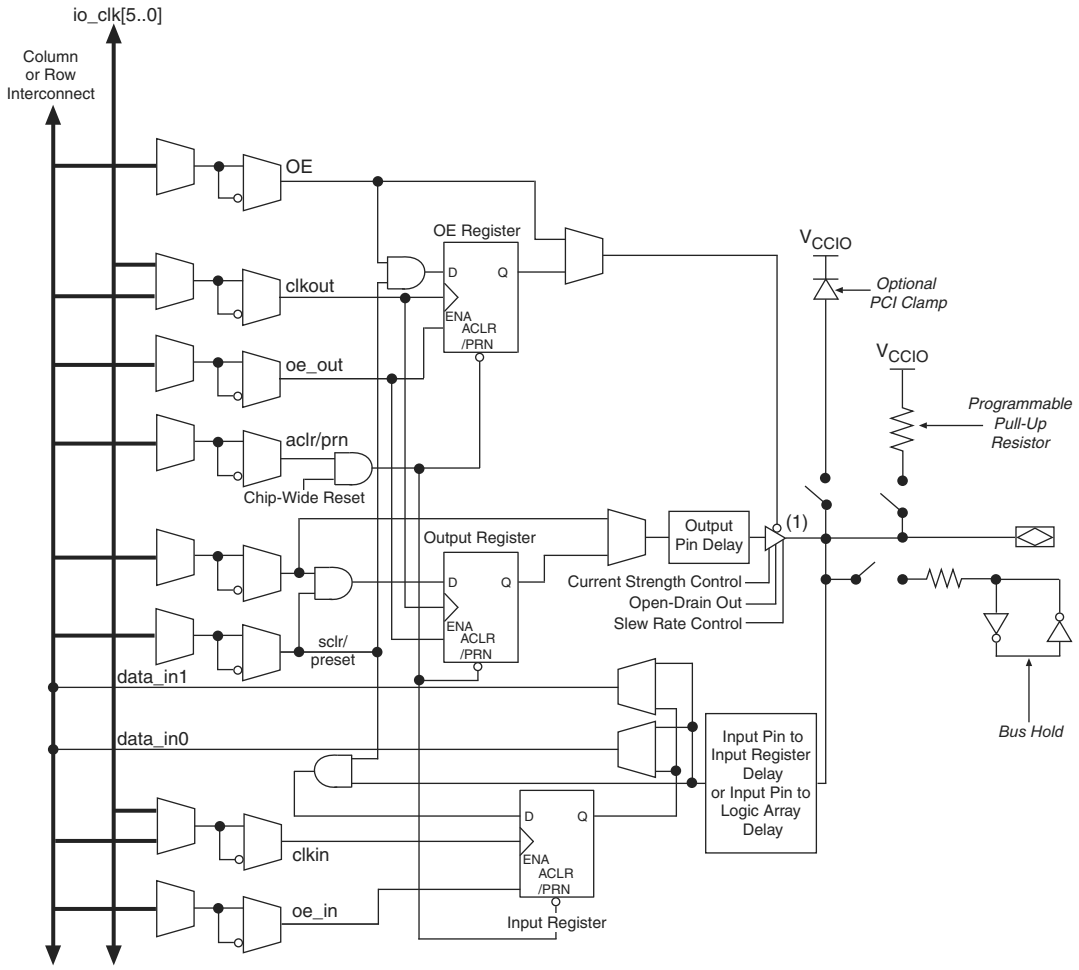
High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. The Cyclone IV devices support LVDS, BLVDS, RSDS, mini-LVDS, and PPDS. The transceiver reference clocks and the existing general-purpose I/O (GPIO) clock input features also support the LVDS I/O standards.

The Quartus® II software completes the solution with powerful pin planning features that allow you to plan and optimize I/O system designs even before the design files are available.

This chapter includes the following sections:

Figure 6–1 shows the Cyclone IV devices IOE structure for single data rate (SDR) operation.

Figure 6–1. Cyclone IV IOEs in a Bidirectional I/O Configuration for SDR Mode



Note to Figure 6–1:

(1) Tri-state control is not available for outputs configured with true differential I/O standards.

I/O Element Features

The Cyclone IV IOE offers a range of programmable features for an I/O pin. These features increase the flexibility of I/O utilization and provide a way to reduce the usage of external discrete components, such as pull-up resistors and diodes.

Programmable Current Strength

The output buffer for each Cyclone IV I/O pin has a programmable current strength control for certain I/O standards.

The LVTTL, LVCMOS, SSTL-2 Class I and II, SSTL-18 Class I and II, HSTL-18 Class I and II, HSTL-15 Class I and II, and HSTL-12 Class I and II I/O standards have several levels of current strength that you can control.

Table 6–2. Cyclone IV Device I/O Features Support (Part 2 of 2)

I/O Standard	IOH/IOL Current Strength Setting (mA) (1), (9)		R_S OCT with Calibration Setting, Ohm (Ω)		R_S OCT Without Calibration Setting, Ohm (Ω)		Cyclone IV E I/O Banks Support	Cyclone IV GX I/O Banks Support	Slew Rate Option (6)	PCI-clamp Diode Support
	Column I/O	Row I/O	Column I/O	Row I/O (8)	Column I/O	Row I/O (8)				
BLVDS	8,12,16	8,12,16	—	—	—	—	1,2,3,4, 5,6,7,8	3,4,5,6, 7,8	0,1,**2**	—
LVDS (3)	—	—	—	—	—	—		5,6	—	—
PPDS (3), (4)	—	—	—	—	—	—			—	—
RSDS and mini-LVDS (3), (4)	—	—	—	—	—	—			—	—
Differential LVPECL (5)	—	—	—	—	—	—		3,4,5,6, 7,8	—	—

Notes to Table 6–2:

(1) The default current strength setting in the Quartus II software is 50-Ω OCT without calibration for all non-voltage reference and HSTL/SSTL Class I I/O standards. The default setting is 25-Ω OCT without calibration for HSTL/SSTL Class II I/O standards.

(2) The differential SSTL-18 and SSTL-2, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards are supported only on clock input pins and PLL output clock pins.

(3) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only for Cyclone IV E devices and right I/O banks 5 and 6 only for Cyclone IV GX devices. Differential outputs in column I/O banks require an external resistor network.

(4) This I/O standard is supported for outputs only.

(5) This I/O standard is supported for clock inputs only

(6) The default Quartus II slew rate setting is in bold; **2** for all I/O standards that supports slew rate option.

(7) Differential SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards do not support Class II output.

(8) Cyclone IV GX devices only support right I/O pins.

(9) Altera not only offers current strength that meets the industrial standard specification but also other additional current strengths.

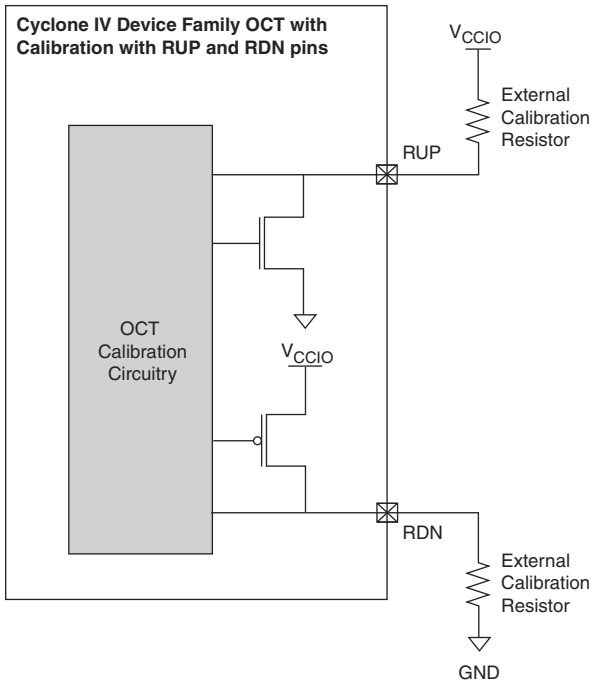
☞ For more details about the differential I/O standards supported in Cyclone IV I/O banks, refer to "High-Speed I/O Interface" on page 6–24.

On-Chip Series Termination with Calibration

Cyclone IV devices support R_S OCT with calibration in the top, bottom, and right I/O banks. The R_S OCT calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the I/O buffer impedance until they match (as shown in Figure 6–2).

Figure 6–3 shows the external calibration resistors setup on the RUP and RDN pins and the associated OCT calibration circuitry.

Figure 6–3. Cyclone IV Devices R_S OCT with Calibration Setup



RUP and RDN pins go to a tri-state condition when calibration is completed or not running. These two pins are dual-purpose I/Os and function as regular I/Os if you do not use the calibration circuit.

On-Chip Series Termination Without Calibration

Cyclone IV devices support driver impedance matching to match the impedance of the transmission line, which is typically 25 or 50 Ω. When used with the output drivers, OCT sets the output driver impedance to 25 or 50 Ω. Cyclone IV devices also support I/O driver series termination (R_S = 50 Ω) for SSTL-2 and SSTL-18.

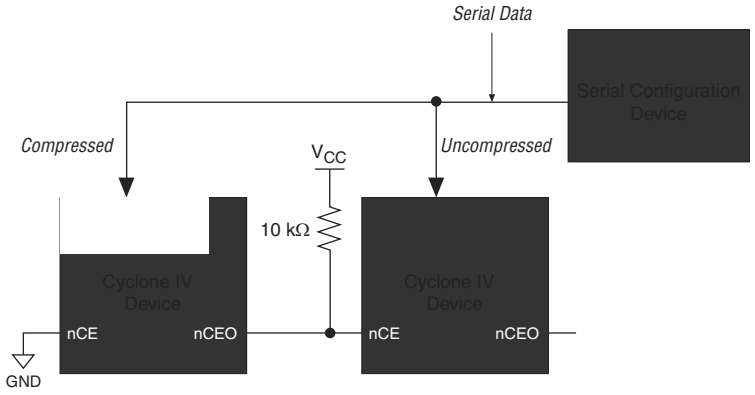
3. Click the **Configuration** tab.
4. Turn on **Generate compressed bitstreams**.
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

You can enable compression when creating programming files from the **Convert Programming Files** dialog box. To enable compression, perform the following steps:

1. On the File menu, click **Convert Programming Files**.
2. Under **Output programming file**, select your desired file type from the **Programming file type** list.
3. If you select **Programmer Object File (.pof)**, you must specify the configuration device in the **Configuration device** list.
4. Under **Input files to convert**, select **SOF Data**.
5. Click **Add File** to browse to the Cyclone IV device SRAM object files (**.sof)**.
6. In the **Convert Programming Files** dialog box, select the **.pof** you added to **SOF Data** and click **Properties**.
7. In the **SOF File Properties** dialog box, turn on the **Compression** option.

When multiple Cyclone IV devices are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 8–1 shows a chain of two Cyclone IV devices. The first device has compression enabled and receives compressed bitstream from the configuration device. The second device has the compression feature disabled and receives uncompressed data. You can generate programming files for this setup in the **Convert Programming Files** dialog box.

Figure 8–1. Compressed and Uncompressed Configuration Data in the Same Configuration File



Configuration Requirement

This section describes Cyclone IV device configuration requirement and includes the following topics:

- "Power-On Reset (POR) Circuit" on page 8–4
- "Configuration File Size" on page 8–4
- "Power Up" on page 8–6

The first Cyclone IV device in the chain is the configuration master and it controls the configuration of the entire chain. Other Altera devices that support PS configuration can also be part of the chain as configuration slaves.

☞ In the multi-device AS configuration, the board trace length between the serial configuration device and the master device of the Cyclone IV device must follow the recommendations in Table 8–7 on page 8–18.

The nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8–3 on page 8–13. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on CONF_DONE line and all devices simultaneously enter initialization mode.

☞ Although you can cascade Cyclone IV devices, serial configuration devices cannot be cascaded or chained together.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device, enable the compression feature, or both. When configuring multiple devices, the size of the bitstream is the sum of the individual device's configuration bitstream.

Configuring Multiple Cyclone IV Devices with the Same Design

Certain designs require that you configure multiple Cyclone IV devices with the same design through a configuration bitstream, or a **.sof**. You can do this through the following methods:

- Multiple **.sof**
- Single **.sof**

☞ For both methods, the serial configuration devices cannot be cascaded or chained together.

Multiple SRAM Object Files

Two copies of the **.sof** are stored in the serial configuration device. Use the first copy to configure the master device of the Cyclone IV device and the second copy to configure all remaining slave devices concurrently. All slave devices must have the same density and package. The setup is similar to Figure 8–3 on page 8–13.

To configure four identical Cyclone IV devices with the same **.sof**, you must set up the chain similar to the example shown in Figure 8–4. The first device is the master device and its MSEL pins must be set to select AS configuration. The other three slave devices are set up for concurrent configuration and their MSEL pins must be set to select PS configuration. The nCEO pin from the master device drives the nCE input pins on all three slave devices, as well as the DATA and DCLK pins that connect in parallel to all

The nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

Guidelines for Connecting Parallel Flash to Cyclone IV E Devices for an AP Interface

For single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and Cyclone IV E devices must follow the recommendations listed in Table 8–11. These recommendations also apply to an AP configuration with multiple bus masters.

Table 8–11. Maximum Trace Length and Loading for AP Configuration

Cyclone IV E AP Pins	Maximum Board Trace Length from Cyclone IV E Device to Flash Device (inches)	Maximum Board Load (pF)
DCLK	6	15
DATA[15..0]	6	30
PADD[23..0]	6	30
nRESET	6	30
Flash_nCE	6	30
nOE	6	30
nAVD	6	30
nWE	6	30
I/O (1)	6	30

Note to Table 8–11:

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, the master must assert nCONFIG low for at least 500 ns to reset the master Cyclone IV E device and override the weak 10-kΩ pull-down resistor on the nCE pin. This resets the master Cyclone IV E device and causes it to tri-state its AP configuration bus. The other master device then takes control of the AP configuration bus. After the other master device is done, it releases the AP configuration bus, then releases the nCE pin, and finally pulses nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

Use the ACTIVE_DISENGAGE instruction with the CONFIG_IO instruction to interrupt configuration. Table 8–16 lists the sequence of instructions to use for various CONFIG_IO usage scenarios.

Table 8–16. JTAG CONFIG_IO (without JTAG_PROGRAM) Instruction Flows *(1)*

JTAG Instruction	Configuration Scheme and Current State of the Cyclone IV Device											
	Prior to User Mode (Interrupting Configuration)				User Mode				Power Up			
	PS	FPP	AS	AP	PS	FPP	AS	AP	PS	FPP	AS	AP
ACTIVE_DISENGAGE	O	O	O	O	O	O	O	O	—	—	—	—
CONFIG_IO	R	R	R	R	R	R	R	R	NA	NA	NA	NA
JTAG Boundary Scan Instructions (no JTAG_PROGRAM)	O	O	O	O	O	O	O	O	—	—	—	—
ACTIVE_ENGAGE	A	A	R *(2)*	R *(2)*	A	A	R *(2)*	R *(2)*	—	—	—	—
PULSE_NCONFIG			A *(3)*	A *(3)*			O	O	—	—	—	—
Pulse nCONFIG pin			A *(3)*	A *(3)*			O	O	—	—	—	—
JTAG TAP Reset	R	R	R	R	R	R	R	R	—	—	—	—

Notes to Table 8–16:

(1) You must execute "R" indicates that the instruction before the next instruction, "O" indicates the optional instruction, "A" indicates that the instruction must be executed, and "NA" indicates that the instruction is not allowed in this mode.

(2) Required if you use ACTIVE_DISENGAGE.

(3) Neither of the instruction is required if you use ACTIVE_ENGAGE.

The CONFIG_IO instruction does not hold nSTATUS low until reconfiguration. You must disengage the AS or AP configuration controller by issuing the ACTIVE_DISENGAGE and ACTIVE_ENGAGE instructions when active configuration is interrupted. You must issue the ACTIVE_DISENGAGE instruction alone or prior to the CONFIG_IO instruction if the JTAG_PROGRAM instruction is to be issued later (Table 8–17). This puts the active configuration controllers into the idle state. The active configuration controller is re-engaged after user mode is reached through JTAG programming (Table 8–17).

While executing the CONFIG_IO instruction, all user I/Os are tri-stated.

If reconfiguration after interruption is performed using configuration modes (rather than using JTAG_PROGRAM), it is not necessary to issue the ACTIVE_DISENGAGE instruction prior to CONFIG_IO. You can start reconfiguration by either pulling nCONFIG low for at least 500 ns or issuing the PULSE_NCONFIG instruction. If the ACTIVE_DISENGAGE instruction was issued and the JTAG_PROGRAM instruction fails to enter user mode, you must issue the ACTIVE_ENGAGE instruction to reactivate the active configuration controller. Issuing the ACTIVE_ENGAGE instruction also triggers reconfiguration in configuration modes; therefore, it is not necessary to pull nCONFIG low or issue the PULSE_NCONFIG instruction.

Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

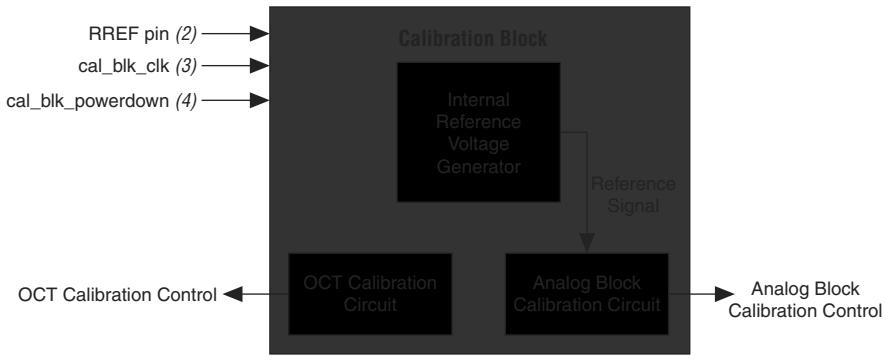
Chapter 1. Cyclone IV Transceivers Architecture
Revised: *February 2015*
Part Number: *CYIV-52001-3.7*

Chapter 2. Cyclone IV Reset Control and Power Down
Revised: *September 2014*
Part Number: *CYIV-52002-1.4*

Chapter 3. Cyclone IV Dynamic Reconfiguration
Revised: *November 2011*
Part Number: *CYIV-52003-2.1*

The calibration block internally generates a constant internal reference voltage, independent of PVT variations and uses this voltage and the external reference resistor on the RREF pin to generate constant reference currents. The OCT calibration circuit calibrates the OCT resistors present in the transceiver channels. Figure 1–41 shows the calibration block diagram.

Figure 1–41. Input Signals to the Calibration Blocks (1)



Notes to Figure 1–41:

(1) All transceiver channels use the same calibration block clock and power down signals.

(2) Connect a 2 kΩ (tolerance max ± 1%) external resistor to the RREF pin to ground. The RREF resistor connection in the board must be free from any external noise.

(3) Supports up to 125 MHz clock frequency. Use either dedicated global clock or divide-down logic from the FPGA fabric to generate a slow clock on the local clock routing.

(4) The calibration block restarts the calibration process following deassertion of the cal_blk_powerdown signal.

PCI-Express Hard IP Block

Figure 1–42 shows the block diagram of the PCIe hard IP block implementing the PHY MAC, Data Link Layer, and Transaction Layer for PCIe interfaces. The PIPE interface is used as the interface between the transceiver and the hard IP block.

Figure 1–42. PCI Express Hard IP High-Level Block Diagram

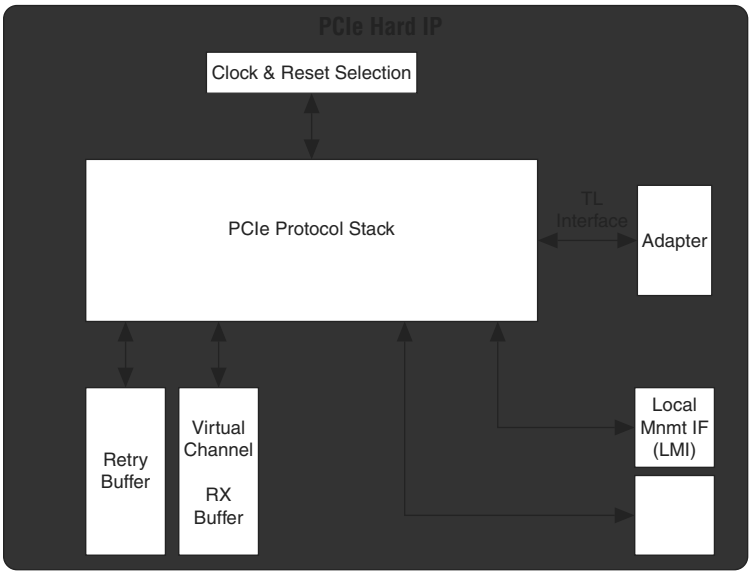


Figure 1–45 and Figure 1–46 show the supported transceiver configurations in Basic mode with the 8-bit and 10-bit PMA-PCS interface width respectively.

Figure 1–45. Supported Transceiver Configurations in Basic Mode with the 8-bit PMA-PCS Interface Width