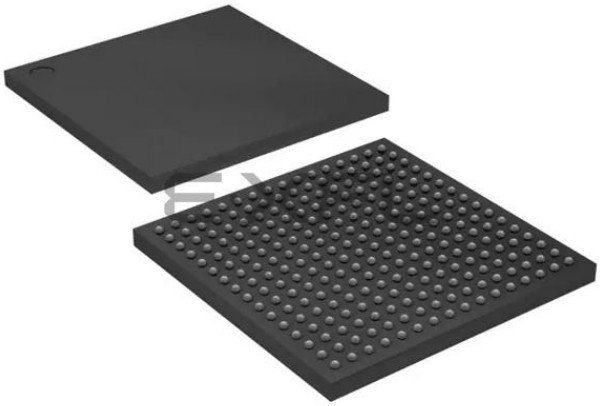

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	165
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce15f17c6

- Cyclone IV GX devices offer up to eight high-speed transceivers that provide:
  - Data rates up to 3.125 Gbps
  - 8B/10B encoder/decoder
  - 8-bit or 10-bit physical media attachment (PMA) to physical coding sublayer (PCS) interface
  - Byte serializer/deserializer (SERDES)
  - Word aligner
  - Rate matching FIFO
  - TX bit slipper for Common Public Radio Interface (CPRI)
  - Electrical idle
  - Dynamic channel reconfiguration allowing you to change data rates and protocols on-the-fly
  - Static equalization and pre-emphasis for superior signal integrity
  - 150 mW per channel power consumption
  - Flexible clocking structure to support multiple protocols in a single transceiver block
- Cyclone IV GX devices offer dedicated hard IP for PCI Express (PIPE) (PCIe) Gen 1:
  - ×1, ×2, and ×4 lane configurations
  - End-point and root-port configurations
  - Up to 256-byte payload
  - One virtual channel
  - 2 KB retry buffer
  - 4 KB receiver (Rx) buffer
- Cyclone IV GX devices offer a wide range of protocol support:
  - PCIe (PIPE) Gen 1 ×1, ×2, and ×4 (2.5 Gbps)
  - Gigabit Ethernet (1.25 Gbps)
  - CPRI (up to 3.072 Gbps)
  - XAUI (3.125 Gbps)
  - Triple rate serial digital interface (SDI) (up to 2.97 Gbps)
  - Serial RapidIO (3.125 Gbps)
  - Basic mode (up to 3.125 Gbps)
  - V-by-One (up to 3.0 Gbps)
  - DisplayPort (2.7 Gbps)
  - Serial Advanced Technology Attachment (SATA) (up to 3.0 Gbps)
  - OBSAI (up to 3.072 Gbps)

For more information about the number of GCLK networks in each device density, refer to the *Cyclone IV FPGA Device Family Overview* chapter.

GCLK Network

GCLKs drive throughout the entire device, feeding all device quadrants. All resources in the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks, and M9K memory blocks) can use GCLKs as clock sources. Use these clock network resources for control signals, such as clock enables and clears fed by an external pin. Internal logic can also drive GCLKs for internally generated GCLKs and asynchronous clears, clock enables, or other control signals with high fan-out.

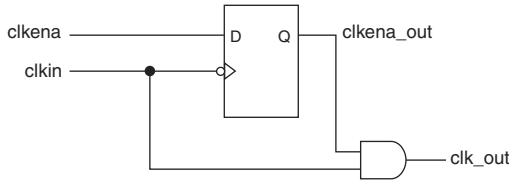
Table 5–1, Table 5–2 on page 5–4, and Table 5–3 on page 5–7 list the connectivity of the clock sources to the GCLK networks.

Table 5–1. GCLK Network Connections for EP4CGX15, EP4CGX22, and EP4CGX30 (1), (2) (Part 1 of 2)

GCLK Network Clock Sources	GCLK Networks																			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CLK4/DIFFCLK_2n	—	—	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—
CLK5/DIFFCLK_2p	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
CLK6/DIFFCLK_3n	—	—	—	—	—	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	—	—
CLK7/DIFFCLK_3p	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
CLK8/DIFFCLK_5n	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	✓	—	—	—	—	—
CLK9/DIFFCLK_5p	—	—	—	—	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—
CLK10/DIFFCLK_4n/REFCLK1n	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓	—	—	—	—	—
CLK11/DIFFCLK_4p/REFCLK1p	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—
CLK12/DIFFCLK_7p/REFCLK0p	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	✓
CLK13/DIFFCLK_7n/REFCLK0n	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	—	—
CLK14/DIFFCLK_6p	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓
CLK15/DIFFCLK_6n	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—
PLL_1_C0	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—
PLL_1_C1	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓
PLL_1_C2	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—
PLL_1_C3	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—
PLL_1_C4	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓
PLL_2_C0	✓	—	—	✓	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—
PLL_2_C1	—	✓	—	—	✓	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—
PLL_2_C2	✓	—	✓	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—
PLL_2_C3	—	✓	—	✓	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—
PLL_2_C4	—	—	✓	—	✓	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—
PLL_3_C0	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	✓	—	—	✓	—

Figure 5–7 shows how to implement the clkena signal with a single register.

Figure 5–7. clkena Implementation

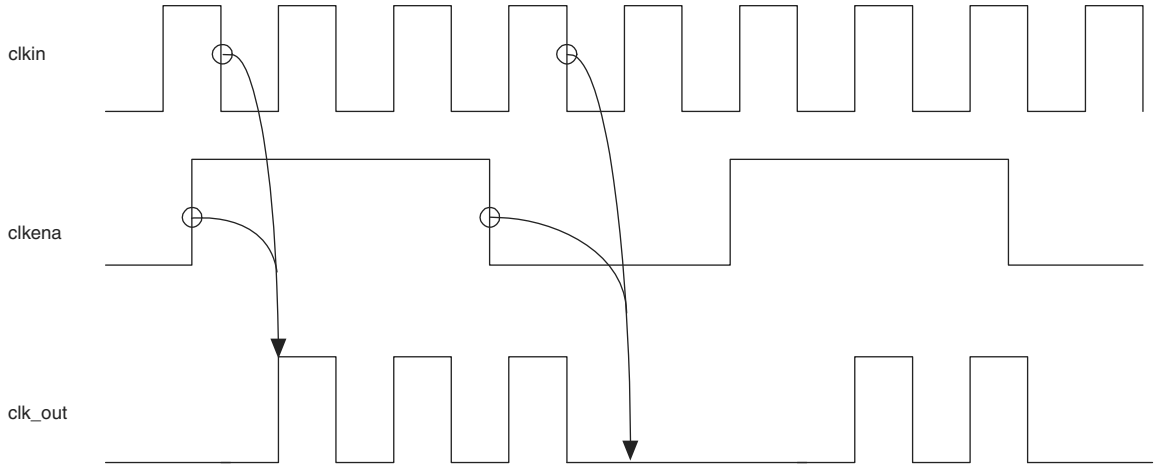


The clkena circuitry controlling the output C0 of the PLL to an output pin is implemented with two registers instead of a single register, as shown in Figure 5–7.

Figure 5–8 shows the waveform example for a clock output enable. The clkena signal is sampled on the falling edge of the clock (clkin).

This feature is useful for applications that require low power or sleep mode.

Figure 5–8. clkena Implementation: Output Enable



The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the clkena signals when switching the clock source to the PLLs or the GCLK. The recommended sequence is:

1. Disable the primary output clock by de-asserting the clkena signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before reasserting the clkena signal. The exact number of clock cycles you must wait before enabling the secondary clock is design-dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual-clock domain application, such as a system that turns on the redundant clock if the previous clock stops running. Your design can automatically perform clock switchover when the clock is no longer toggling, or based on the user control signal, `clkswitch`.

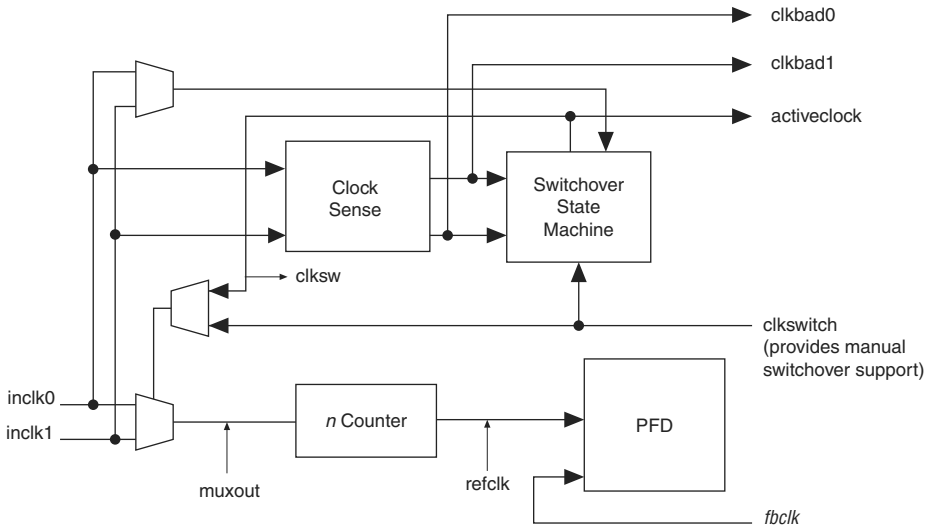
Automatic Clock Switchover

PLLs of Cyclone IV devices support a fully configurable clock switchover capability.

When the current reference clock is not present, the clock-sense block automatically switches to the backup clock for PLL reference. The clock switchover circuit also sends out three status signals—`clkbad0`, `clkbad1`, and `activeclock`—from the PLL to implement a custom switchover circuit. You can select a clock source at the backup clock by connecting it to the `inclk1` port of the PLL in your design.

Figure 5–17 shows the block diagram of the switchover circuit built into the PLL.

Figure 5–17. Automatic Clock Switchover Circuit



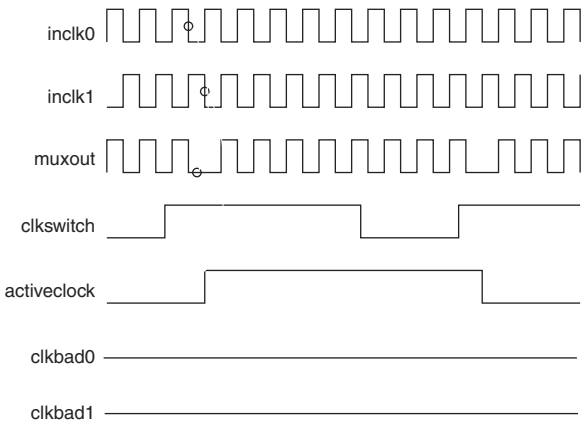
There are two ways to use the clock switchover feature:

- Use the switchover circuitry for switching from `inclk0` to `inclk1` running at the same frequency. For example, in applications that require a redundant clock with the same frequency as the reference clock, the switchover state machine generates a signal that controls the multiplexer select input shown in Figure 5–17. In this case, `inclk1` becomes the reference clock for the PLL. This automatic switchover can switch back and forth between the `inclk0` and `inclk1` clocks any number of times, when one of the two clocks fails and the other clock is available.
- Use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 200 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than

In this mode, the activeclock signal mirrors the clkswitch signal. As both blocks are still functional during the manual switch, neither clkbad signals go high. Because the switchover circuit is positive edge-sensitive, the falling edge of the clkswitch signal does not cause the circuit to switch back from inclk1 to inclk0. When the clkswitch signal goes high again, the process repeats. The clkswitch signal and the automatic switch only works depending on the availability of the clock that is switched to. If the clock is unavailable, the state machine waits until the clock is available.

When CLKSWITCH = 1, it overrides the automatic switch-over function. As long as clkswitch signal is high, further switch-over action is blocked.

Figure 5–19. Clock Switchover Using the clkswitch Control *(1)*



Note to Figure 5–19:

(1) Both inclk0 and inclk1 must be running when the clkswitch signal goes high to start a manual clock switchover event.

Manual Clock Switchover

PLLs of Cyclone IV devices support manual switchover, in which the clkswitch signal controls whether inclk0 or inclk1 is the input clock to the PLL. The characteristics of a manual switchover are similar to the manual override feature in an automatic clock switchover, in which the switchover circuit is edge-sensitive. When the clkswitch signal goes high, the switchover sequence starts. The falling edge of the clkswitch signal does not cause the circuit to switch back to the previous input clock.

For more information about PLL software support in the Quartus II software, refer to the *ALTPLL Megafunction User Guide*.

Guidelines

Use the following guidelines to design with clock switchover in PLLs:

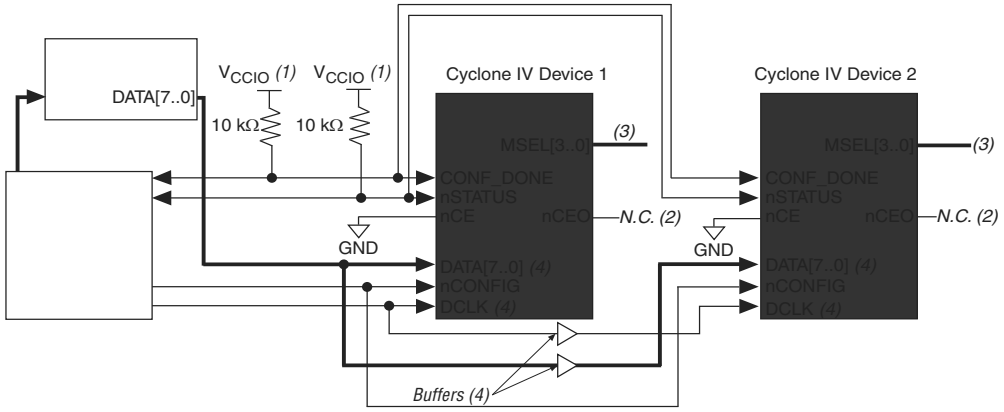
- Clock loss detection and automatic clock switchover require the inclk0 and inclk1 frequencies be within 20% of each other. Failing to meet this requirement causes the clkbad0 and clkbad1 signals to function improperly.

DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. All devices initialize and enter user mode at the same time, because all device CONF_DONE pins are tied together.

All nSTATUS and CONF_DONE pins are tied together and if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

Figure 8–21 shows multi-device FPP configuration when both Cyclone IV devices are receiving the same configuration data. Configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be of the same density and package. All devices start and complete configuration at the same time.

Figure 8–21. Multi-Device FPP Configuration Using an External Host When Both Devices Receive the Same Data



Notes to Figure 8–21:

(1) You must connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices are left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8–4 on page 8–8 and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot outlined in Equation 8–1 on page 8–5.

You can use a single configuration chain to configure Cyclone IV devices with other Altera devices that support FPP configuration. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device starts reconfiguration in all devices, tie all the CONF_DONE and nSTATUS pins together.

For more information about configuring multiple Altera devices in the same configuration chain, refer to *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*.

The **.rbf** used by the JRunner software driver cannot be a compressed **.rbf** because the JRunner software driver uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

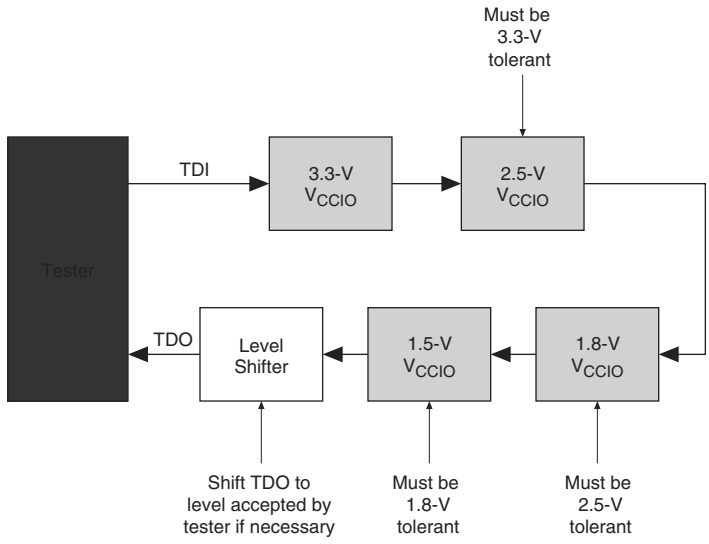
For more information about the JRunner software driver, refer to *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website at (www.altera.com).

Combining JTAG and AS Configuration Schemes

You can combine the AS configuration scheme with the JTAG-based configuration (Figure 8–28). This setup uses two 10-pin download cable headers on the board. One download cable is used in JTAG mode to configure the Cyclone IV device directly through the JTAG interface. The other download cable is used in AS mode to program the serial configuration device in-system through the AS programming interface. If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration terminates.

Figure 10–3 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 10–3. JTAG Chain of Mixed Voltages



Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1/IEEE Std. 1149.6 BST-capable device that can be tested.

For more information about how to download BSDL files for IEEE Std. 1149.1-compliant Cyclone IV E devices, refer to *IEEE Std. 1149.1 BSDL Files*.

For more information about how to download BSDL files for IEEE Std. 1149.6-compliant Cyclone IV GX devices, refer to *IEEE Std. 1149.6 BSDL Files*.

You can also generate BSDL files (pre-configuration and post-configuration) for IEEE Std. 1149.1/IEEE Std. 1149.6-compliant Cyclone IV devices with the Quartus® II software version 9.1 SP1 and later. For more information about the procedure to generate BSDL files using the Quartus II software, refer to *BSDL Files Generation in Quartus II*.

Transmitter Channel Datapath

The following sections describe the Cyclone IV GX transmitter channel datapath architecture as shown in Figure 1–3:

- TX Phase Compensation FIFO
- Byte Serializer
- 8B/10B Encoder
- Serializer
- Transmitter Output Buffer

TX Phase Compensation FIFO

The TX phase compensation FIFO compensates for the phase difference between the low-speed parallel clock and the FPGA fabric interface clock, when interfacing the transmitter channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP). The FIFO is four words deep, with latency between two to three parallel clock cycles. Figure 1–4 shows the TX phase compensation FIFO block diagram.

Figure 1–4. TX Phase Compensation FIFO Block Diagram

Note to Figure 1–4:

(1) The x refers to the supported 8-, 10-, 16-, or 20-bits transceiver channel width.

The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in Deterministic Latency functional mode. For more information, refer to "Deterministic Latency Mode" on page 1–73.

For more information about FIFO clocking, refer to "FPGA Fabric-Transceiver Interface Clocking" on page 1–43.

Byte Serializer

The byte serializer divides the input datapath width by two to allow transmitter channel operation at higher data rates while meeting the maximum FPGA fabric frequency limit. This module is required in configurations that exceed the maximum FPGA fabric-transceiver interface clock frequency limit and optional in configurations that do not.

For the FPGA fabric-transceiver interface frequency specifications, refer to the *Cyclone IV Device Data Sheet*.

In a DC-coupled link, the transmitter DC common mode voltage is seen unblocked at the receiver input buffer as shown in Figure 1–13. The link common mode voltage depends on the transmitter common mode voltage and the receiver common mode voltage. When using the receiver OCT and on-chip biasing circuitry in a DC coupled link, you must ensure the transmitter common mode voltage is compatible with the receiver common mode requirements. If you disable the OCT, you must terminate and bias the receiver externally and ensure compatibility between the transmitter and the receiver common mode voltage.

Figure 1–13. DC-Coupled Link with OCT

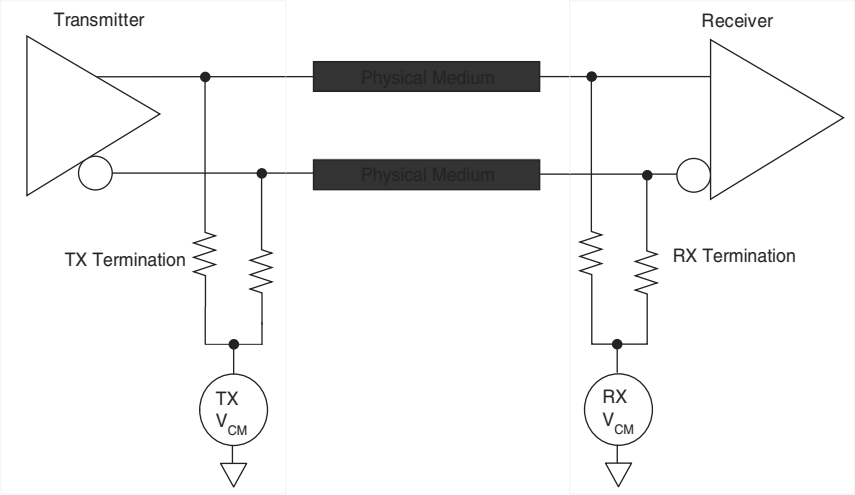
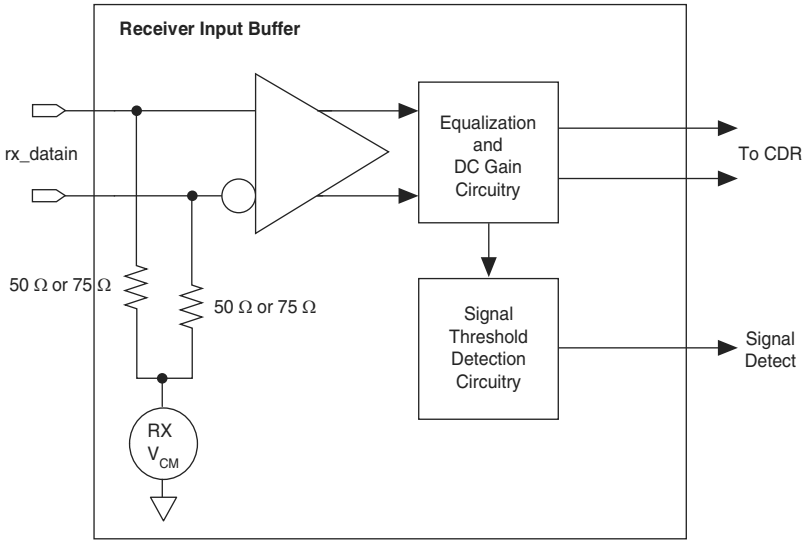


Figure 1–14 shows the receiver input buffer block diagram.

Figure 1–14. Receiver Input Buffer Block Diagram



The receiver input buffers support the following features:

Actual lock time depends on the transition density of the incoming data and the ppm difference between the receiver input reference clock and the upstream transmitter reference clock.

Transition from the LTD state to the LTR state occurs when either of the following conditions is met:

- Signal detection circuitry indicates the absence of valid signal levels at the receiver input buffer. This condition is valid for PCI Express (PIPE) mode only. CDR transitions are not dependent on signal detection circuitry in other modes.
- The recovered clock is not within the configured ppm frequency threshold setting with respect to CDR clocks from multipurpose PLLs.

In automatic lock mode, the switch from LTR to LTD states is indicated by the assertion of the `rx_freqlocked` signal and the switch from LTD to LTR states indicated by the de-assertion of the `rx_freqlocked` signal.

Manual Lock Mode

State transitions are controlled manually by using `rx_locktorefclk` and `rx_locktodata` ports. The LTR/LTD controller sets the CDR state depending on the logic level on the `rx_locktorefclk` and `rx_locktodata` ports. This mode provides the flexibility to control the CDR for a reduced lock time compared to the automatic lock mode. In automatic lock mode, the LTR/LTD controller relies on the ppm detector and the phase relationship detector to set the CDR in LTR or LTD mode. The ppm detector and phase relationship detector reaction times can be too long for some applications that require faster CDR lock time.

In manual lock mode, the `rx_freqlocked` signal is asserted when the CDR is in LTD state and de-asserted when CDR is in LTR state. For descriptions of `rx_locktorefclk` and `rx_locktodata` port controls, refer to Table 1–27 on page 1–87.

If you do not enable the optional `rx_locktorefclk` and `rx_locktodata` ports, the Quartus II software automatically configures the LTR/LTD controller in automatic lock mode.

The recommended transceiver reset sequence varies depending on the CDR lock mode. For more information about the reset sequence recommendations, refer to the *Reset Control and Power Down for Cyclone IV GX Devices* chapter.

Deserializer

The deserializer converts received serial data from the receiver input buffer to parallel 8- or 10-bit data. Serial data is assumed to be received from the LSB to the MSB. The deserializer operates with the high-speed recovered clock from the CDR with the frequency at half of the serial data rate.

Byte Deserializer

The byte deserializer halves the FPGA fabric-transceiver interface frequency while doubles the parallel data width to the FPGA fabric.

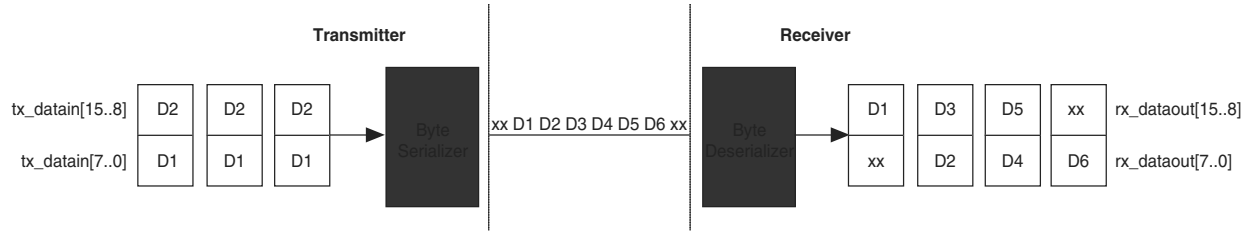
For example, when operating an EP4CGX150 receiver channel at 3.125 Gbps with deserialization factor of 10, the receiver PCS datapath runs at 312.5 MHz. The byte deserializer converts the 10-bit data at 312.5 MHz into 20-bit data at 156.25 MHz before forwarding the data to the FPGA fabric.

Byte Ordering

In the 16- or 20-bit FPGA fabric-transceiver interface, the byte deserializer receives one data byte (8 or 10 bits) and deserializes it into two data bytes (16 or 20 bits). Depending on when the receiver PCS logic comes out of reset, the byte ordering at the output of the byte deserializer may not match the original byte ordering of the transmitted data. The byte misalignment resulting from byte deserialization is unpredictable because it depends on which byte is being received by the byte deserializer when it comes out of reset.

Figure 1–23 shows a scenario where the most significant byte and the least significant byte of the two-byte transmitter data appears straddled across two word boundaries after the data is deserialized at the receiver.

Figure 1–23. Example of Byte Deserializer at the Receiver



The byte ordering block restores the proper byte ordering by performing the following actions:

- Look for the user-programmed byte ordering pattern in the byte-deserialized data
- Inserts a user-programmed pad byte if the user-programmed byte ordering pattern is found in the most significant byte position

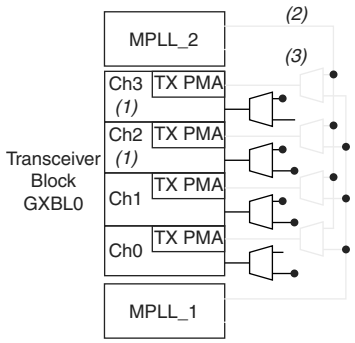
You must select a byte ordering pattern that you know appears at the least significant byte position of the parallel transmitter data.

The byte ordering block is supported in the following receiver configurations:

- 16-bit FPGA fabric-transceiver interface, 8B/10B disabled, and the word aligner in manual alignment mode. Program a custom 8-bit byte ordering pattern and 8-bit pad byte.
- 16-bit FPGA fabric-transceiver interface, 8B/10B enabled, and the word aligner in automatic synchronization state machine mode. Program a custom 9-bit byte ordering pattern and 9-bit pad byte. The MSB of the 9-bit byte ordering pattern and pad byte represents the control identifier of the 8B/10B decoded data.

Figure 1–31 and Figure 1–32 show the high- and low-speed clock distribution for transceivers in F324 and smaller packages, and in F484 and larger packages in non-bonded channel configuration.

Figure 1–31. Clock Distribution in Non-Bonded Channel Configuration for Transceivers in F324 and Smaller Packages

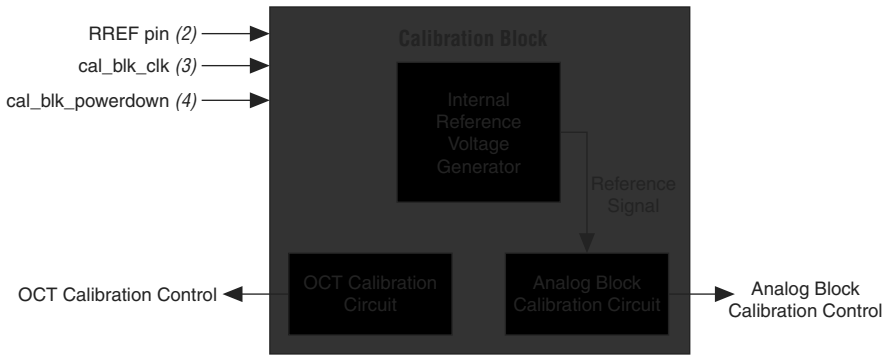


Notes to Figure 1–31:

(1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
(2) High-speed clock.
(3) Low-speed clock.

The calibration block internally generates a constant internal reference voltage, independent of PVT variations and uses this voltage and the external reference resistor on the RREF pin to generate constant reference currents. The OCT calibration circuit calibrates the OCT resistors present in the transceiver channels. Figure 1–41 shows the calibration block diagram.

Figure 1–41. Input Signals to the Calibration Blocks (1)



Notes to Figure 1–41:

(1) All transceiver channels use the same calibration block clock and power down signals.

(2) Connect a 2 kΩ (tolerance max ± 1%) external resistor to the RREF pin to ground. The RREF resistor connection in the board must be free from any external noise.

(3) Supports up to 125 MHz clock frequency. Use either dedicated global clock or divide-down logic from the FPGA fabric to generate a slow clock on the local clock routing.

(4) The calibration block restarts the calibration process following deassertion of the cal_blk_powerdown signal.

PCI-Express Hard IP Block

Figure 1–42 shows the block diagram of the PCIe hard IP block implementing the PHY MAC, Data Link Layer, and Transaction Layer for PCIe interfaces. The PIPE interface is used as the interface between the transceiver and the hard IP block.

Figure 1–42. PCI Express Hard IP High-Level Block Diagram

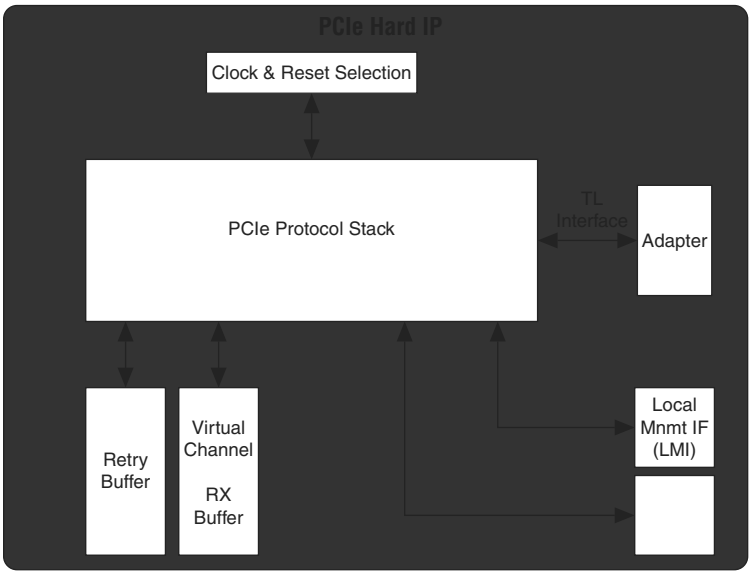
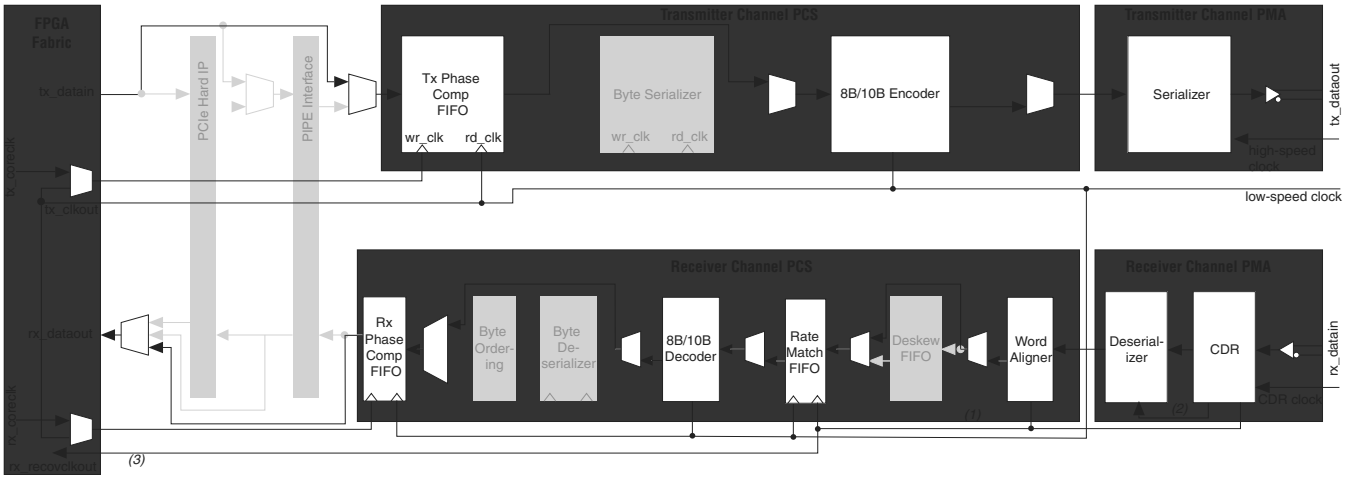


Figure 1–55 shows the transceiver channel datapath and clocking when configured in GIGE mode.

Figure 1–55. Transceiver Channel Datapath and Clocking when Configured in GIGE Mode



Notes to Figure 1–55:

(1) Low-speed recovered clock.

(2) High-speed recovered clock.

(3) Optional `rx_recovclkout` port from CDR low-speed recovered clock is available for applications such as Synchronous Ethernet.

Table 1–28. PIPE Interface Ports in ALTGX Megafunction for Cyclone IV GX (1) (Part 1 of 2)

Port Name	Input/ Output	Clock Domain	Description
fixedclk	Input	Clock signal	125-MHz clock for receiver detect and offset cancellation only in PIPE mode.
tx_detectrxloop	Input	Asynchronous signal	Receiver detect or reverse parallel loopback control. ■ A high level in the P1 power state and `tx_forceelecidle` signal asserted begins the receiver detection operation to determine if there is a valid receiver downstream. This signal must be deasserted when the `pipephydonestatus` signal indicates receiver detect completion. ■ A high level in the P0 power state with the `tx_forceelecidle` signal deasserted dynamically configures the channel to support reverse parallel loopback mode.
tx_forcedisp compliance	Input	Asynchronous signal	Force the 8B/10B encoder to encode with negative running disparity. ■ Assert only when transmitting the first byte of the PIPE-compliance pattern to force the 8B/10B encoder with a negative running disparity.
pipe8b10binvpolarity	Input	Asynchronous signal	Invert the polarity of every bit of the 10-bit input to the 8B/10B decoder
powerdn	Input	Asynchronous signal	PIPE power state control. ■ Signal is 2 bits wide and is encoded as follows: ■ 2'b00: P0 (Normal operation) ■ 2'b01: P0s (Low recovery time latency, low power state) ■ 2'b10: P1 (Longer recovery time latency, lower power state) ■ 2'b11: P2 (Lowest power state)
pipedatavalid	Output	N/A	Valid data and control on the `rx_dataout` and `rx_ctrldetect` ports indicator.
pipephydone status	Output	Asynchronous signal	PHY function completion indicator. ■ Asserted for one clock cycle to communicate completion of several PHY functions, such as power state transition and receiver detection.
pipeelecidle	Output	Asynchronous signal	Electrical idle detected or inferred at the receiver indicator. ■ When electrical idle inference is used, this signal is driven high when it infers an electrical idle condition ■ When electrical idle inference is not used, the `rx_signaldetect` signal is inverted and driven on this port.

Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2) (1)

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1–7:

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

OCT Specifications

Table 1–8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

Table 1–8. Series OCT Without Calibration Specifications for Cyclone IV Devices

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT without calibration	3.0	±30	±40	%
	2.5	±30	±40	%
	1.8	±40	±50	%
	1.5	±50	±50	%
	1.2	±50	±50	%

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1–9 lists the OCT calibration accuracy at device power-up.

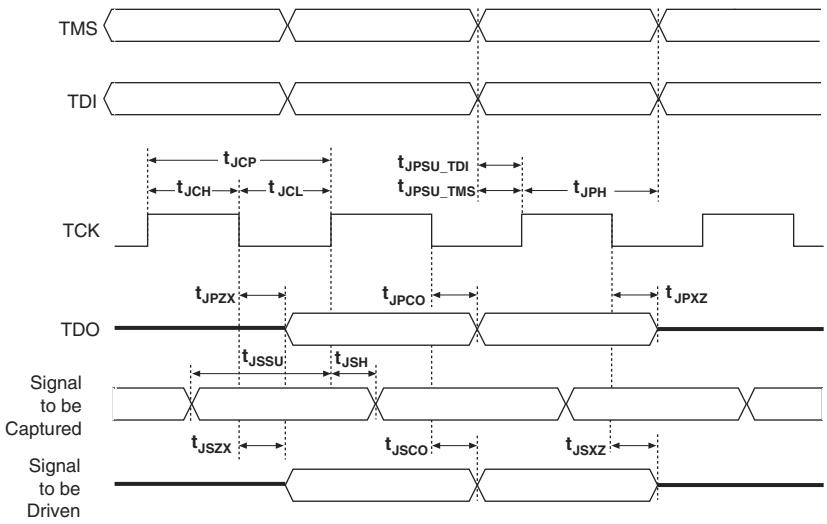
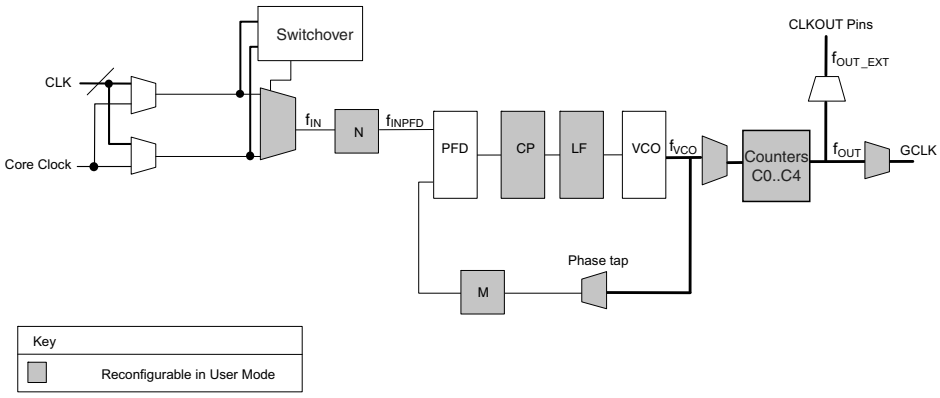
Table 1–9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices (1)

Description	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT with calibration at device power-up	3.0	±10	±10	%
	2.5	±10	±10	%
	1.8	±10	±10	%
	1.5	±10	±10	%
	1.2	±10	±10	%

Note to Table 1–9:

(1) This specification is not applicable to EP4CGX15, EP4CGX22, and EP4CGX30 devices.

Table 1–46. Glossary (Part 2 of 5)

Letter	Term	Definitions
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following highlights the PLL specification parameters: 
Q	—	—