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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

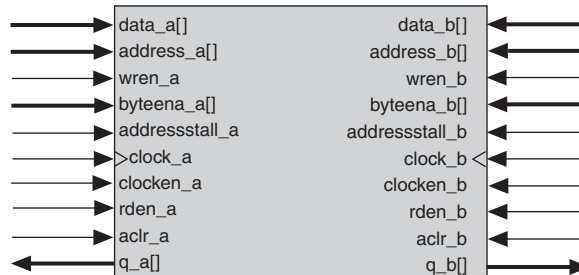
Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	165
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep4ce15f17c7">https://www.e-xfl.com/product-detail/intel/ep4ce15f17c7</a>



## True Dual-Port Mode

True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write, at two different clock frequencies. Figure 3-10 shows Cyclone IV devices true dual-port memory configuration.

**Figure 3-10. Cyclone IV Devices True Dual-Port Memory** <sup>(1)</sup>



**Note to Figure 3-10:**

(1) True dual-port memory supports input or output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M9K blocks in true dual-port mode is 512 × 16-bit (18-bit with parity).

Table 3-4 lists the possible M9K block mixed-port width configurations.

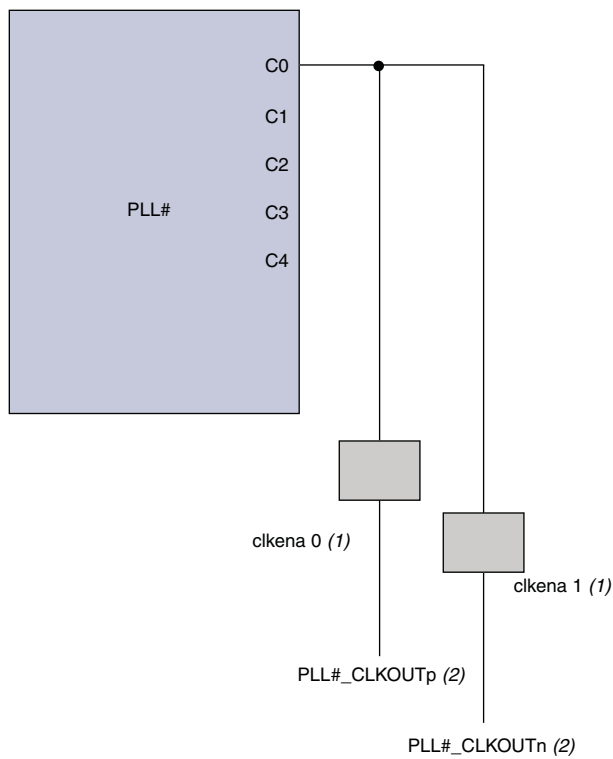
**Table 3-4. Cyclone IV Devices M9K Block Mixed-Width Configurations (True Dual-Port Mode)**

Read Port	Write Port						
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	1024 × 9	512 × 18
8192 × 1	✓	✓	✓	✓	✓	—	—
4096 × 2	✓	✓	✓	✓	✓	—	—
2048 × 4	✓	✓	✓	✓	✓	—	—
1024 × 8	✓	✓	✓	✓	✓	—	—
512 × 16	✓	✓	✓	✓	✓	—	—
1024 × 9	—	—	—	—	—	✓	✓
512 × 18	—	—	—	—	—	✓	✓

In true dual-port mode, M9K memory blocks support separate wren and rden signals. You can save power by keeping the rden signal low (inactive) when not reading. Read-during-write operations to the same address can either output “New Data” at that location or “Old Data”. To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to “Read-During-Write Operations” on page 3-15.

Figure 5-11 shows the external clock outputs for PLLs.

**Figure 5-11. External Clock Outputs for PLLs**



**Notes to Figure 5-11:**

- (1) These external clock enable signals are available only when using the ALTCLKCTRL megafunction.
- (2) PLL#\_CLKOUTp and PLL#\_CLKOUTn pins are dual-purpose I/O pins that you can use as one single-ended clock output or one differential clock output. When using both pins as single-ended I/Os, one of them can be the clock output while the other pin is configured as a regular user I/O.

Each pin of a differential output pair is 180° out of phase. The Quartus II software places the NOT gate in your design into the I/O element to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins.

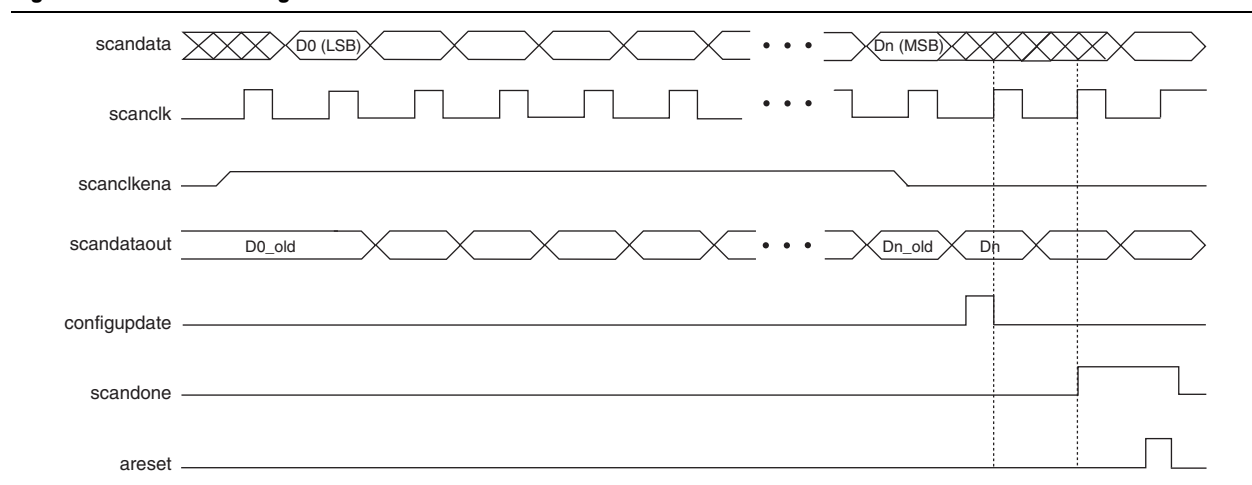


To determine which I/O standards are supported by the PLL clock input and output pins, refer to the *Cyclone IV Device I/O Features* chapter.

Cyclone IV PLLs can drive out to any regular I/O pin through the GCLK. You can also use the external clock output pins as GPIO pins if external PLL clocking is not required.

Figure 5–23 shows a functional simulation of the PLL reconfiguration feature.

**Figure 5–23. PLL Reconfiguration Scan Chain**



When reconfiguring the counter clock frequency, the corresponding counter phase shift settings cannot be reconfigured using the same interface. You can reconfigure phase shifts in real time using the dynamic phase shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase shift setting (for example, 90°) on the clock output, you must reconfigure the phase shift after reconfiguring the counter clock frequency.

### Post-Scale Counters (C0 to C4)

You can configure multiply or divide values and duty cycle of post-scale counters in real time. Each counter has an 8-bit high time setting and an 8-bit low time setting. The duty cycle is the ratio of output high or low time to the total cycle time, that is the sum of the two. Additionally, these counters have two control bits, *rbypass*, for bypassing the counter, and *rseledd*, to select the output clock duty cycle.

When the *rbypass* bit is set to 1, it bypasses the counter, resulting in a divide by one. When this bit is set to 0, the PLL computes the effective division of the VCO output frequency based on the high and low time counters. For example, if the post-scale divide factor is 10, the high and low count values are set to 5 and 5, to achieve a 50–50% duty cycle. The PLL implements this duty cycle by transitioning the output clock from high-to-low on the rising edge of the VCO output clock. However, a 4 and 6 setting for the high and low count values, respectively, would produce an output clock with a 40–60% duty cycle.

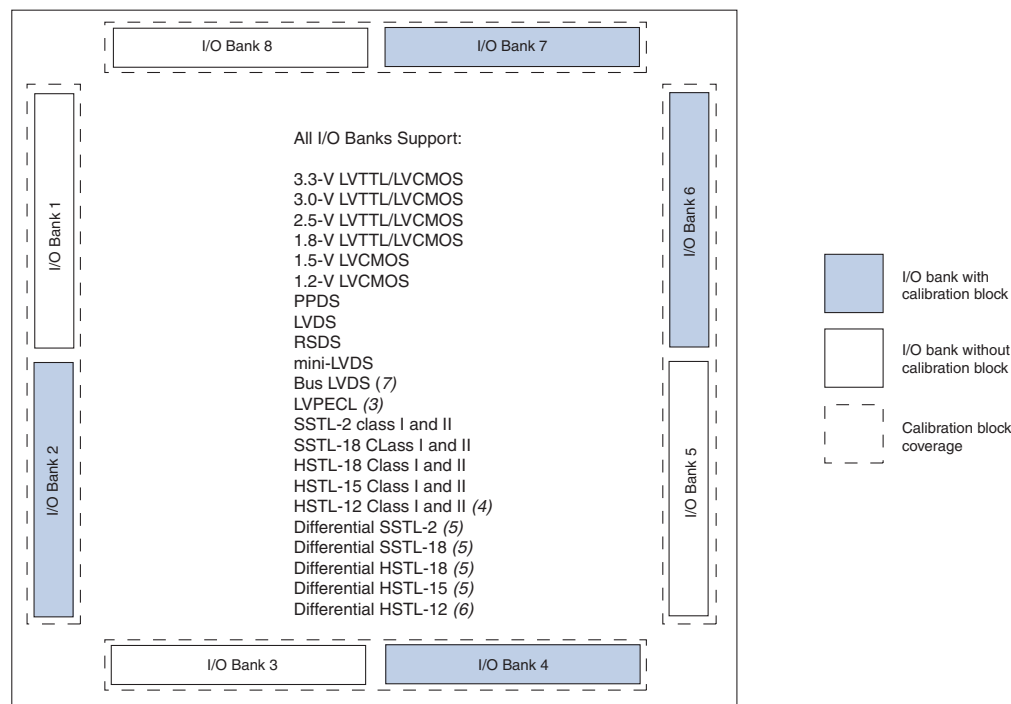
The *rseledd* bit indicates an odd divide factor for the VCO output frequency with a 50% duty cycle. For example, if the post-scale divide factor is three, the high and low time count values are 2 and 1, respectively, to achieve this division. This implies a 67%–33% duty cycle. If you need a 50%–50% duty cycle, you must set the *rseledd* control bit to 1 to achieve this duty cycle despite an odd division factor. The PLL implements this duty cycle by transitioning the output clock from high-to-low on a falling edge of the VCO output clock. When you set *rseledd* = 1, subtract 0.5 cycles from the high time and add 0.5 cycles to the low time.

For example:

- High time count = 2 cycles

Figure 6-9 shows the overview of Cyclone IV E I/O banks.

**Figure 6-9. Cyclone IV E I/O Banks (1), (2)**



**Notes to Figure 6-9:**

- (1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.
- (2) True differential (PPDS, LVDS, mini-LVDS, and RSDS) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.
- (3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
- (4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.
- (5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. Differential SSTL-18, differential HSTL-18, and HSTL-15 I/O standards do not support Class II output.
- (6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 3, 4, 7, and 8.
- (7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses true LVDS input buffer.

**Table 6-12. Document Revision History (Part 2 of 2)**

Date	Version	Changes
February 2010	2.0	<ul style="list-style-type: none"> <li>■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release.</li> <li>■ Updated Table 6-2, Table 6-3, and Table 6-10.</li> <li>■ Updated “I/O Banks” section.</li> <li>■ Added Figure 6-9.</li> <li>■ Updated Figure 6-10 and Figure 6-11.</li> <li>■ Added Table 6-4, Table 6-6, and Table 6-8.</li> </ul>
November 2009	1.0	Initial release.

This chapter describes the memory interface pin support and the external memory interface features of Cyclone® IV devices.

In addition to an abundant supply of on-chip memory, Cyclone IV devices can easily interface with a broad range of external memory devices, including DDR2 SDRAM, DDR SDRAM, and QDR II SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.



Altera recommends that you construct all DDR2 or DDR SDRAM external memory interfaces using the Altera® ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2 or DDR SDRAM memory controllers, third-party controllers, or a custom controller for unique application needs. Cyclone IV devices support QDR II interfaces electrically, but Altera does not supply controller or physical layer (PHY) megafunctions for QDR II interfaces.

This chapter includes the following sections:

- “Cyclone IV Devices Memory Interfaces Pin Support” on page 7-2
- “Cyclone IV Devices Memory Interfaces Features” on page 7-12



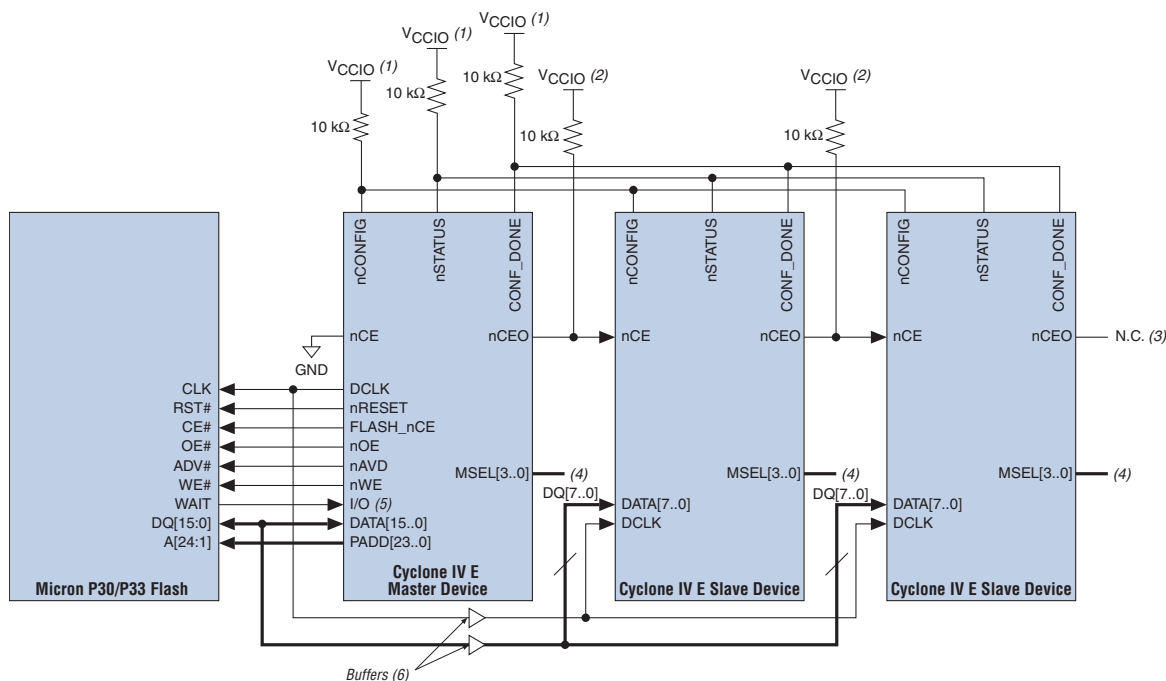
For more information about supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to the *External Memory Interface Handbook*.



## Byte-Wide Multi-Device AP Configuration

The simpler method for multi-device AP configuration is the byte-wide multi-device AP configuration. In the byte-wide multi-device AP configuration, the LSB of the DATA [7..0] pin from the flash and master device (set to the AP configuration scheme) is connected to the slave devices set to the FPP configuration scheme, as shown in Figure 8–8.

**Figure 8–8. Byte-Wide Multi-Device AP Configuration**



### Notes to Figure 8–8:

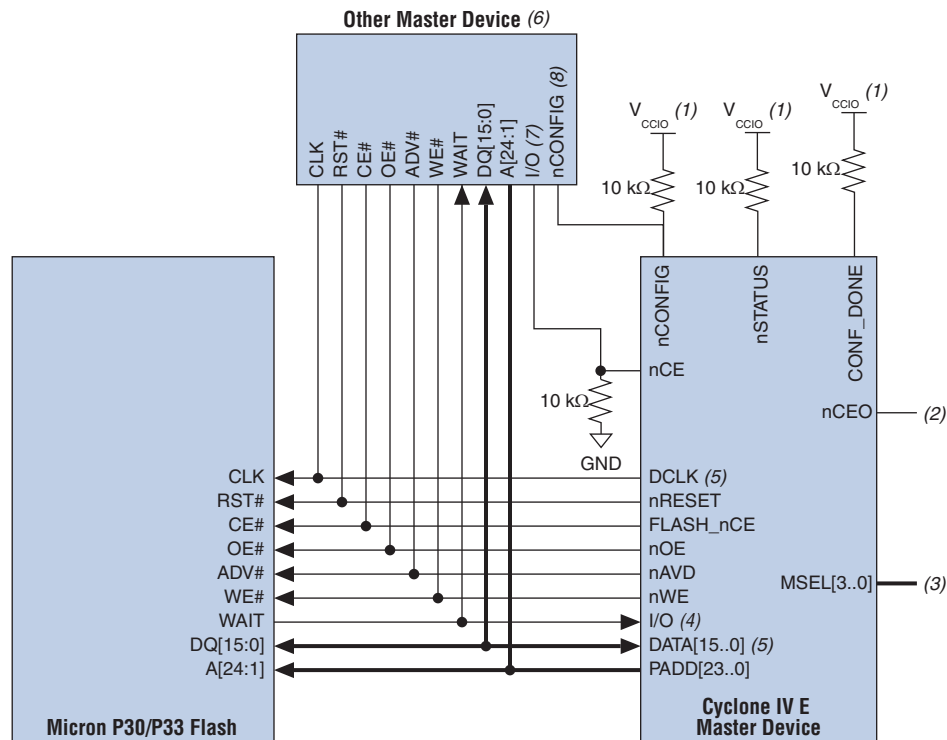
- (1) Connect the pull-up resistors to the  $V_{CCIO}$  supply of the bank in which the pin resides.
- (2) Connect the pull-up resistor to the  $V_{CCIO}$  supply voltage of the I/O bank in which the  $nCE$  pin resides.
- (3) The  $nCEO$  pin is left unconnected or used as a user I/O pin when it does not feed the  $nCE$  pin of another device.
- (4) The  $MSEL$  pin settings vary for different configuration voltage standards and POR time. You must set the master device in AP mode and the slave devices in FPP mode. To connect  $MSEL[3..0]$  for the master device in AP mode and the slave devices in FPP mode, refer to Table 8–5 on page 8–9. Connect the  $MSEL$  pins directly to  $V_{CCA}$  or GND.
- (5) The AP configuration ignores the  $WAIT$  signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the  $WAIT$  signal from the Micron P30 or P33 flash.
- (6) Connect the repeater buffers between the Cyclone IV E master device and slave devices for  $DATA[15..0]$  and  $DCLK$ . All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in “Configuration and JTAG Pin I/O Requirements” on page 8–5.

## Word-Wide Multi-Device AP Configuration

The more efficient setup is one in which some of the slave devices are connected to the LSB of the DATA [7..0] and the remaining slave devices are connected to the MSB of the DATA [15..8]. In the word-wide multi-device AP configuration, the  $nCEO$  pin of the master device enables two separate daisy chains of slave devices, allowing both chains to be programmed concurrently, as shown in Figure 8–9.

Figure 8-10 shows the AP configuration with multiple bus masters.

**Figure 8-10. AP Configuration with Multiple Bus Masters**

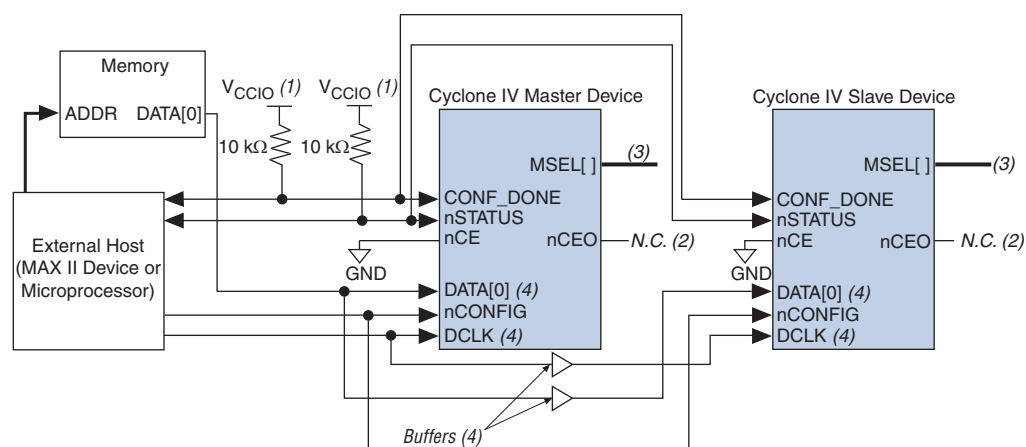


**Notes to Figure 8-10:**

- (1) Connect the pull-up resistors to the V<sub>CCIO</sub> supply of the bank in which the pin resides.
- (2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 8-5 on page 8-9. Connect the MSEL pins directly to V<sub>CCA</sub> or GND.
- (4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.
- (5) When cascading Cyclone IV E devices in a multi-device AP configuration, connect the repeater buffers between the master device and slave devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8-5.
- (6) The other master device must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8-5.
- (7) The other master device can control the AP configuration bus by driving the nCE to high with an output high on the I/O pin.
- (8) The other master device can pulse nCONFIG if it is under system control and not tied to V<sub>CCIO</sub>.

You can have multiple devices that contain the same configuration data in your system. To support this configuration scheme, all device `nCE` inputs are tied to GND, while the `nCEO` pins are left floating. `nCONFIG`, `nSTATUS`, `DCLK`, `DATA[0]`, and `CONF_DONE` configuration pins are connected to every device in the chain. To ensure signal integrity and prevent clock skew problems, configuration signals may require buffering. Ensure that the `DCLK` and `DATA` lines are buffered. Devices must be of the same density and package. All devices start and complete configuration at the same time.

**Figure 8–15. Multi-Device PS Configuration When Both Devices Receive the Same Data**



- (1) You must connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain.  $V_{CC}$  must be high enough to meet the  $V_{IH}$  specification of the I/O on the device and the external host.
- (2) The  $n_{CEO}$  pins of both devices are left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.
- (3) The  $MSEL$  pin settings vary for different configuration voltage standards and POR time. To connect the  $MSEL$  pins, refer to [Table 8-3 on page 8-8](#), [Table 8-4 on page 8-8](#), and [Table 8-5 on page 8-9](#). Connect the  $MSEL$  pins directly to  $V_{CCA}$  or GND.
- (4) All I/O inputs must maintain a maximum AC voltage of 4.1 V.  $DATA[0]$  and  $DCLK$  must fit the maximum overshoot outlined in [Equation 8-1 on page 8-5](#).

You can perform JTAG testing on Cyclone IV devices before, during, and after configuration. Cyclone IV devices support the `BYPASS`, `IDCODE`, and `SAMPLE` instructions during configuration without interrupting configuration. All other JTAG instructions can only be issued by first interrupting configuration and reprogramming I/O pins with the `ACTIVE_DISENGAGE` and `CONFIG_IO` instructions.

The `CONFIG_IO` instruction allows you to configure the I/O buffers through the JTAG port and interrupts configuration when issued after the `ACTIVE_DISENGAGE` instruction. This instruction allows you to perform board-level testing prior to configuring the Cyclone IV device or waiting for a configuration device to complete configuration. Prior to issuing the `CONFIG_IO` instruction, you must issue the `ACTIVE_DISENGAGE` instruction. This is because in Cyclone IV devices, the `CONFIG_IO` instruction does not hold `nSTATUS` low until reconfiguration, so you must disengage the active configuration mode controller when active configuration is interrupted. The `ACTIVE_DISENGAGE` instruction places the active configuration mode controllers in an idle state prior to JTAG programming. Additionally, the `ACTIVE_ENGAGE` instruction allows you to re-engage a disengaged active configuration mode controller.



You must follow a specific flow when executing the `ACTIVE_DISENGAGE`, `CONFIG_IO`, and `ACTIVE_ENGAGE` JTAG instructions in Cyclone IV devices.

The chip-wide reset (`DEV_CLRn`) and chip-wide output enable (`DEV_OE`) pins in Cyclone IV devices do not affect JTAG boundary-scan or programming operations. Toggling these pins do not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Cyclone IV devices, consider the dedicated configuration pins. Table 8-15 describes how you must connect these pins during JTAG configuration.

**Table 8-15. Dedicated Configuration Pin Connections During JTAG Configuration**

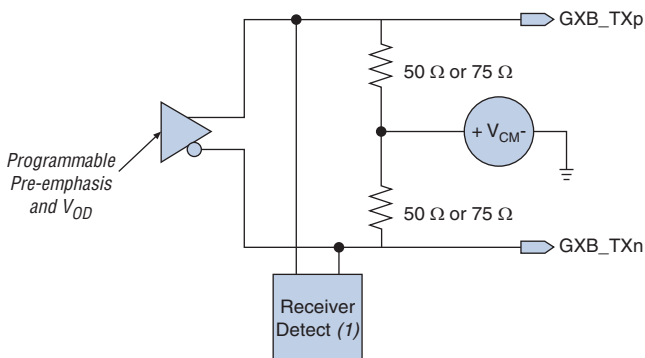
Signal	Description
<code>nCE</code>	On all Cyclone IV devices in the chain, <code>nCE</code> must be driven low by connecting it to GND, pulling it low through a resistor, or driving it by some control circuitry. For devices that are also in multi-device AS, AP, PS, or FPP configuration chains, you must connect the <code>nCE</code> pins to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
<code>nCEO</code>	On all Cyclone IV devices in the chain, <code>nCEO</code> is left floating or connected to the <code>nCE</code> of the next device.
<code>MSEL</code>	These pins must not be left floating. These pins support whichever non-JTAG configuration that you used in production. If you only use JTAG configuration, tie these pins to GND.
<code>nCONFIG</code>	Driven high by connecting to the <code>V<sub>CCIO</sub></code> supply of the bank in which the pin resides and pulling up through a resistor or driven high by some control circuitry.
<code>nSTATUS</code>	Pull to the <code>V<sub>CCIO</sub></code> supply of the bank in which the pin resides through a 10-k $\Omega$ resistor. When configuring multiple devices in the same JTAG chain, each <code>nSTATUS</code> pin must be pulled up to the <code>V<sub>CCIO</sub></code> individually.
<code>CONF_DONE</code>	Pull to the <code>V<sub>CCIO</sub></code> supply of the bank in which the pin resides through a 10-k $\Omega$ resistor. When configuring multiple devices in the same JTAG chain, each <code>CONF_DONE</code> pin must be pulled up to <code>V<sub>CCIO</sub></code> supply of the bank in which the pin resides individually. <code>CONF_DONE</code> going high at the end of JTAG configuration indicates successful configuration.
<code>DCLK</code>	Must not be left floating. Drive low or high, whichever is more convenient on your board.



## Transmitter Output Buffer

Figure 1-11 shows the transmitter output buffer block diagram.

**Figure 1-11. Transmitter Output Buffer Block Diagram**



**Note to Figure 1-11:**

- (1) Receiver detect function is specific for PCIe protocol implementation only. For more information, refer to “PCI Express (PIPE) Mode” on page 1-52.

The Cyclone IV GX transmitter output buffers support the **1.5-V PCML** I/O standard and are powered by `VCCH_GXB` power pins with 2.5-V supply. The 2.5-V supply on `VCCH_GXB` pins are regulated internally to 1.5-V for the transmitter output buffers. The transmitter output buffers support the following additional features:

- Programmable differential output voltage ( $V_{OD}$ )—customizes the  $V_{OD}$  up to 1200 mV to handle different trace lengths, various backplanes, and various receiver requirements.
- Programmable pre-emphasis—boosts high-frequency components in the transmitted signal to maximize the data eye opening at the far-end. The high-frequency components might be attenuated in the transmission media due to data-dependent jitter and intersymbol interference (ISI) effects. The requirement for pre-emphasis increases as the data rates through legacy backplanes increase.
- Programmable differential on-chip termination (OCT)—provides calibrated OCT at differential 100  $\Omega$  or 150  $\Omega$  with on-chip transmitter common mode voltage ( $V_{CM}$ ) at 0.65 V.  $V_{CM}$  is tri-stated when you disable the OCT to use external termination.



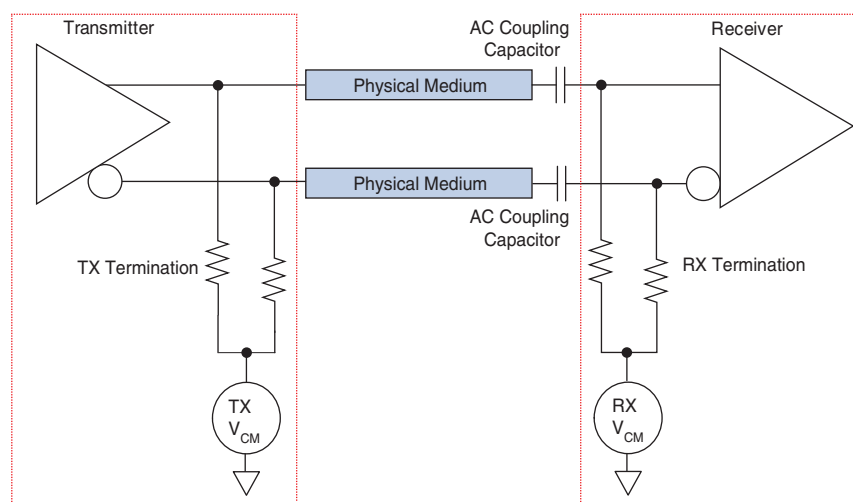
Disable OCT to use external termination if the link requires a 85  $\Omega$  termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.



The Cyclone IV GX transmitter output buffers are current-mode drivers. The resulting  $V_{OD}$  voltage is therefore a function of the transmitter termination value. For lists of supported  $V_{OD}$  settings, refer to the *Cyclone IV Device Data Sheet*.

The high-speed serial link can be AC- or DC-coupled, depending on the serial protocol implementation. In an AC-coupled link, the AC-coupling capacitor blocks the transmitter DC common mode voltage as shown in [Figure 1-12](#). Receiver OCT and on-chip biasing circuitry automatically restores the common mode voltage. The biasing circuitry is also enabled by enabling OCT. If you disable the OCT, then you must externally terminate and bias the receiver. AC-coupled links are required for PCIe, GbE, Serial RapidIO, SDI, XAUI, SATA, V-by-One and Display Port protocols.

**Figure 1-12. AC-Coupled Link with OCT**



**Table 1–27. Receiver Ports in ALTGX Megafunction for Cyclone IV GX (Part 1 of 3)**

Block	Port Name	Input/ Output	Clock Domain	Description
RX PCS	rx_syncstatus	Output	Synchronous to tx_clkout (non-bonded modes with rate match FIFO), rx_clkout (non-bonded modes without rate match FIFO), coreclkout (bonded modes), or rx_coreclk (when using the optional rx_coreclk input)	Word alignment synchronization status indicator. This signal passes through the RX Phase Compensation FIFO. ■ Not available in bit-slip mode
	rx_patterndetect	Output	Synchronous to tx_clkout (non-bonded modes with rate match FIFO), rx_clkout (non-bonded modes without rate match FIFO), coreclkout (bonded modes), or rx_coreclk (when using the optional rx_coreclk input)	Indicates when the word alignment logic detects the alignment pattern in the current word boundary. This signal passes through the RX Phase Compensation FIFO.
	rx_bitslip	Input	Asynchronous signal. Minimum pulse width is two parallel clock cycles.	Bit-slip control for the word aligner configured in bit-slip mode. ■ At every rising edge, word aligner slips one bit into the received data stream, effectively shifting the word boundary by one bit.
	rx_rlv	Output	Asynchronous signal. Driven for a minimum of two recovered clock cycles in configurations without byte serializer and a minimum of three recovered clock cycles in configurations with byte serializer.	Run-length violation indicator. ■ A high pulse indicates that the number of consecutive 1s or 0s in the received data stream exceeds the programmed run length violation threshold.
	rx_invpolarity	Input	Asynchronous signal. Minimum pulse width is two parallel clock cycles.	Generic receiver polarity inversion control. ■ A high level to invert the polarity of every bit of the 8- or 10-bit data to the word aligner.
	rx_enapatternalign	Input	Asynchronous signal.	Controls the word aligner operation configured in manual alignment mode.
	rx_rmfifoinserted	Output	Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes)	Rate match FIFO insertion status indicator. ■ A high level indicates the rate match pattern byte is inserted to compensate for the ppm difference in the reference clock frequencies between the upstream transmitter and the local receiver.
	rx_rmfiodeleted	Output	Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes)	Rate match FIFO deletion status indicator. ■ A high level indicates the rate match pattern byte is deleted to compensate for the ppm difference in the reference clock frequencies between the upstream transmitter and the local receiver.



Table 3-4 describes the tx\_datainfull[21..0] FPGA fabric-transceiver channel interface signals.

**Table 3-4. tx\_datainfull[21..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions <sup>(1)</sup>**

FPGA Fabric-Transceiver Channel Interface Description	Transmit Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)
8-bit FPGA fabric-Transceiver Channel Interface	tx_datainfull[7:0]: 8-bit data (tx_datain)
	<b>The following signals are used only in 8B/10B modes:</b>
	tx_datainfull[8]: Control bit (tx_ctrlenable)
	tx_datainfull[9] Transmitter force disparity Compliance (PCI Express [PIPE]) (tx_forcedisp) in all modes except PCI Express (PIPE) functional mode. For PCI Express (PIPE) functional mode, (tx_forcedispcompliance) is used.
	<ul style="list-style-type: none"> <li>For non-PIPE: tx_datainfull[10]: Forced disparity value (tx_dispval)</li> <li>For PCIe: tx_datainfull[10]: Forced electrical idle (tx_forceelectedle)</li> </ul>
10-bit FPGA fabric-Transceiver Channel Interface	tx_datainfull[9:0]: 10-bit data (tx_datain)
16-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 8/10 bits	Two 8-bit Data (tx_datain) tx_datainfull[7:0] - tx_datain (LSByte) and tx_datainfull[18:11] - tx_datain (MSByte)
	<b>The following signals are used only in 8B/10B modes:</b>
	tx_datainfull[8] - tx_ctrlenable (LSB) and tx_datainfull[19] - tx_ctrlenable (MSB)
	Force Disparity Enable <ul style="list-style-type: none"> <li>For non-PIPE: tx_datainfull[9] - tx_forcedisp (LSB) and tx_datainfull[20] - tx_forcedisp (MSB)</li> <li>For PCIe: tx_datainfull[9] - tx_forcedispcompliance and tx_datainfull[20] - 0</li> </ul>
	Force Disparity Value <ul style="list-style-type: none"> <li>For non-PIPE: tx_datainfull[10] - tx_dispval (LSB) and tx_datainfull[21] - tx_dispval (MSB)</li> <li>For PCIe: tx_datainfull[10] - tx_forceelectedle and tx_datainfull[21] - tx_forceelectedle</li> </ul>
20-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 10 bits	Two 10-bit Data (tx_datain) tx_datainfull[9:0] - tx_datain (LSByte) and tx_datainfull[20:11] - tx_datain (MSByte)

**Note to Table 3-4:**

(1) For all transceiver-related ports, refer to the “Transceiver Port Lists” section in the *Cyclone IV GX Transceiver Architecture* chapter.

### Clocking/Interface Options

The following describes the **Clocking/Interface** options available in Cyclone IV GX devices. The core clocking setup describes the transceiver core clocks that are the write and read clocks of the Transmit Phase Compensation FIFO and the Receive Phase Compensation FIFO, respectively. Core clocking is classified as transmitter core clocking and receiver core clocking.

**Table 3–6** lists the supported clocking interface settings for channel reconfiguration mode in Cyclone IV GX devices.

**Table 3–6. Dynamic Reconfiguration Clocking Interface Settings in Channel Reconfiguration Mode**

ALTGX Setting	Description
Dynamic Reconfiguration Channel Internal and Interface Settings	
How should the receivers be clocked?	Select one of the available options: <ul style="list-style-type: none"> <li>■ <b>Share a single transmitter core clock between receivers</b></li> <li>■ <b>Use the respective channel transmitter core clocks</b></li> <li>■ <b>Use the respective channel receiver core clocks</b></li> </ul>
How should the transmitters be clocked?	Select one of the available options: <ul style="list-style-type: none"> <li>■ <b>Share a single transmitter core clock between transmitters</b></li> <li>■ <b>Use the respective channel transmitter core clocks</b></li> </ul>

Transmitter core clocking refers to the clock that is used to write the parallel data from the FPGA fabric into the Transmit Phase Compensation FIFO. You can use one of the following clocks to write into the Transmit Phase Compensation FIFO:

- **tx\_coreclk**—you can use a clock of the same frequency as tx\_clkout from the FPGA fabric to provide the write clock to the Transmit Phase Compensation FIFO. If you use tx\_coreclk, it overrides the tx\_clkout options in the ALTGX MegaWizard Plug-In Manager.
- **tx\_clkout**—the Quartus II software automatically routes tx\_clkout to the FPGA fabric and back into the Transmit Phase Compensation FIFO.

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## Section I. Device Datasheet

### Chapter 1. Cyclone IV Device Datasheet

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Figure 1-2 shows the lock time parameters in manual mode.

 LTD = lock-to-data. LTR = lock-to-reference.

**Figure 1-2. Lock Time Parameters for Manual Mode**

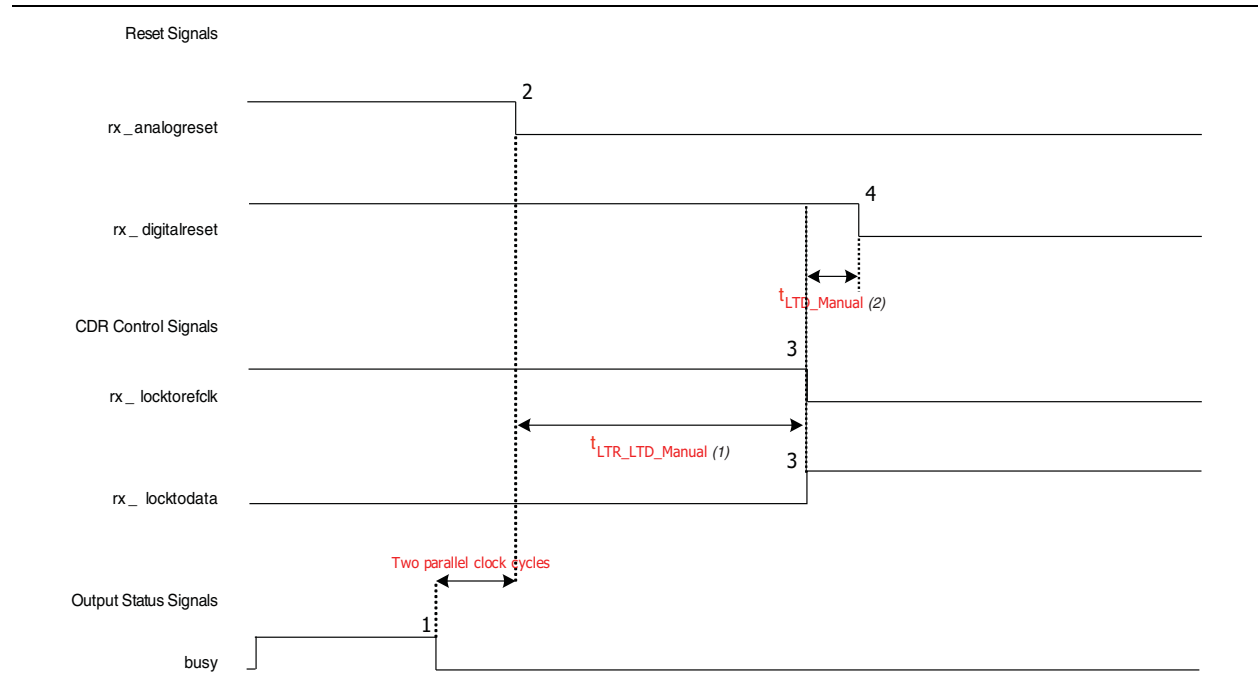
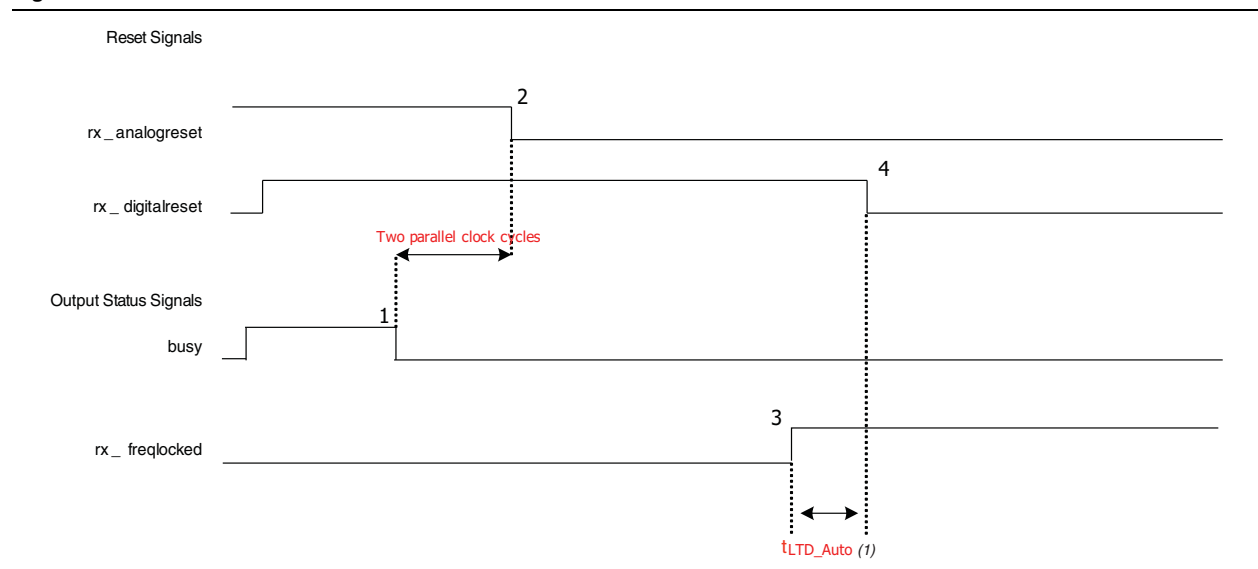


Figure 1-3 shows the lock time parameters in automatic mode.

**Figure 1-3. Lock Time Parameters for Automatic Mode**



## I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Excel-based I/O Timing spreadsheet is downloadable from [Cyclone IV Devices Literature](#) website.

## Glossary

Table 1-46 lists the glossary for this chapter.

**Table 1-46. Glossary (Part 1 of 5)**

Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	$f_{\text{HSCLK}}$	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through the PLL.
H	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate ( $\text{HSIODR} = 1/\text{TUI}$ ).
I	Input Waveforms for the SSTL Differential I/O Standard	