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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	343
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce15f23c7

In addition to the three general routing outputs, LEs in an LAB have register chain outputs, which allows registers in the same LAB to cascade together. The register chain output allows the LUTs to be used for combinational functions and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources.

LE Operating Modes

Cyclone IV LEs operate in the following modes:

- Normal mode
- Arithmetic mode

The Quartus® II software automatically chooses the appropriate mode for common functions, such as counters, adders, subtractors, and arithmetic functions, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions. You can also create special-purpose functions that specify which LE operating mode to use for optimal performance, if required.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (Figure 2–2). The Quartus II Compiler automatically selects the carry-in (`cin`) or the `data3` signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

Figure 2–2 shows LEs in normal mode.

Figure 2–2. Cyclone IV Device LEs in Normal Mode

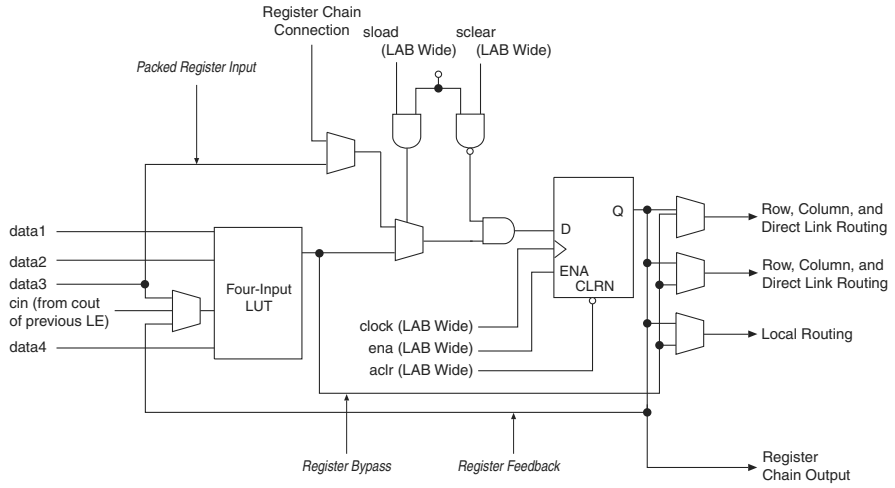
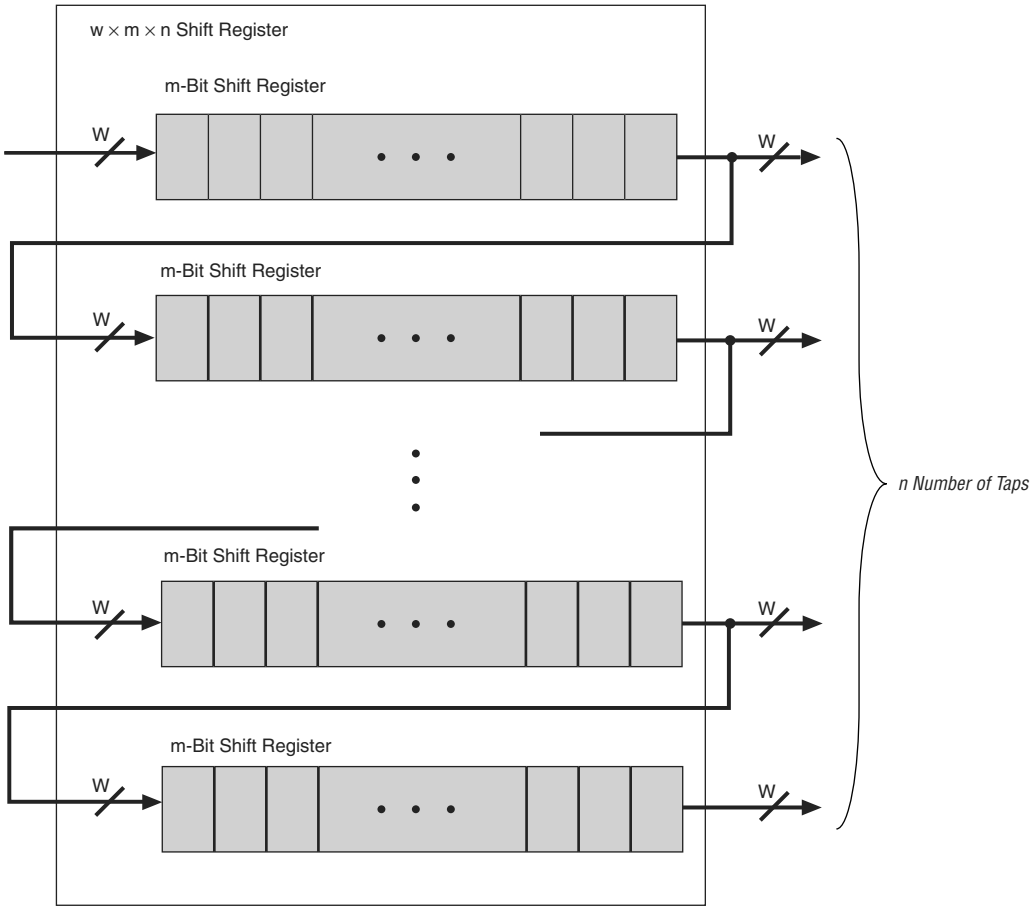


Figure 3–12 shows the Cyclone IV devices M9K memory block in shift register mode.

Figure 3–12. Cyclone IV Devices Shift Register Mode Configuration



ROM Mode

Cyclone IV devices M9K memory blocks support ROM mode. A **.mif** initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

Cyclone IV devices M9K memory blocks support single-clock or dual-clock FIFO buffers. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. Cyclone IV devices M9K memory blocks do not support simultaneous read and write from an empty FIFO buffer.

For more information about FIFO buffers, refer to the *Single- and Dual-Clock FIFO Megafunction User Guide*.

Table 4–2 lists the sign of the multiplication results for the various operand sign representations. The results of the multiplication are signed if any one of the operands is a signed value.

Table 4–2. Multiplier Sign Representation

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Unsigned	Low	Unsigned	Low	Unsigned
Unsigned	Low	Signed	High	Signed
Signed	High	Unsigned	Low	Signed
Signed	High	Signed	High	Signed

Each embedded multiplier block has only one `signa` and one `signb` signal to control the sign representation of the input data to the block. If the embedded multiplier block has two 9 × 9 multipliers, the `Data A` input of both multipliers share the same `signa` signal, and the `Data B` input of both multipliers share the same `signb` signal. You can dynamically change the `signa` and `signb` signals to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision, regardless of the sign representation.

☞ When the `signa` and `signb` signals are unused, the Quartus II software sets the multiplier to perform unsigned multiplication by default.

Output Registers

You can register the embedded multiplier output with output registers in either 18- or 36-bit sections, depending on the operational mode of the multiplier. The following control signals are available for each output register in the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers in a single embedded multiplier are fed by the same clock, clock enable, and asynchronous clear signals.

Operational Modes

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

☞ You can also use embedded multipliers of Cyclone IV devices to implement multiplier adder and multiplier accumulator functions, in which the multiplier portion of the function is implemented with embedded multipliers, and the adder or accumulator function is implemented in logic elements (LEs).

Table 5–2. GCLK Network Connections for EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 Devices (1), (2) (Part 2 of 4)

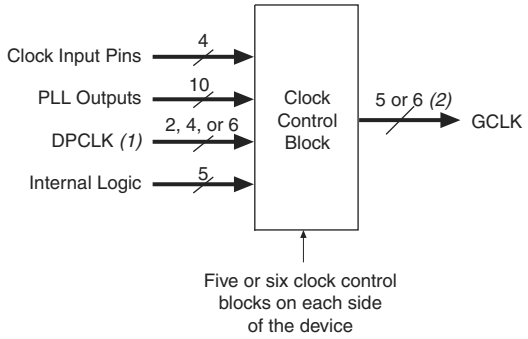
GCLK Network Clock Sources	GCLK Networks																													
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PLL_3_C0	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	✓	—	—	—	—	—	—	✓	—	—	✓	—	✓
PLL_3_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	✓	—	—	✓	—
PLL_3_C2	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—
PLL_3_C3	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—
PLL_3_C4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	✓	—	✓	✓
PLL_4_C0	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	✓	✓	—	—	✓	—	✓	—	—	—	—	—	—
PLL_4_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	✓	—	—	✓	—	—	—	—	—	—	—
PLL_4_C2	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—
PLL_4_C3	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—
PLL_4_C4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓	—	—	✓	—	✓	✓	—	—	—	—	—	—
PLL_5_C0	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C3	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C4	—	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C0	✓	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C4	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C0 (3)	—	—	—	—	—	—	✓	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C1 (3)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C2 (3)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C3 (3)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C4 (3)	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

From the clock sources listed above, only two clock input pins, two out of four PLL clock outputs (two clock outputs from either adjacent PLLs), one DPCLK pin, and one source from internal logic can drive into any given clock control block, as shown in Figure 5–1 on page 5–11.

Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs are dynamically selected to feed a GCLK. The clock control block supports static selection of the signal from internal logic.

Figure 5–5 shows a simplified version of the clock control blocks on each side of the Cyclone IV GX device periphery.

Figure 5–5. Clock Control Blocks on Each Side of Cyclone IV GX Device



Notes to Figure 5–5:

(1) The EP4CGX15 device has two DPCLK pins; the EP4CGX22 and EP4CGX30 devices have four DPCLK pins; the EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have six DPCLK pins.

(2) Each clock control block in the EP4CGX15, EP4CGX22, and EP4CGX30 devices can drive five GCLK networks. Each clock control block in the EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices can drive six GCLK networks.

The inputs to the five clock control blocks on each side of the Cyclone IV E device must be chosen from among the following clock sources:

- Three or four clock input pins, depending on the specific device
- Five PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins from both the top and bottom
- Five signals from internal logic

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control block, as shown in Figure 5–1 on page 5–11.

Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs are dynamically selected to feed a GCLK. The clock control block supports static selection of the signal from internal logic.

Document Revision History

Table 5–14 lists the revision history for this chapter.

Table 5–14. Document Revision History

Date	Version	Changes
October 2012	2.4	■ Updated “Manual Override” and “PLL Cascading” sections. ■ Updated Figure 5–9.
November 2011	2.3	■ Updated the “Dynamic Phase Shifting” section. ■ Updated Figure 5–26.
December 2010	2.2	■ Updated for the Quartus II software version 10.1 release. ■ Updated Figure 5–3 and Figure 5–10. ■ Updated “GCLK Network Clock Source Generation”, “PLLs in Cyclone IV Devices”, and “Manual Override” sections. ■ Minor text edits.
July 2010	2.1	■ Updated Figure 5–2, Figure 5–3, Figure 5–4, and Figure 5–10. ■ Updated Table 5–1, Table 5–2, and Table 5–5. ■ Updated “Clock Feedback Modes” section.
February 2010	2.0	■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release. ■ Updated “Clock Networks” section. ■ Updated Table 5–1 and Table 5–2. ■ Added Table 5–3. ■ Updated Figure 5–2, Figure 5–3, and Figure 5–9. ■ Added Figure 5–4 and Figure 5–10.
November 2009	1.0	Initial release.

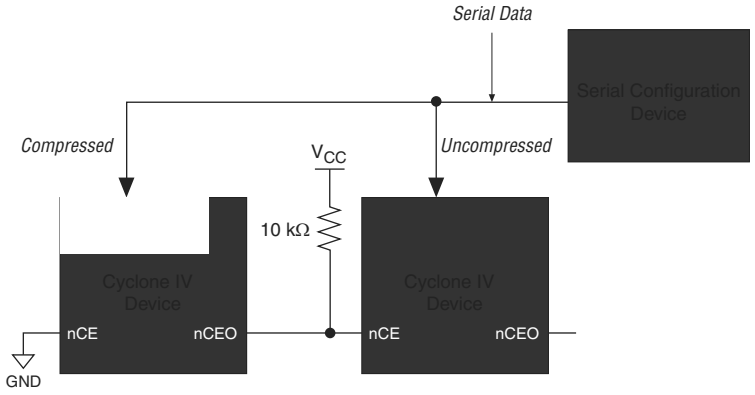
3. Click the **Configuration** tab.
4. Turn on **Generate compressed bitstreams**.
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

You can enable compression when creating programming files from the **Convert Programming Files** dialog box. To enable compression, perform the following steps:

1. On the File menu, click **Convert Programming Files**.
2. Under **Output programming file**, select your desired file type from the **Programming file type** list.
3. If you select **Programmer Object File (.pof)**, you must specify the configuration device in the **Configuration device** list.
4. Under **Input files to convert**, select **SOF Data**.
5. Click **Add File** to browse to the Cyclone IV device SRAM object files (**.sof)**.
6. In the **Convert Programming Files** dialog box, select the **.pof** you added to **SOF Data** and click **Properties**.
7. In the **SOF File Properties** dialog box, turn on the **Compression** option.

When multiple Cyclone IV devices are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 8–1 shows a chain of two Cyclone IV devices. The first device has compression enabled and receives compressed bitstream from the configuration device. The second device has the compression feature disabled and receives uncompressed data. You can generate programming files for this setup in the **Convert Programming Files** dialog box.

Figure 8–1. Compressed and Uncompressed Configuration Data in the Same Configuration File



Configuration Requirement

This section describes Cyclone IV device configuration requirement and includes the following topics:

- "Power-On Reset (POR) Circuit" on page 8–4
- "Configuration File Size" on page 8–4
- "Power Up" on page 8–6

FPP Configuration

The FPP configuration in Cyclone IV devices is designed to meet the increasing demand for faster configuration time. Cyclone IV devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

You can perform FPP configuration of Cyclone IV devices with an intelligent host, such as a MAX II device or microprocessor with flash memory. If your system already contains a CFI flash memory, you can use it for the Cyclone IV device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone IV device.

For more information about the PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

FPP configuration is supported in EP4CGX30 (only for F484 package), EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150, and all Cyclone IV E devices.

The FPP configuration is not supported in E144 package of Cyclone IV E devices.

Cyclone IV devices do not support enhanced configuration devices for FPP configuration.

FPP Configuration Using an External Host

FPP configuration using an external host provides a fast method to configure Cyclone IV devices. In the FPP configuration scheme, you can use an external host device to control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone IV device. You can store configuration data in an **.rbf**, **.hex**, or **.ttf** format. When using the external host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to

Device Configuration Pins

Table 8–18 through Table 8–21 describe the connections and functionality of all the configuration related pins on Cyclone IV devices. Table 8–18 and Table 8–19 list the device pin configuration for the Cyclone IV GX and Cyclone IV E, respectively.

Table 8–18. Configuration Pin Summary for Cyclone IV GX Devices

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
8	Data[4:2]	Input	—	V_{CCIO}	FPP
3	Data[7:5]	Input	—	V_{CCIO}	FPP
9	nCSO (2)	Output	—	V_{CCIO}	AS
3	CRC_ERROR	Output	—	V_{CCIO}/Pull-up (1)	Optional, all modes
9	DATA[0] (2)	Input	Yes	V_{CCIO}	PS, FPP, AS
9	DATA[1]/ASDO (2)	Input	—	V_{CCIO}	FPP
		Output		V_{CCIO}	AS
3	INIT_DONE	Output	—	Pull-up	Optional, all modes
3	nSTATUS	Bidirectional	Yes	Pull-up	All modes
9	nCE	Input	Yes	V_{CCIO}	All modes
9	DCLK (2)	Input	Yes	V_{CCIO}	PS, FPP
		Output		V_{CCIO}	AS
3	CONF_DONE	Bidirectional	Yes	Pull-up	All modes
9	TDI	Input	Yes	V_{CCIO}	JTAG
9	TMS	Input	Yes	V_{CCIO}	JTAG
9	TCK	Input	Yes	V_{CCIO}	JTAG
9	nCONFIG	Input	Yes	V_{CCIO}	All modes
8	CLKUSR	Input	—	V_{CCIO}	Optional
3	nCEO	Output	—	V_{CCIO}	Optional, all modes
3	MSEL	Input	Yes	V_{CCINT}	All modes
9	TDO	Output	Yes	V_{CCIO}	JTAG
6	DEV_OE	Input	—	V_{CCIO}	Optional
6	DEV_CLRn	Input	—	V_{CCIO}	Optional

Notes to Table 8–18:

(1) The CRC_ERROR pin is a dedicated open-drain output or an optional user I/O pin. Active high signal indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled in the Quartus II software from the **Error Detection CRC** tab of the **Device and Pin Options** dialog box. When using this pin, connect it to an external 10-kΩ pull-up resistor to an acceptable voltage that satisfies the input voltage of the receiving device.

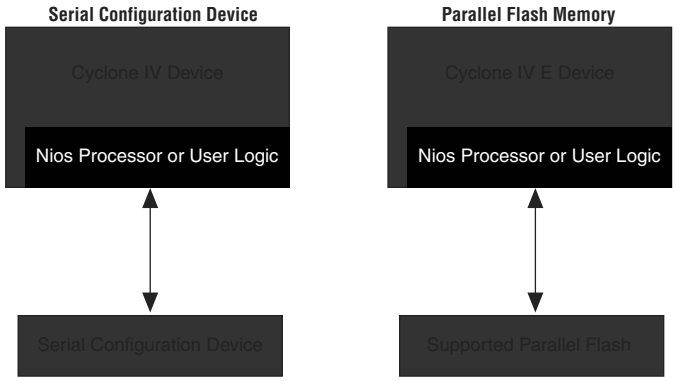
(2) To tri-state AS configuration pins in the AS configuration scheme, turn on the **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box. This tri-states DCLK, nCSO, Data[0], and Data[1]/ASDO pins. Dual-purpose pins settings for these pins are ignored. To set these pins to different settings, turn off the **Enable input tri-state on active configuration pins in user mode** option and set the desired setting from the Dual-purpose Pins Setting menu.

Table 8–19. Configuration Pin Summary for Cyclone IV E Devices (Part 1 of 3)

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
1	nCSO (1) FLASH_nCE (2)	Output	—	V_{CCIO}	AS, AP
6	CRC_ERROR (3)	Output	—	V_{CCIO}/Pull-up (4)	Optional, all modes

Figure 8–31 shows the block diagrams to implement remote system upgrade in Cyclone IV devices.

Figure 8–31. Remote System Upgrade Block Diagrams for AS and AP Configuration Schemes



The MSEL pin setting in the remote system upgrade mode is the same as the standard configuration mode. Standard configuration mode refers to normal Cyclone IV device configuration mode with no support for remote system upgrades (the remote system upgrade circuitry is disabled). When using remote system upgrade in Cyclone IV devices, you must enable the remote update mode option setting in the Quartus II software.

Enabling Remote Update

You can enable or disable remote update for Cyclone IV devices in the Quartus II software before design compilation (in the Compiler Settings menu). To enable remote update in the compiler settings of the project, perform the following steps:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.
3. Click the **Configuration** tab.
4. From the **Configuration Mode** list, select **Remote**.
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

Configuration Image Types

When using remote system upgrade, Cyclone IV device configuration bitstreams are classified as factory configuration images or application configuration images. An image, also referred to as a configuration, is a design loaded into the device that performs certain user-defined functions. Each device in your system requires one factory image or with addition of one or more application images. The factory image is a user-defined fall-back or safe configuration and is responsible for administering remote updates with the dedicated circuitry. Application images implement user-defined functionality in the target Cyclone IV device. You can include the default application image functionality in the factory image.

Table 9–7 lists the input and output ports that you must include in the atom.

Table 9–7. CRC Block Input and Output Ports

Port	Input/Output	Definition
<crcblock_name>	Input	Unique identifier for the CRC block, and represents any identifier name that is legal for the given description language (for example, Verilog HDL, VHDL, and AHDL). This field is required.
.clk(*<clock source>*	Input	This signal designates the clock input of this cell. All operations of this cell are with respect to the rising edge of the clock. Whether it is the loading of the data into the cell or data out of the cell, it always occurs on the rising edge. This port is required.
.shiftnld (*<shiftnld source>*)	Input	This signal is an input into the error detection block. If `shiftnld=1`, the data is shifted from the internal shift register to the `regout` at each rising edge of `clk`. If `shiftnld=0`, the shift register parallel loads either the pre-calculated CRC value or the update register contents, depending on the `ldsrc` port input. To do this, the `shiftnld` must be driven low for at least two clock cycles. This port is required.
.ldsrc (*<ldsrc source>*)	Input	This signal is an input into the error detection block. If `ldsrc=0`, the pre-computed CRC register is selected for loading into the 32-bit shift register at the rising edge of `clk` when `shiftnld=0`. If `ldsrc=1`, the signature register (result of the CRC calculation) is selected for loading into the shift register at the rising edge of `clk` when `shiftnld=0`. This port is ignored when `shiftnld=1`. This port is required.
.crcerror (*<crcerror indicator output>*)	Output	This signal is the output of the cell that is synchronized to the internal oscillator of the device (80-MHz internal oscillator) and not to the `clk` port. It asserts high if the error block detects that a SRAM bit has flipped and the internal CRC computation has shown a difference with respect to the pre-computed value. You must connect this signal either to an output pin or a bidirectional pin. If it is connected to an output pin, you can only monitor the CRC_ERROR pin (the core cannot access this output). If the CRC_ERROR signal is used by core logic to read error detection logic, you must connect this signal to a `BIDIR` pin. The signal is fed to the core indirectly by feeding a `BIDIR` pin that has its output enable port connected to V_{CC} (see Figure 9–3 on page 9–8).
.regout (*<registered output>*)	Output	This signal is the output of the error detection shift register synchronized to the `clk` port to be read by core logic. It shifts one bit at each cycle, so you should clock the `clk` signal 31 cycles to read out the 32 bits of the shift register.

Recovering from CRC Errors

The system that the Altera FPGA resides in must control device reconfiguration. After detecting an error on the CRC_ERROR pin, strobing the nCONFIG low directs the system to perform the reconfiguration at a time when it is safe for the system to reconfigure the FPGA.

When the data bit is rewritten with the correct value by reconfiguring the device, the device functions correctly.

While soft errors are uncommon in Altera devices, certain high-reliability applications might require a design to account for these errors.

After updating the word boundary, word aligner status signals (rx_syncstatus and rx_patterndetect) are driven high for one parallel clock cycle synchronous to the most significant byte of the word alignment pattern. The rx_syncstatus and rx_patterndetect signals have the same latency as the datapath and are forwarded to the FPGA fabric to indicate the word aligner status. Any word alignment pattern received thereafter in the same word boundary causes only the rx_patterndetect signal to go high for one clock cycle.

Figure 1–17 shows the manual alignment mode word aligner operation in 10-bit data width mode. In this example, a /K28.5/ (10'b0101111100) is specified as the word alignment pattern.

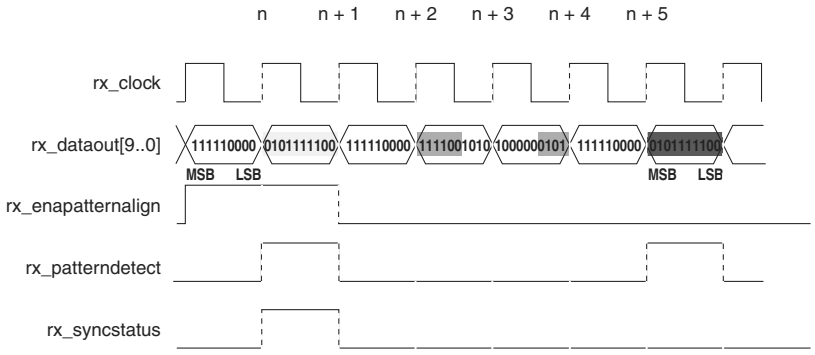
The word aligner aligns to the /K28.5/ alignment pattern (red) in cycle *n* because the rx_enapatternalign signal is asserted high. The rx_syncstatus signal goes high for one clock cycle indicating alignment to a new word boundary. The rx_patterndetect signal also goes high for one clock cycle to indicate initial word alignment.

At time *n* + 1, the rx_enapatternalign signal is deasserted to instruct the word aligner to lock the current word boundary.

The alignment pattern is detected again (green) in a new word boundary across cycles *n* + 2 and *n* + 3. The word aligner does not align to this new word boundary because the rx_enapatternalign signal is held low.

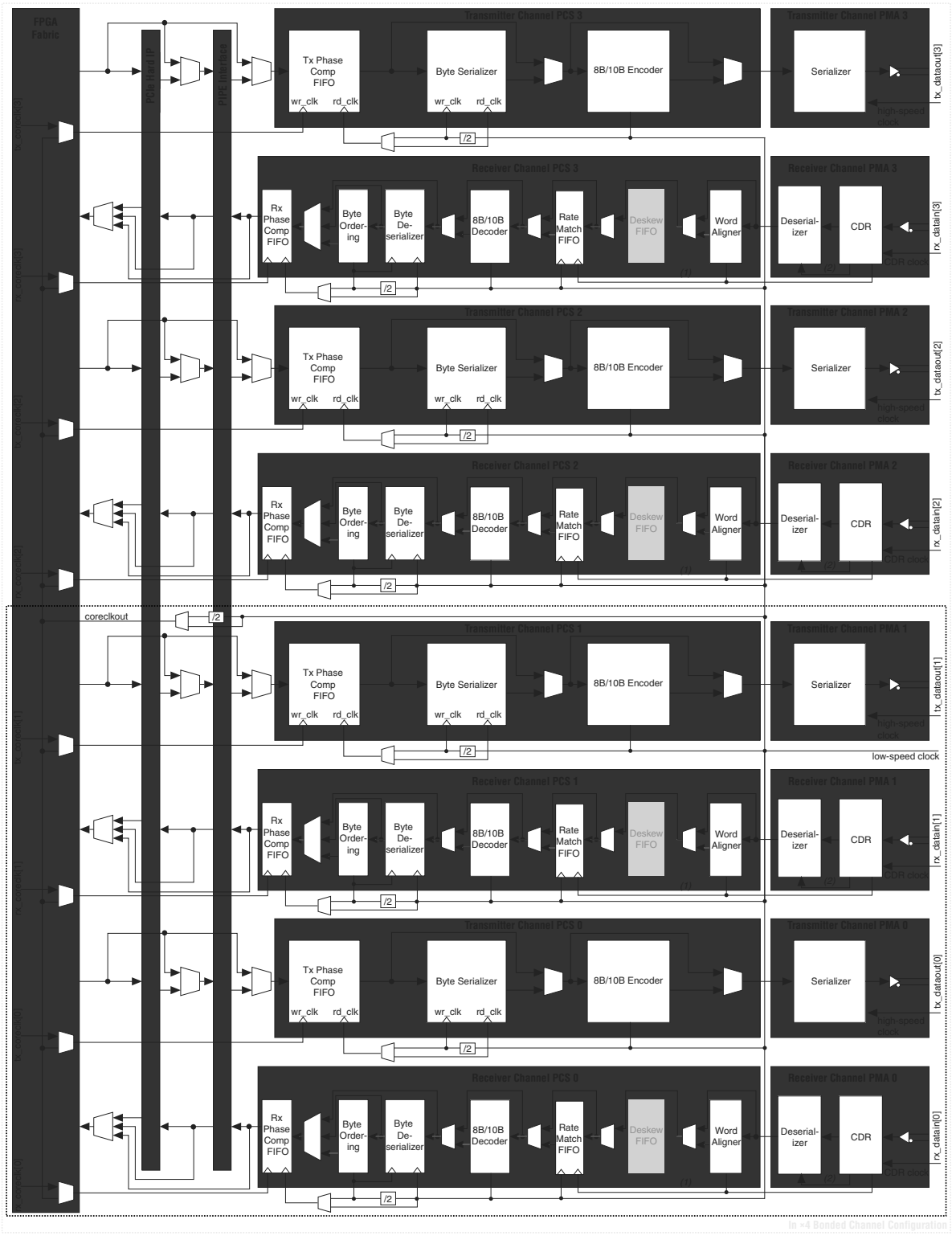
The /K28.5/ word alignment pattern is detected again (blue) in the current word boundary during cycle *n* + 5 causing the rx_patterndetect signal to go high for one parallel clock cycle.

Figure 1–17. Word Aligner in 10-bit Manual Alignment Mode



If the word alignment pattern is known to be unique and does not appear between word boundaries, you can hold the rx_enapatternalign signal constantly high because there is no possibility of false word alignment. If there is a possibility of the word alignment pattern occurring across word boundaries, you must control the rx_enapatternalign signal to lock the word boundary after the desired word alignment is achieved to avoid re-alignment to an incorrect word boundary.

Figure 1–39. Transmitter and Receiver Datapath Clocking with Rate Match FIFO in Bonded Channel Configuration



Notes to Figure 1–39:

(1) Low-speed recovered clock.

(2) High-speed recovered clock.

Clock Rate Compensation

In XAUI mode, the rate match FIFO compensates up to ±100 ppm (200 ppm total) difference between the upstream transmitter and the local receiver reference clock. The XAUI protocol requires the transmitter to send /R/ (/K28.0/) code groups simultaneously on all four lanes (denoted as ||R|| column) during inter-packet gaps, adhering to rules listed in the IEEE P802.3ae specification.

The rate match operation begins after `rx_syncstatus` and `rx_channelaligned` are asserted. The `rx_syncstatus` signal is from the word aligner, indicating that synchronization is acquired on all four channels, while `rx_channelaligned` signal is from the deskew FIFO, indicating channel alignment.

The rate match FIFO looks for the ||R|| column (simultaneous /R/ code groups on all four channels) and deletes or inserts ||R|| columns to prevent the rate match FIFO from overflowing or under running. The rate match FIFO can insert or delete as many ||R|| columns as necessary to perform the rate match operation.

The `rx_rmfifodatadeleted` and `rx_rmfifodatainserted` flags that indicate rate match FIFO deletion and insertion events, respectively, are forwarded to the FPGA fabric. If an ||R|| column is deleted, the `rx_rmfifodeleted` flag from each of the four channels goes high for one clock cycle per deleted ||R|| column. If an ||R|| column is inserted, the `rx_rmfifoinserted` flag from each of the four channels goes high for one clock cycle per inserted ||R|| column.

☞ The rate match FIFO does not insert or delete code groups automatically to overcome FIFO empty or full conditions. In this case, the rate match FIFO asserts the `rx_rmfifofull` and `rx_rmfifoempty` flags for at least three recovered clock cycles to indicate rate match FIFO full and empty conditions, respectively. You must then assert the `rx_digitalreset` signal to reset the receiver PCS blocks.

Deterministic Latency Mode

Deterministic Latency mode provides the transceiver configuration that allows no latency uncertainty in the datapath and features to strictly control latency variation. This mode supports non-bonded (×1) and bonded (×4) channel configurations, and is typically used to support CPRI and OBSAI protocols that require accurate delay measurements along the datapath. The Cyclone IV GX transceivers configured in Deterministic Latency mode provides the following features:

- registered mode phase compensation FIFO
- receive bit-slip indication
- transmit bit-slip control
- PLL PFD feedback

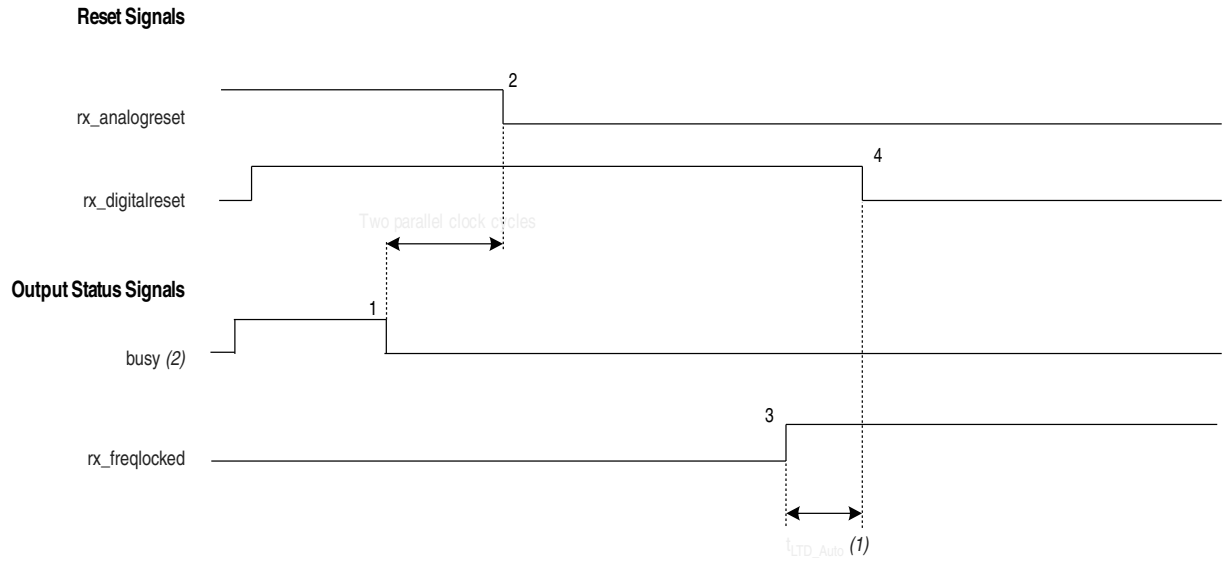
Transmitter Only Channel

This configuration contains only a transmitter channel. If you create a **Transmitter Only** instance in the ALTGX MegaWizard Plug-In Manager, use the same reset sequence shown in Figure 2–3 on page 2–7.

Receiver Only Channel—Receiver CDR in Automatic Lock Mode

This configuration contains only a receiver channel. If you create a **Receiver Only** instance in the ALTGX MegaWizard Plug-In Manager with the receiver CDR in automatic lock mode, use the reset sequence shown in Figure 2–6.

Figure 2–6. Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Automatic Lock Mode



Notes to Figure 2–6:

(1) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.

(2) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

As shown in Figure 2–6, perform the following reset procedure for the receiver in CDR automatic lock mode:

1. After power up, wait for the `busy` signal to be deasserted.
2. Keep the `rx_digitalreset` and `rx_analogreset` signals asserted during this time period.
3. After the busy signal is deasserted, wait for another two parallel clock cycles, then deassert the `rx_analogreset` signal.
4. Wait for the `rx_freqlocked` signal to go high.
5. When `rx_freqlocked` goes high (marker 3), from that point onwards, wait for at least t_{LTD_Auto}, then de-assert the `rx_digitalreset` signal (marker 4). At this point, the receiver is ready to receive data.

If you are reconfiguring the multipurpose PLL with a different M counter value, follow these steps:

1. During transceiver PLL reconfiguration, assert `tx_digitalreset`, `rx_digitalreset`, and `rx_analogreset` signals.
2. Perform PLL reconfiguration to update the multipurpose PLL with the PLL **.mif** files.
3. Perform channel reconfiguration and update the transceiver with the GXB reconfiguration **.mif** files. If you have multiple channel instantiations connected to the same multipurpose PLL, reconfigure each channel.
4. Deassert `tx_digitalreset` and `rx_analogreset` signals.
5. After the `rx_freqlocked` signal goes high, wait for at least 4 µs, and then deassert the `rx_digitalreset` signal.

Error Indication During Dynamic Reconfiguration

The ALTGX_RECONFIG MegaWizard Plug-In Manager provides an error status signal when you select the **Enable illegal mode checking** option or the **Enable self recovery** option in the **Error checks/data rate switch** screen. The conditions under which the error signal is asserted are:

- **Enable illegal mode checking option**—when you select this option, the dynamic reconfiguration controller checks whether an attempted operation falls under one of the conditions listed below. The dynamic reconfiguration controller detects these conditions within two `reconfig_clk` cycles, deasserts the `busy` signal, and asserts the error signal for two `reconfig_clk` cycles.
  - PMA controls, read operation—none of the output ports (`rx_eqctrl_out`, `rx_eqdcgain_out`, `tx_vodctrl_out`, and `tx_preemp_out`) are selected in the ALTGX_RECONFIG instance and the `read` signal is asserted.
  - PMA controls, write operation—none of the input ports (`rx_eqctrl`, `rx_eqdcgain`, `tx_vodctrl`, and `tx_preemp`) are selected in the ALTGX_RECONFIG instance and the `write_all` signal is asserted.
- **Channel reconfiguration** and **PMA reconfiguration mode** select - read operation option:
  - The `reconfig_mode_sel` input port is set to **3'b001** (Channel reconfiguration mode)
  - The `read` signal is asserted
- **Enable self recovery** option—when you select this option, the ALTGX_RECONFIG MegaWizard Plug-In Manager provides the error output port. The dynamic reconfiguration controller quits an operation if it did not complete within the expected number of clock cycles. After recovering from the illegal operation, the dynamic reconfiguration controller deasserts the `busy` signal and asserts the error output port for two `reconfig_clk` cycles.

☞ The error signal is not asserted when an illegal value is written to any of the PMA controls.

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The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1–10 and Equation 1–1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1–10 lists the change percentage of the OCT resistance with voltage and temperature.

Table 1–10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices *(1)*

Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	–0.026
2.5	0.234	–0.039
1.8	0.219	–0.086
1.5	0.199	–0.136
1.2	0.161	–0.288

Note to Table 1–10:

(1) This specification is not applicable to EP4CGX15, EP4CGX22, and EP4CGX30 devices.

Equation 1–1. Final OCT Resistance *(1), (2), (3), (4), (5), (6)*

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV \quad (7)$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \quad (8)$$

$$\text{For } \Delta R_x < 0;\ MF_x = 1/ (|\Delta R_x|/100 + 1) \quad (9)$$

$$\text{For } \Delta R_x > 0;\ MF_x = \Delta R_x/100 + 1 \quad (10)$$

$$MF = MF_V \times MF_T \quad (11)$$

$$R_{final} = R_{initial} \times MF \quad (12)$$

Notes to Equation 1–1:

(1) T_2 is the final temperature.
(2) T_1 is the initial temperature.
(3) MF is multiplication factor.
(4) R_{final} is final resistance.
(5) $R_{initial}$ is initial resistance.
(6) Subscript $_x$ refers to both $_V$ and $_T$.
(7) ΔR_V is a variation of resistance with voltage.
(8) ΔR_T is a variation of resistance with temperature.
(9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
(10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
(11) V_2 is final voltage.
(12) V_1 is the initial voltage.

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

Glossary

Table 1–46 lists the glossary for this chapter.

Table 1–46. Glossary (Part 1 of 5)

Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through the PLL.
H	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard