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Details

Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	343
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce15f23c7n

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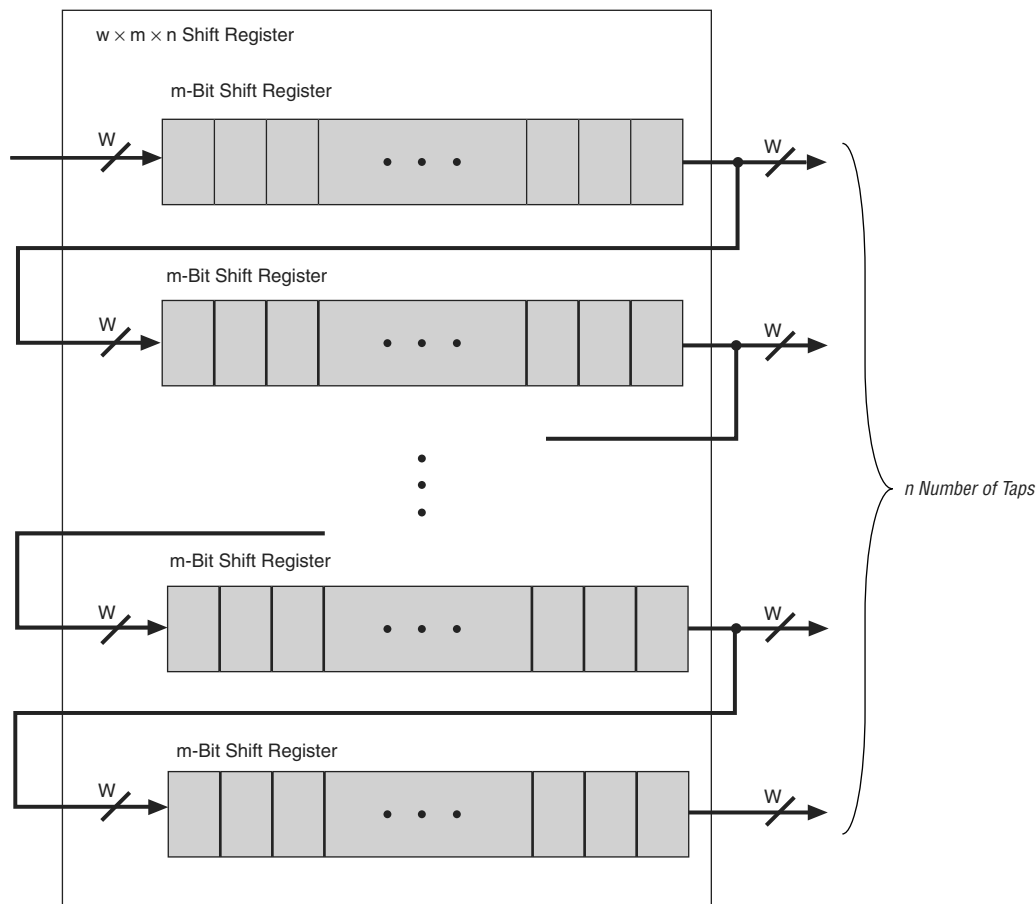
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- Cyclone IV GX devices offer up to eight high-speed transceivers that provide:
 - Data rates up to 3.125 Gbps
 - 8B/10B encoder/decoder
 - 8-bit or 10-bit physical media attachment (PMA) to physical coding sublayer (PCS) interface
 - Byte serializer/deserializer (SERDES)
 - Word aligner
 - Rate matching FIFO
 - TX bit slipper for Common Public Radio Interface (CPRI)
 - Electrical idle
 - Dynamic channel reconfiguration allowing you to change data rates and protocols on-the-fly
 - Static equalization and pre-emphasis for superior signal integrity
 - 150 mW per channel power consumption
 - Flexible clocking structure to support multiple protocols in a single transceiver block
- Cyclone IV GX devices offer dedicated hard IP for PCI Express (PIPE) (PCIe) Gen 1:
 - ×1, ×2, and ×4 lane configurations
 - End-point and root-port configurations
 - Up to 256-byte payload
 - One virtual channel
 - 2 KB retry buffer
 - 4 KB receiver (Rx) buffer
- Cyclone IV GX devices offer a wide range of protocol support:
 - PCIe (PIPE) Gen 1 ×1, ×2, and ×4 (2.5 Gbps)
 - Gigabit Ethernet (1.25 Gbps)
 - CPRI (up to 3.072 Gbps)
 - XAUI (3.125 Gbps)
 - Triple rate serial digital interface (SDI) (up to 2.97 Gbps)
 - Serial RapidIO (3.125 Gbps)
 - Basic mode (up to 3.125 Gbps)
 - V-by-One (up to 3.0 Gbps)
 - DisplayPort (2.7 Gbps)
 - Serial Advanced Technology Attachment (SATA) (up to 3.0 Gbps)
 - OBSAI (up to 3.072 Gbps)

Figure 3-12 shows the Cyclone IV devices M9K memory block in shift register mode.

Figure 3-12. Cyclone IV Devices Shift Register Mode Configuration



ROM Mode

Cyclone IV devices M9K memory blocks support ROM mode. A `.mif` initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

Cyclone IV devices M9K memory blocks support single-clock or dual-clock FIFO buffers. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. Cyclone IV devices M9K memory blocks do not support simultaneous read and write from an empty FIFO buffer.



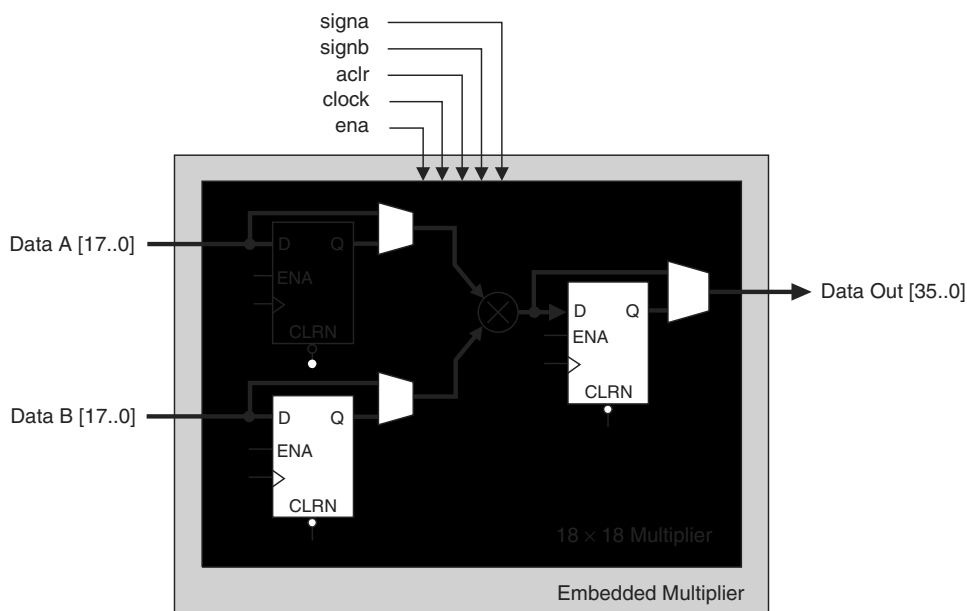
For more information about FIFO buffers, refer to the *Single- and Dual-Clock FIFO Megafunction User Guide*.

18-Bit Multipliers

You can configure each embedded multiplier to support a single 18×18 multiplier for input widths of 10 to 18 bits.

Figure 4-3 shows the embedded multiplier configured to support an 18-bit multiplier.

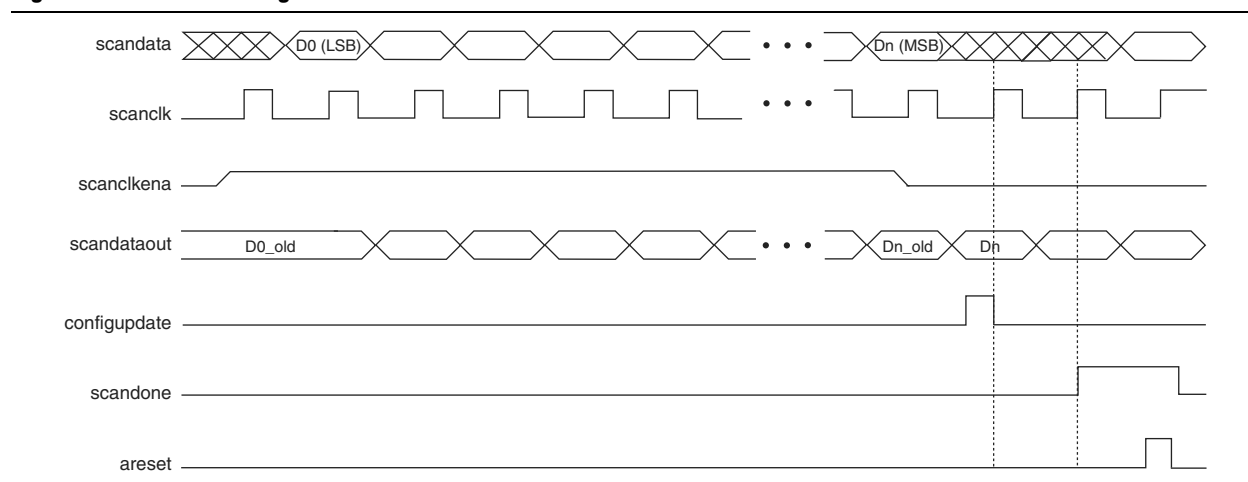
Figure 4-3. 18-Bit Multiplier Mode



All 18-bit multiplier inputs and results are independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Also, you can dynamically change the *signa* and *signb* signals and send these signals through dedicated input registers.

Figure 5–23 shows a functional simulation of the PLL reconfiguration feature.

Figure 5–23. PLL Reconfiguration Scan Chain



When reconfiguring the counter clock frequency, the corresponding counter phase shift settings cannot be reconfigured using the same interface. You can reconfigure phase shifts in real time using the dynamic phase shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase shift setting (for example, 90°) on the clock output, you must reconfigure the phase shift after reconfiguring the counter clock frequency.

Post-Scale Counters (C0 to C4)

You can configure multiply or divide values and duty cycle of post-scale counters in real time. Each counter has an 8-bit high time setting and an 8-bit low time setting. The duty cycle is the ratio of output high or low time to the total cycle time, that is the sum of the two. Additionally, these counters have two control bits, *rbypass*, for bypassing the counter, and *rse1odd*, to select the output clock duty cycle.

When the *rbypass* bit is set to 1, it bypasses the counter, resulting in a divide by one. When this bit is set to 0, the PLL computes the effective division of the VCO output frequency based on the high and low time counters. For example, if the post-scale divide factor is 10, the high and low count values are set to 5 and 5, to achieve a 50–50% duty cycle. The PLL implements this duty cycle by transitioning the output clock from high-to-low on the rising edge of the VCO output clock. However, a 4 and 6 setting for the high and low count values, respectively, would produce an output clock with a 40–60% duty cycle.

The *rse1odd* bit indicates an odd divide factor for the VCO output frequency with a 50% duty cycle. For example, if the post-scale divide factor is three, the high and low time count values are 2 and 1, respectively, to achieve this division. This implies a 67%–33% duty cycle. If you need a 50%–50% duty cycle, you must set the *rse1odd* control bit to 1 to achieve this duty cycle despite an odd division factor. The PLL implements this duty cycle by transitioning the output clock from high-to-low on a falling edge of the VCO output clock. When you set *rse1odd* = 1, subtract 0.5 cycles from the high time and add 0.5 cycles to the low time.

For example:

- High time count = 2 cycles

implements either a high-speed deserializer receiver or a high-speed serializer transmitter. There is a list of parameters in the ALTLVDS megafunction that you can set to customize your SERDES based on your design requirements. The megafunction is optimized to use Cyclone IV devices resources to create high-speed I/O interfaces in the most effective manner.



When you use Cyclone IV devices with the ALTLVDS megafunction, the interface always sends the MSB of your parallel data first.



For more details about designing your high-speed I/O systems interfaces using the ALTLVDS megafunction, refer to the *ALTLVDS Megafunction User Guide* and the *Quartus II Handbook*.

Document Revision History

Table 6-12 lists the revision history for this chapter.

Table 6-12. Document Revision History (Part 1 of 2)

Date	Version	Changes
March 2016	2.7	<ul style="list-style-type: none"> ■ Updated Table 6-5 and Table 6-9 to remove support for the N148 package.
May 2013	2.6	<ul style="list-style-type: none"> ■ Updated Table 6-2 by adding Note (9). ■ Updated Table 6-4 and Table 6-8 to add new device options and packages.
February 2013	2.5	Updated Table 6-4 and Table 6-8 to add new device options and packages.
October 2012	2.4	<ul style="list-style-type: none"> ■ Updated “I/O Banks” and “High Speed Serial Interface (HSSI) Input Reference Clock Support” sections. ■ Updated Table 6-3 and Table 6-5. ■ Updated Figure 6-10.
November 2011	2.3	<ul style="list-style-type: none"> ■ Updated “Differential SSTL I/O Standard Support in Cyclone IV Devices” and “Differential HSTL I/O Standard Support in Cyclone IV Devices” sections. ■ Updated Table 6-1, Table 6-8, and Table 6-9. ■ Updated Figure 6-1.
December 2010	2.2	<ul style="list-style-type: none"> ■ Updated for the Quartus II software version 10.1 release. ■ Added Cyclone IV E new device package information. ■ Added “Clock Pins Functionality” section. ■ Updated Table 6-4 and Table 6-8. ■ Minor text edits.
July 2010	2.1	<ul style="list-style-type: none"> ■ Updated “Cyclone IV I/O Elements”, “Programmable Pull-Up Resistor”, “I/O Banks”, “High-Speed I/O Interface”, and “Designing with BLVDS” sections. ■ Updated Table 6-6 and Table 6-7. ■ Updated Figure 6-19.

7. External Memory Interfaces in Cyclone IV Devices

CYIV-51007-2.6

This chapter describes the memory interface pin support and the external memory interface features of Cyclone® IV devices.

In addition to an abundant supply of on-chip memory, Cyclone IV devices can easily interface with a broad range of external memory devices, including DDR2 SDRAM, DDR SDRAM, and QDR II SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.



Altera recommends that you construct all DDR2 or DDR SDRAM external memory interfaces using the Altera® ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2 or DDR SDRAM memory controllers, third-party controllers, or a custom controller for unique application needs. Cyclone IV devices support QDR II interfaces electrically, but Altera does not supply controller or physical layer (PHY) megafunctions for QDR II interfaces.

This chapter includes the following sections:

- “Cyclone IV Devices Memory Interfaces Pin Support” on page 7-2
- “Cyclone IV Devices Memory Interfaces Features” on page 7-12



For more information about supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to the *External Memory Interface Handbook*.

During device configuration, Cyclone IV E devices read configuration data using the parallel interface and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where an external host controls the interface.

AP Configuration Supported Flash Memories

The AP configuration controller in Cyclone IV E devices is designed to interface with two industry-standard flash families—the Micron P30 Parallel NOR flash family and the Micron P33 Parallel NOR flash family. Unlike serial configuration devices, both of the flash families supported in AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash after entering user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Micron P30 flash family and the P33 flash family support a continuous synchronous burst read mode at 40 MHz DCLK frequency for reading data from the flash. Additionally, the Micron P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.



Cyclone IV E devices use a 40-MHz oscillator for the AP configuration scheme. The oscillator is the same oscillator used in the Cyclone IV E AS configuration scheme.

Table 8–10 lists the supported families of the commodity parallel flash for the AP configuration scheme.

Table 8–10. Supported Commodity Flash for AP Configuration Scheme for Cyclone IV E Devices ⁽¹⁾

Flash Memory Density	Micron P30 Flash Family ⁽²⁾	Micron P33 Flash Family ⁽³⁾
64 Mbit	✓	✓
128 Mbit	✓	✓
256 Mbit	✓	✓

Notes to Table 8–10:

- (1) The AP configuration scheme only supports flash memory speed grades of 40 MHz and above.
- (2) 3.3-, 3.0-, 2.5-, and 1.8-V I/O options are supported for the Micron P30 flash family.
- (3) 3.3-, 3.0- and 2.5-V I/O options are supported for the Micron P33 flash family.

Configuring Cyclone IV E devices from the Micron P30 and P33 family 512-Mbit flash memory is possible, but you must properly drive the extra address and FLASH_nCE pins as required by these flash memories.



To check for supported speed grades and package options, refer to the respective flash datasheets.

The AP configuration scheme in Cyclone IV E devices supports flash speed grades of 40 MHz and above. However, AP configuration for all these speed grades must be capped at 40 MHz. The advantage of faster speed grades is realized when your design in the Cyclone IV E devices accesses flash memory in user mode.

- For more information about the operation of the Micron P30 Parallel NOR and P33 Parallel NOR flash memories, search for the keyword “P30” or “P33” on the Micron website (www.micron.com) to obtain the P30 or P33 family datasheet.

Single-Device AP Configuration

The following groups of interface pins are supported in Micron P30 and P33 flash memories:

- Control pins
- Address pins
- Data pins

The following control signals are from the supported parallel flash memories:

- CLK
- active-low reset (RST#)
- active-low chip enable (CE#)
- active-low output enable (OE#)
- active-low address valid (ADV#)
- active-low write enable (WE#)

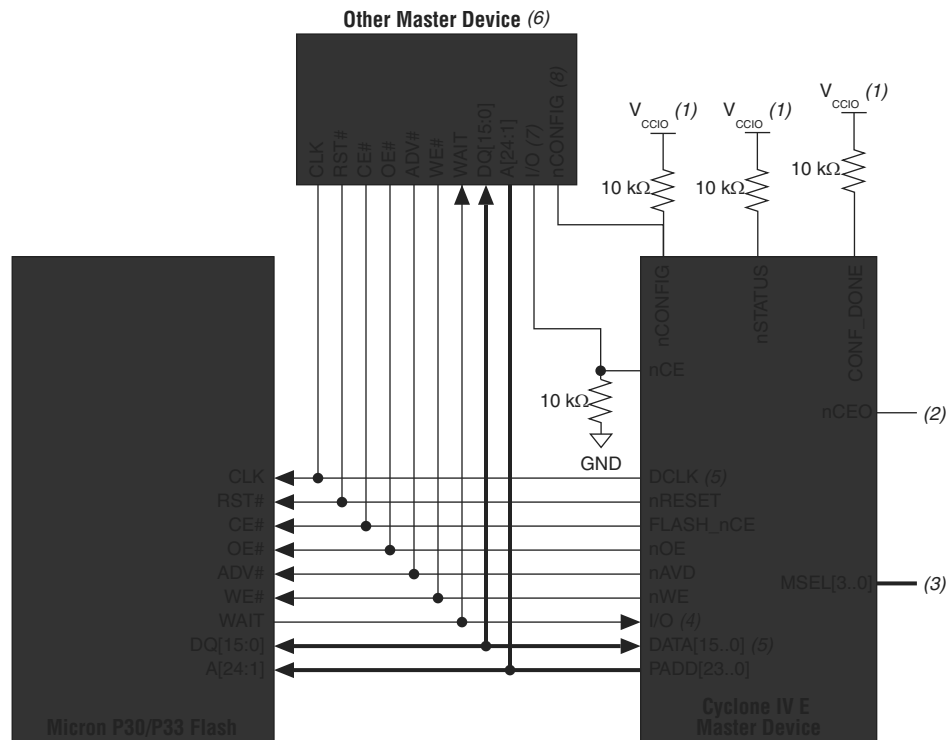
The supported parallel flash memories output a control signal (WAIT) to Cyclone IV E devices to indicate when synchronous data is ready on the data bus. Cyclone IV E devices have a 24-bit address bus connecting to the address bus (A[24:1]) of the flash memory. A 16-bit bidirectional data bus (DATA[15:0]) provides data transfer between the Cyclone IV E device and the flash memory.

The following control signals are from the Cyclone IV E device to flash memory:

- DCLK
- active-low hard reset (nRESET)
- active-low chip enable (FLASH_nCE)
- active-low output enable for the DATA[15:0] bus and WAIT pin (nOE)
- active-low address valid signal and is used to write data into the flash (nAVD)
- active-low write enable and is used to write data into the flash (nWE)

Figure 8–10 shows the AP configuration with multiple bus masters.

Figure 8–10. AP Configuration with Multiple Bus Masters



Notes to Figure 8–10:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3:0], refer to Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.
- (5) When cascading Cyclone IV E devices in a multi-device AP configuration, connect the repeater buffers between the master device and slave devices for DATA[15:0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in “Configuration and JTAG Pin I/O Requirements” on page 8–5.
- (6) The other master device must fit the maximum overshoot equation outlined in “Configuration and JTAG Pin I/O Requirements” on page 8–5.
- (7) The other master device can control the AP configuration bus by driving the nCE to high with an output high on the I/O pin.
- (8) The other master device can pulse nCONFIG if it is under system control and not tied to V_{CCIO}.

- In AP configuration scheme, the only way to re-engage the AP controller is to issue the `ACTIVE_ENGAGE` instruction. In this case, asserting the `nCONFIG` pin does not re-engage either active controller.

ACTIVE_ENGAGE

The `ACTIVE_ENGAGE` instruction allows you to re-engage a disengaged active controller. You can issue this instruction any time during configuration or user mode to re-engage an already disengaged active controller, as well as trigger reconfiguration of the Cyclone IV device in the active configuration scheme.

The `ACTIVE_ENGAGE` instruction functions as the `PULSE_NCONFIG` instruction when the device is in the PS or FPP configuration schemes. The `nCONFIG` pin is disabled when the `ACTIVE_ENGAGE` instruction is issued.



Altera does not recommend using the `ACTIVE_ENGAGE` instruction, but it is provided as a fail-safe instruction for re-engaging the active configuration controller (AS and AP).

Overriding the Internal Oscillator

This feature allows you to override the internal oscillator during the active configuration scheme. The AS and AP configuration controllers use the internal oscillator as the clock source. You can change the clock source to `CLKUSR` through the JTAG instruction.

The `EN_ACTIVE_CLK` and `DIS_ACTIVE_CLK` JTAG instructions toggle on or off whether or not the active clock is sourced from the `CLKUSR` pin or the internal configuration oscillator. To source the active clock from the `CLKUSR` pin, issue the `EN_ACTIVE_CLK` instruction. This causes the `CLKUSR` pin to become the active clock source. When using the `EN_ACTIVE_CLK` instruction, you must enable the internal oscillator for the clock change to occur. By default, the configuration oscillator is disabled after configuration and initialization is complete as well as the device has entered user mode.

However, the internal oscillator is enabled in user mode by any of the following conditions:

- A reconfiguration event (for example, driving the `nCONFIG` pin to go low)
- Remote update is enabled
- Error detection is enabled



When using the `EN_ACTIVE_CLK` and `DIS_ACTIVE_CLK` JTAG instructions to override the internal oscillator, you must clock the `CLKUSR` pin at two times the expected `DCLK` frequency. The `CLKUSR` pin allows a maximum frequency of 40 MHz (40 MHz `DCLK`).

Normally, a test instrument uses the `CLKUSR` pin when it wants to drive its own clock to control the AS state machine.

To revert the clock source back to the configuration oscillator, issue the `DIS_ACTIVE_CLK` instruction. After you issue the `DIS_ACTIVE_CLK` instruction, you must continue to clock the `CLKUSR` pin for 10 clock cycles. Otherwise, even toggling the `nCONFIG` pin does not revert the clock source and reconfiguration does not occur. A POR reverts the clock source back to the configuration oscillator. Toggling the `nCONFIG` pin or driving the JTAG state machine to reset state does not revert the clock source.


Table 8-20. Dedicated Configuration Pins on the Cyclone IV Device (Part 2 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	<ul style="list-style-type: none"> Status output—the target Cyclone IV device drives the CONF_DONE pin low before and during configuration. After all the configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input—after all the data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. <p>Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect bus holds or ADC to CONF_DONE pin.</p>
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the Cyclone IV device with a low signal to allow configuration. You must hold nCE pin low during configuration, initialization, and user-mode. In a single-device configuration, you must tie the nCE pin low. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. You must hold the nCE pin low for successful JTAG programming of the device.
nCEO	N/A if option is on. I/O if option is off.	All	Output open-drain	<p>Output that drives low when configuration is complete. In a single-device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In a multi-device configuration, this pin feeds the nCE pin of the next device. The nCEO of the last device in the chain is left floating or used as a user I/O pin after configuration.</p> <p>If you use the nCEO pin to feed the nCE pin of the next device, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor.</p> <p>If you use the nCEO pin as a user I/O pin after configuration, set the state of the pin on the Dual-Purpose Pin settings.</p>
nCSO, FLASH_nCE (1)	I/O	AS, AP (2)	Output	<p>Output control signal from the Cyclone IV device to the serial configuration device in AS mode that enables the configuration device. This pin functions as nCSO in AS mode and FLASH_nCE in AP mode.</p> <p>Output control signal from the Cyclone IV device to the parallel flash in AP mode that enables the flash. Connects to the CE# pin on the Micron P30 or P33 flash. (2)</p> <p>This pin has an internal pull-up resistor that is always active.</p>

EXTEST_PULSE


The instruction code for EXTEST_PULSE is 0010001111. The EXTEST_PULSE instruction generates three output transitions:


- Driver drives data on the falling edge of TCK in UPDATE_IR/DR.
- Driver drives inverted data on the falling edge of TCK after entering the RUN_TEST/IDLE state.
- Driver drives data on the falling edge of TCK after leaving the RUN_TEST/IDLE state.

 If you use DC-coupling on HSSI signals, you must execute the EXTEST instruction. If you use AC-coupling on HSSI signals, you must execute the EXTEST_PULSE instruction. AC-coupled and DC-coupled HSSI are only supported in post-configuration mode.

EXTEST_TRAIN

The instruction code for EXTEST_TRAIN is 0001001111. The EXTEST_TRAIN instruction behaves the same as the EXTEST_PULSE instruction with one exception. The output continues to toggle on the TCK falling edge as long as the test access port (TAP) controller is in the RUN_TEST/IDLE state.


 These two instruction codes are only supported in post-configuration mode for Cyclone IV GX devices.

 When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

I/O Voltage Support in a JTAG Chain

A Cyclone IV device operating in BST mode uses four required pins: TDI, TDO, TMS, and TCK. The TDO output pin and all JTAG input pins are powered by the V_{CCIO} power supply of I/O Banks (I/O Bank 9 for Cyclone IV GX devices and I/O Bank 1 for Cyclone IV E devices).

A JTAG chain can contain several different devices. However, you must use caution if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specification of the TDI pin it drives. For example, a device with a 3.3-V TDO pin can drive a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin.

 For multiple devices in a JTAG chain with the 3.0-V/3.3-V I/O standard, you must connect a 25-Ω series resistor on a TDO pin driving a TDI pin.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should have a device with a higher V_{CCIO} level driving a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester.

1. Cyclone IV Transceivers Architecture

CYIV-52001-3.7

Cyclone® IV GX devices include up to eight full-duplex transceivers at serial data rates between 600 Mbps and 3.125 Gbps in a low-cost FPGA. Table 1–1 lists the supported Cyclone IV GX transceiver channel serial protocols.

Table 1–1. Serial Protocols Supported by the Cyclone IV GX Transceiver Channels

Protocol	Data Rate (Gbps)	F324 and smaller packages	F484 and larger packages
PCI Express® (PCIe®) (1)	2.5	✓	✓
Gbps Ethernet (GbE)	1.25	✓	✓
Common Public Radio Interface (CPRI)	0.6144, 1.2288, 2.4576, and 3.072	✓ (2)	✓
OBSAI	0.768, 1.536, and 3.072	✓ (2)	✓
XAUI	3.125	—	✓
Serial digital interface (SDI)	HD-SDI at 1.485 and 1.4835	✓	✓
	3G-SDI at 2.97 and 2.967	—	
Serial RapidIO® (SRIO)	1.25, 2.5, and 3.125	—	✓
Serial Advanced Technology Attachment (SATA)	1.5 and 3.0	—	✓
V-by-one	3.125	—	✓
Display Port	1.62 and 2.7	—	✓

Notes to Table 1–1:

- (1) Provides the physical interface for PCI Express (PIPE)-compliant interface that supports Gen1 ×1, ×2, and ×4 initial lane width configurations. When implementing ×1 or ×2 interface, remaining channels in the transceiver block are available to implement other protocols.
- (2) Supports data rates up to 2.5 Gbps only.

You can implement these protocols through the ALTGX MegaWizard™ Plug-In Manager, which also offers the highly flexible Basic functional mode to implement proprietary serial protocols at the following serial data rates:

- 600 Mbps to 2.5 Gbps for devices in F324 and smaller packages
- 600 Mbps to 3.125 Gbps for devices in F484 and larger packages

For descriptions of the ports available when instantiating a transceiver using the ALTGX megafunction, refer to “Transceiver Top-Level Port Lists” on page 1–85.



For more information about Cyclone IV transceivers that run at ≥2.97 Gbps data rate, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

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For example, when operating an EP4CGX150 transmitter channel at 3.125 Gbps without byte serializer, the FPGA fabric frequency is 312.5 MHz (3.125 Gbps/10). This implementation violates the frequency limit and is not supported. Channel operation at 3.125 Gbps is supported when byte serializer is used, where the FPGA fabric frequency is 156.25 MHz (3.125 Gbps/20).

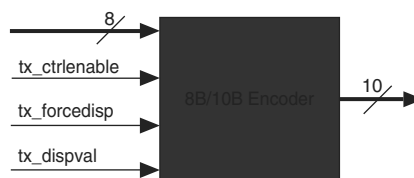
The byte serializer forwards the least significant byte first, followed by the most significant byte.

8B/10B Encoder

The optional 8B/10B encoder generates 10-bit code groups with proper disparity from the 8-bit data and 1-bit control identifier as shown in Figure 1–5.

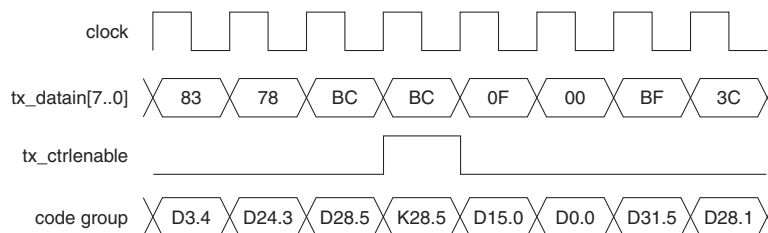
 The encoder is compliant with Clause 36 of the *IEEE 802.3 Specification*.


Figure 1–5. 8B/10B Encoder Block Diagram



The 1-bit control identifier (`tx_ctrlenable`) port controls the 8-bit translation to either a 10-bit data word (`Dx.y`) or a 10-bit control word (`Kx.y`). Figure 1–6 shows the 8B/10B encoding operation with the `tx_ctrlenable` port, where the second 8'hBC data is encoded as a control word when `tx_ctrlenable` port is asserted, while the rest of the data is encoded as a data word.

Figure 1–6. Control and Data Word Encoding with the 8B/10B Encoder



 The IEEE 802.3 8B/10B encoder specification identifies only a set of 8-bit characters for which the `tx_ctrlenable` port should be asserted. If you assert `tx_ctrlenable` port for any other set of characters, the 8B/10B encoder might encode the output 10-bit code as an invalid code (it does not map to a valid `Dx.y` or `Kx.y` code), or an unintended valid `Dx.y` code, depending on the value entered. It is possible for a downstream 8B/10B decoder to decode an invalid control word into a valid `Dx.y` code without asserting any code error flags. Altera recommends not to assert `tx_ctrlenable` port for unsupported 8-bit characters.

Receiver Channel Datapath

The following sections describe the Cyclone IV GX receiver channel datapath architecture as shown in Figure 1-3 on page 1-4:

- “Receiver Input Buffer” on page 1-11
- “Clock Data Recovery” on page 1-15
- “Deserializer” on page 1-16
- “Word Aligner” on page 1-17
- “Deskew FIFO” on page 1-22
- “Rate Match FIFO” on page 1-23
- “8B/10B Decoder” on page 1-23
- “Byte Deserializer” on page 1-24
- “Byte Ordering” on page 1-24
- “RX Phase Compensation FIFO” on page 1-25

Receiver Input Buffer

Table 1-2 lists the electrical features supported by the Cyclone IV GX receiver input buffer.

Table 1-2. Electrical Features Supported by the Receiver Input Buffer

I/O Standard	Programmable Common Mode Voltage (V)	Coupling
1.4-V PCML	0.82	AC, DC
1.5-V PCML	0.82	AC, DC
2.5-V PCML	0.82	AC
LVPECL	0.82	AC
LVDS	0.82	AC, DC ⁽¹⁾

Note to Table 1-2:

(1) DC coupling is supported for **LVDS** with lower on-chip common mode voltage of 0.82 V.

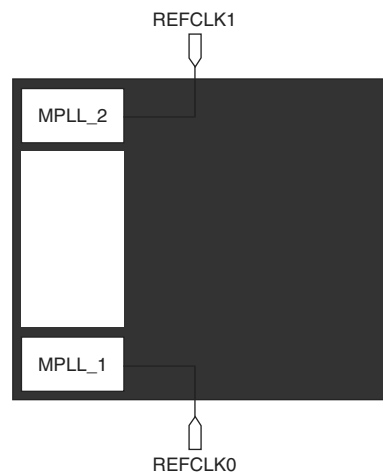
Input Reference Clocking

When used for transceiver, the left PLLs synthesize the input reference clock to generate the required clocks for the transceiver channels. Figure 1–25 and Figure 1–26 show the sources of input reference clocks for PLLs used in the transceiver operation.



Clock output from PLLs in the FPGA core cannot feed into PLLs used by the transceiver as input reference clock.

Figure 1–25. PLL Input Reference Clocks in Transceiver Operation for F324 and Smaller Packages ^{(1), (2)}



Notes to Figure 1–25:

- (1) The REFCLK0 and REFCLK1 pins are dual-purpose CLK, REFCLK, or DIFFCLK pins that reside in banks 3A and 8A respectively.
- (2) Using any clock input pins other than the designated REFCLK pins as shown here to drive the MPLLs may have reduced jitter performance.

Clock Rate Compensation

In XAUI mode, the rate match FIFO compensates up to ± 100 ppm (200 ppm total) difference between the upstream transmitter and the local receiver reference clock. The XAUI protocol requires the transmitter to send /R/ (/K28.0/) code groups simultaneously on all four lanes (denoted as ||R|| column) during inter-packet gaps, adhering to rules listed in the IEEE P802.3ae specification.

The rate match operation begins after rx_syncstatus and rx_channelaligned are asserted. The rx_syncstatus signal is from the word aligner, indicating that synchronization is acquired on all four channels, while rx_channelaligned signal is from the deskew FIFO, indicating channel alignment.

The rate match FIFO looks for the ||R|| column (simultaneous /R/ code groups on all four channels) and deletes or inserts ||R|| columns to prevent the rate match FIFO from overflowing or under running. The rate match FIFO can insert or delete as many ||R|| columns as necessary to perform the rate match operation.

The rx_rmfiodeleted and rx_rmfiodeinserted flags that indicate rate match FIFO deletion and insertion events, respectively, are forwarded to the FPGA fabric. If an ||R|| column is deleted, the rx_rmfiodeleted flag from each of the four channels goes high for one clock cycle per deleted ||R|| column. If an ||R|| column is inserted, the rx_rmfiodeinserted flag from each of the four channels goes high for one clock cycle per inserted ||R|| column.




The rate match FIFO does not insert or delete code groups automatically to overcome FIFO empty or full conditions. In this case, the rate match FIFO asserts the rx_rmfiodefull and rx_rmfiodeempty flags for at least three recovered clock cycles to indicate rate match FIFO full and empty conditions, respectively. You must then assert the rx_digitalreset signal to reset the receiver PCS blocks.

Deterministic Latency Mode

Deterministic Latency mode provides the transceiver configuration that allows no latency uncertainty in the datapath and features to strictly control latency variation. This mode supports non-bonded ($\times 1$) and bonded ($\times 4$) channel configurations, and is typically used to support CPRI and OBSAI protocols that require accurate delay measurements along the datapath. The Cyclone IV GX transceivers configured in Deterministic Latency mode provides the following features:

- registered mode phase compensation FIFO
- receive bit-slip indication
- transmit bit-slip control
- PLL PFD feedback

 The busy signal remains low for the first `reconfig_clk` clock cycle. It then gets asserted from the second `reconfig_clk` clock cycle. Subsequent deassertion of the busy signal indicates the completion of the offset cancellation process. This busy signal is required in transceiver reset sequences except for transmitter only channel configurations. Refer to the reset sequences shown in Figure 2–2 and the associated references listed in the notes for the figure.


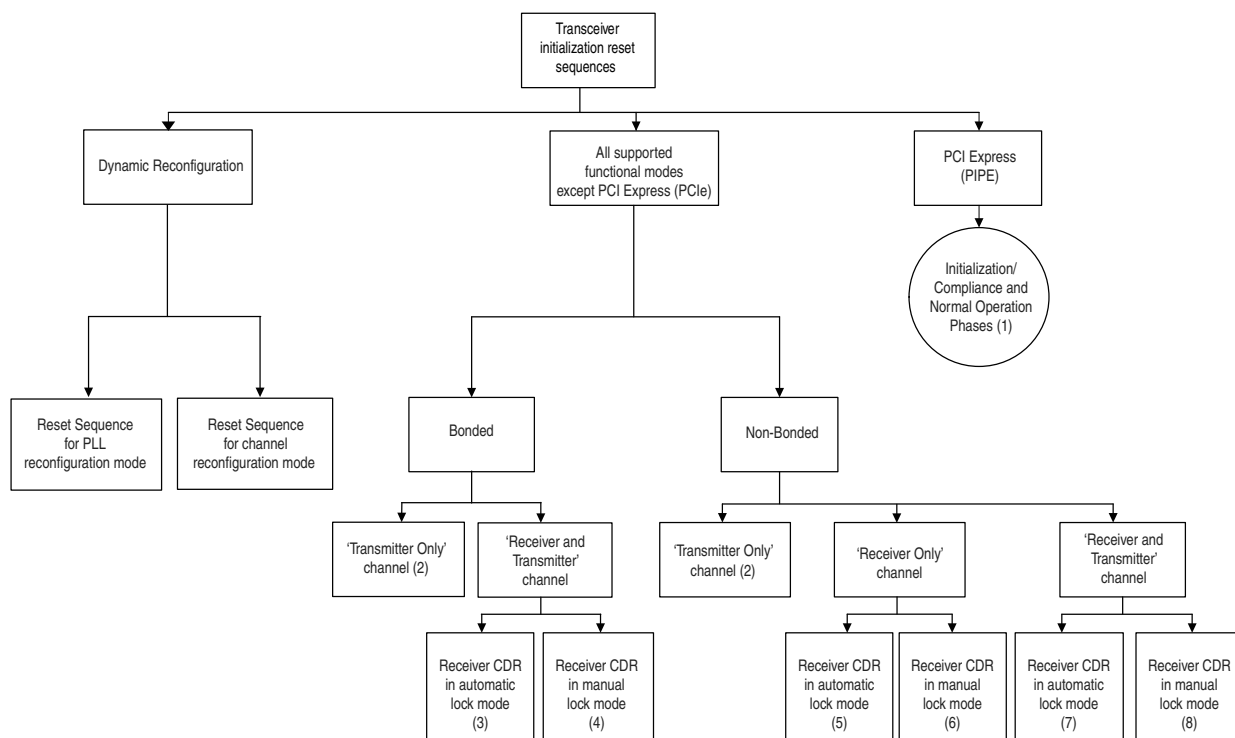
 Altera strongly recommends adhering to these reset sequences for proper operation of the Cyclone IV GX transceiver.

Figure 2–2 shows the transceiver reset sequences for Cyclone IV GX devices.

Figure 2–2. Transceiver Reset Sequences Chart



Notes to Figure 2–2:

- (1) Refer to the Timing Diagram in Figure 2–10.
- (2) Refer to the Timing Diagram in Figure 2–3.
- (3) Refer to the Timing Diagram in Figure 2–4.
- (4) Refer to the Timing Diagram in Figure 2–5.
- (5) Refer to the Timing Diagram in Figure 2–6.
- (6) Refer to the Timing Diagram in Figure 2–7.
- (7) Refer to the Timing Diagram in Figure 2–8.
- (8) Refer to the Timing Diagram in Figure 2–9.

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