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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	963
Number of Logic Elements/Cells	15408
Total RAM Bits	516096
Number of I/O	343
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce15f23c8

Cyclone IV Device Family Speed Grades

Table 1-5 lists the Cyclone IV GX devices speed grades.

Table 1-5. Speed Grades for the Cyclone IV GX Device Family

Device	F169	F324	F484	F672	F896
EP4CGX15	C6, C7, C8, I7	—	—	—	—
EP4CGX22	C6, C7, C8, I7	C6, C7, C8, I7	—	—	—
EP4CGX30	C6, C7, C8, I7	C6, C7, C8, I7	C6, C7, C8, I7	—	—
EP4CGX50	—	—	C6, C7, C8, I7	C6, C7, C8, I7	—
EP4CGX75	—	—	C6, C7, C8, I7	C6, C7, C8, I7	—
EP4CGX110	—	—	C7, C8, I7	C7, C8, I7	C7, C8, I7
EP4CGX150	—	—	C7, C8, I7	C7, C8, I7	C7, C8, I7

Table 1-6 lists the Cyclone IV E devices speed grades.

Table 1-6. Speed Grades for the Cyclone IV E Device Family ⁽¹⁾, ⁽²⁾

Device	E144	M164	M256	U256	F256	F324	U484	F484	F780
EP4CE6	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	—	—
EP4CE10	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	—	—
EP4CE15	C8L, C9L, I8L C6, C7, C8, I7	I7N	C7N, I7N	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	C8L, C9L, I8L C6, C7, C8, I7, A7	—
EP4CE22	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	—	—	—	—
EP4CE30	—	—	—	—	—	A7N	—	C8L, C9L, I8L C6, C7, C8, I7, A7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE40	—	—	—	—	—	A7N	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE55	—	—	—	—	—	—	I7N	C8L, C9L, I8L C6, C7, C8, I7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE75	—	—	—	—	—	—	I7N	C8L, C9L, I8L C6, C7, C8, I7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE115	—	—	—	—	—	—	—	C8L, C9L, I8L C7, C8, I7	C8L, C9L, I8L C7, C8, I7

Notes to Table 1-6:

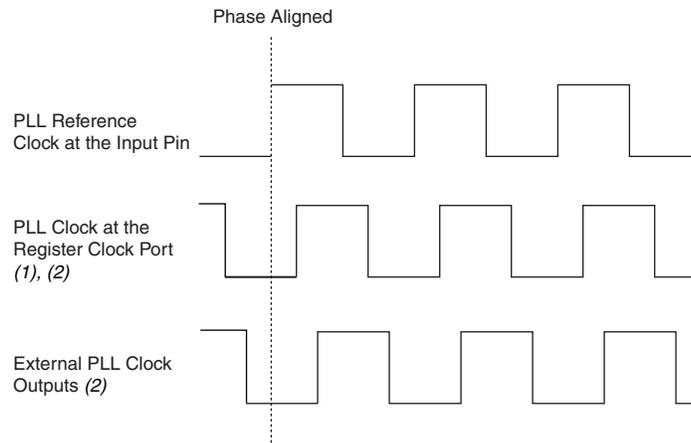
- (1) C8L, C9L, and I8L speed grades are applicable for the 1.0-V core voltage.
- (2) C6, C7, C8, I7, and A7 speed grades are applicable for the 1.2-V core voltage.

No Compensation Mode

In no compensation mode, the PLL does not compensate for any clock networks. This provides better jitter performance because clock feedback into the PFD does not pass through as much circuitry. Both the PLL internal and external clock outputs are phase shifted with respect to the PLL clock input.

Figure 5-13 shows a waveform example of the phase relationship of the PLL clock in this mode.

Figure 5-13. Phase Relationship Between PLL Clocks in No Compensation Mode



Notes to Figure 5-13:

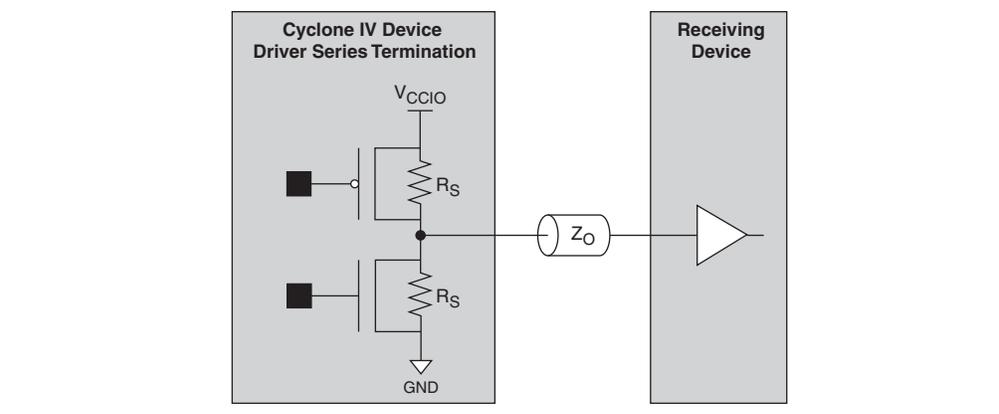
- (1) Internal clocks fed by the PLL are phase-aligned to each other.
- (2) The PLL clock outputs can lead or lag the PLL input clocks.

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock output pin has a phase delay relative to the clock input pin if connected in this mode. The Quartus II software timing analyzer reports any phase difference between the two. In normal mode, the PLL fully compensates the delay introduced by the GCLK network.

Figure 6-4 shows the single-ended I/O standards for OCT without calibration. The R_S shown is the intrinsic transistor impedance.

Figure 6-4. Cyclone IV Devices R_S OCT Without Calibration



All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

R_S OCT is supported on any I/O bank. V_{CCI0} and V_{REF} must be compatible for all I/O pins to enable R_S OCT in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCI0} and V_{REF} do not conflict.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage, and temperature.

 For more information about tolerance specification, refer to the *Cyclone IV Device Datasheet* chapter.

I/O Standards

Cyclone IV devices support multiple single-ended and differential I/O standards. Cyclone IV devices support 3.3-, 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V I/O standards.

Table 6-3 summarizes I/O standards supported by Cyclone IV devices and which I/O pins support them.

Table 6-3. Cyclone IV Devices Supported I/O Standards and Constraints (Part 1 of 3)

I/O Standard	Type	Standard Support	V_{CCI0} Level (in V)		Column I/O Pins			Row I/O Pins ⁽¹⁾	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
3.3-V LVTTTL, 3.3-V LVCMOS ⁽²⁾	Single-ended	JESD8-B	3.3/3.0/2.5 ⁽³⁾	3.3	✓	✓	✓	✓	✓
3.0-V LVTTTL, 3.0-V LVCMOS ⁽²⁾	Single-ended	JESD8-B	3.3/3.0/2.5 ⁽³⁾	3.0	✓	✓	✓	✓	✓

External Memory Interfacing

Cyclone IV devices support I/O standards required to interface with a broad range of external memory interfaces, such as DDR SDRAM, DDR2 SDRAM, and QDR II SRAM.

-  For more information about Cyclone IV devices external memory interface support, refer to the *External Memory Interfaces in Cyclone IV Devices* chapter.

Pad Placement and DC Guidelines

You can use the Quartus II software to validate your pad and pin placement.

Pad Placement

Altera recommends that you create a Quartus II design, enter your device I/O assignments and compile your design to validate your pin placement. The Quartus II software checks your pin connections with respect to the I/O assignment and placement rules to ensure proper device operation. These rules depend on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this chapter.

-  For more information about how the Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

DC Guidelines

For the Quartus II software to automatically check for illegally placed pads according to the DC guidelines, set the DC current sink or source value to **Electromigration Current** assignment on each of the output pins that are connected to the external resistive load.

The programmable current strength setting has an impact on the amount of DC current that an output pin can source or sink. Determine if the current strength setting is sufficient for the external resistive load condition on the output pin.

Clock Pins Functionality

Cyclone IV clock pins have multiple purposes, as per listed:

- CLK pins—Input support for single-ended and voltage-referenced standards. For I/O standard support, refer to [Table 6-3 on page 6-11](#).
- DIFFCLK pins—Input support for differential standards. For I/O standard support, refer to [Table 6-3 on page 6-11](#). When used as DIFFCLK pins, DC or AC coupling can be used depending on the interface requirements and external termination is required. For more information, refer to [“High-Speed I/O Standards Support” on page 6-28](#).
- REFCLK pins—Input support for high speed differential reference clocks used by the transceivers in Cyclone IV GX devices. For I/O support, coupling, and termination requirements, refer to [Table 6-10 on page 6-29](#).

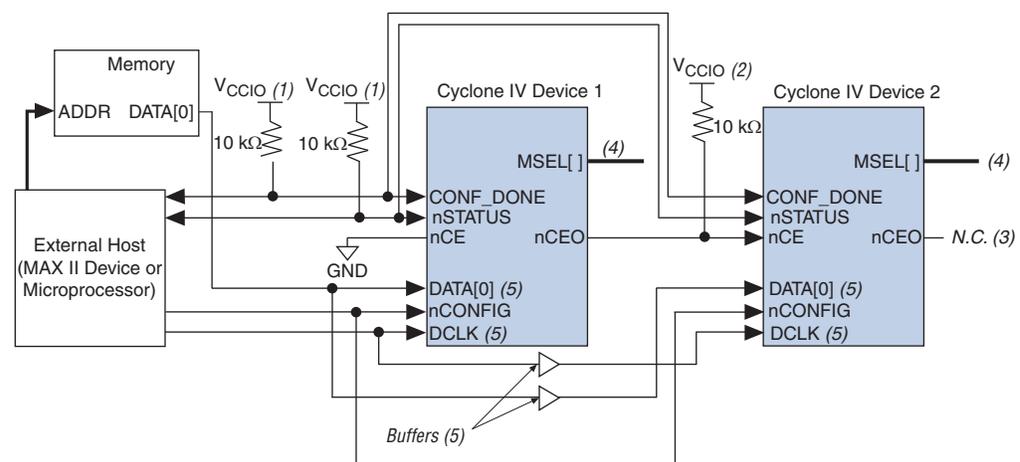
To ensure DCLK and DATA [0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA [0] pin is available as a user I/O pin after configuration. In the PS scheme, the DATA [0] pin is tri-stated by default in user mode and must be driven by the external host device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified system frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

The external host device can also monitor CONF_DONE and INIT_DONE to ensure successful configuration. The CONF_DONE pin must be monitored by the external device to detect errors and to determine when programming is complete. If all configuration data is sent, but CONF_DONE or INIT_DONE has not gone high, the external device must reconfigure the target device.

Figure 8-14 shows how to configure multiple devices using an external host device. This circuit is similar to the PS configuration circuit for a single device, except that Cyclone IV devices are cascaded for multi-device configuration.

Figure 8-14. Multi-Device PS Configuration Using an External Host



Notes to Figure 8-14:

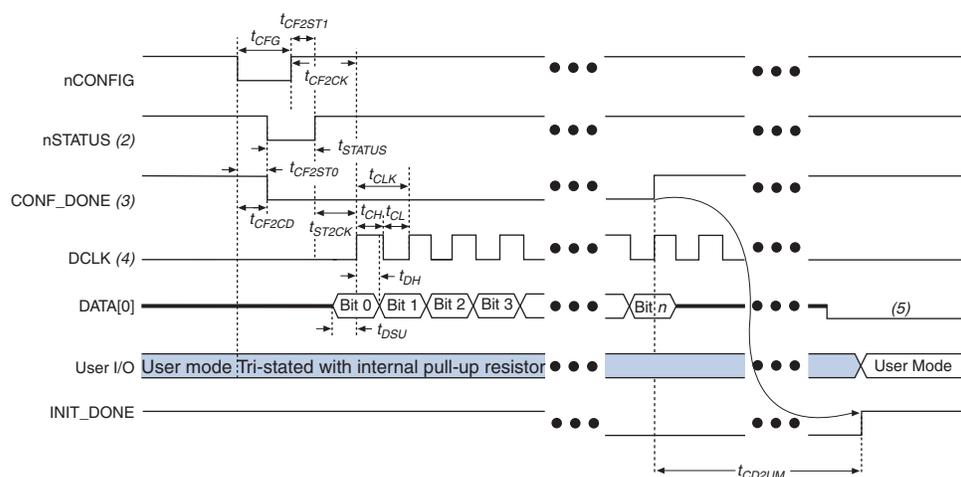
- (1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.
- (2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.
- (3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8-3 on page 8-8, Table 8-4 on page 8-8, and Table 8-5 on page 8-9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA [0] and DCLK must fit the maximum overshoot outlined in Equation 8-1 on page 8-5.

PS Configuration Timing

A PS configuration must meet the setup and hold timing parameters and the maximum clock frequency. When using a microprocessor or another intelligent host to control the PS interface, ensure that you meet these timing requirements.

Figure 8-16 shows the timing waveform for PS configuration when using an external host device.

Figure 8-16. PS Configuration Timing Waveform (1)



Notes to Figure 8-16:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power up, the Cyclone IV device holds nSTATUS low during POR delay.
- (3) After power up, before and during configuration, CONF_DONE is low.
- (4) In user mode, drive DCLK either high or low when using the PS configuration scheme, whichever is more convenient. When using the AS configuration scheme, DCLK is a Cyclone IV device output pin and must not be driven externally.
- (5) Do not leave the DATA [0] pin floating after configuration. Drive the DATA [0] pin high or low, whichever is more convenient.

Table 8-12 lists the PS configuration timing parameters for Cyclone IV devices.

Table 8-12. PS Configuration Timing Parameters For Cyclone IV Devices (Part 1 of 2)

Symbol	Parameter	Minimum		Maximum		Unit
		Cyclone IV (1)	Cyclone IV E (2)	Cyclone IV (1)	Cyclone IV E (2)	
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	—	500	—	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	—	500	—	ns
t _{CFG}	nCONFIG low pulse width	500	—	—	—	ns
t _{STATUS}	nSTATUS low pulse width	45	—	230 (3)	—	μs

FPP Configuration

The FPP configuration in Cyclone IV devices is designed to meet the increasing demand for faster configuration time. Cyclone IV devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

You can perform FPP configuration of Cyclone IV devices with an intelligent host, such as a MAX II device or microprocessor with flash memory. If your system already contains a CFI flash memory, you can use it for the Cyclone IV device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone IV device.



For more information about the PFL, refer to [AN 386: Using the Parallel Flash Loader with the Quartus II Software](#).



FPP configuration is supported in EP4CGX30 (only for F484 package), EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150, and all Cyclone IV E devices.



The FPP configuration is not supported in E144 package of Cyclone IV E devices.



Cyclone IV devices do not support enhanced configuration devices for FPP configuration.

FPP Configuration Using an External Host

FPP configuration using an external host provides a fast method to configure Cyclone IV devices. In the FPP configuration scheme, you can use an external host device to control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone IV device. You can store configuration data in an **.rbf**, **.hex**, or **.tff** format. When using the external host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to

Remote System Upgrade Mode

In remote update mode, Cyclone IV devices load the factory configuration image after power up. The user-defined factory configuration determines the application configuration to be loaded and triggers a reconfiguration cycle. The factory configuration can also contain application logic.

When used with configuration memory, the remote update mode allows an application configuration to start at any flash sector boundary. Additionally, the remote update mode features a user watchdog timer that can detect functional errors in an application configuration.

Remote Update Mode

In AS configuration scheme, when a Cyclone IV device is first powered up in remote update, it loads the factory configuration located at address `boot_address[23:0] = 24b'0`. Altera recommends storing the factory configuration image for your system at boot address `24b'0`, which corresponds to the start address location `0x000000` in the serial configuration device. A factory configuration image is a bitstream for the Cyclone IV device in your system that is programmed during production and is the fall-back image when an error occurs. This image is stored in non-volatile memory and is never updated or modified using remote access.

When you use the AP configuration in Cyclone IV E devices, the Cyclone IV E device loads the default factory configuration located at the following address after device power-up in remote update mode:

```
boot_address[23:0] = 24'h010000 = 24'b1 0000 0000 0000 0000.
```

You can change the default factory configuration address to any desired address using the `APFC_BOOT_ADDR JTAG` instruction. The factory configuration image is stored in non-volatile memory and is never updated or modified using remote access. This corresponds to the default start address location `0x010000` represented in 16-bit word addressing (or the updated address if the default address is changed) in the supported parallel flash memory. For more information about the application of the `APFC_BOOT_ADDR JTAG` instruction in AP configuration scheme, refer to the [“JTAG Instructions” on page 8-57](#).

The factory configuration image is user-designed and contains soft logic (Nios II processor or state machine and the remote communication interface) to:

- Process any errors based on status information from the dedicated remote system upgrade circuitry
- Communicate with the remote host and receive new application configurations and store the new configuration data in the local non-volatile memory device
- Determine the application configuration to be loaded into the Cyclone IV device
- Enable or disable the user watchdog timer and load its time-out value (optional)
- Instruct the dedicated remote system upgrade circuitry to start a reconfiguration cycle

Configuration error detection determines if the configuration data received through an external memory device is corrupted during configuration. To validate the configuration data, the Quartus® II software uses a function to calculate the CRC value for each configuration data frame and stores the frame-based CRC value in the configuration data as part of the configuration bit stream.

During configuration, Cyclone IV devices use the same methodology to calculate the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or all the values are calculated.

In addition to the frame-based CRC value, the Quartus II software generates a 32-bit CRC value for the whole configuration bit stream. This 32-bit CRC value is stored in the 32-bit storage register at the end of the configuration and is used for user mode error detection that is discussed in “[User Mode Error Detection](#)”.

User Mode Error Detection

 User mode error detection is available in Cyclone IV GX and Cyclone IV E devices with 1.2-V core voltage. Cyclone IV E devices with 1.0-V core voltage do not support user mode error detection.

Soft errors are changes in a configuration random-access memory (CRAM) bit state due to an ionizing particle. Cyclone IV devices have built-in error detection circuitry to detect data corruption by soft errors in the CRAM cells.

This error detection capability continuously computes the CRC of the configured CRAM bits based on the contents of the device and compares it with the pre-calculated CRC value obtained at the end of the configuration. If the CRCs match, there is no error in the current configuration CRAM bits. The process of error detection continues until the device is reset (by setting `nCONFIG` to low).

The Cyclone IV device error detection feature does not check memory blocks and I/O buffers. These device memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection because the configuration data uses flip-flops as storage elements that are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.

The error detection circuitry in Cyclone IV devices uses a 32-bit CRC IEEE 802 standard and a 32-bit polynomial as the CRC generator. Therefore, a single 32-bit CRC calculation is performed by the device. If a soft error does not occur, the resulting 32-bit signature value is `0x00000000`, that results in a 0 on the `CRC_ERROR` output signal. If a soft error occurs in the device, the resulting signature value is non-zero and the `CRC_ERROR` output signal is 1.

You can inject a soft error by changing the 32-bit CRC storage register in the CRC circuitry. After verifying the induced failure, you can restore the 32-bit CRC value to the correct CRC value with the same instruction and inserting the correct value.

 Before updating it with a known bad value, Altera recommends reading out the correct value.

Document Revision History

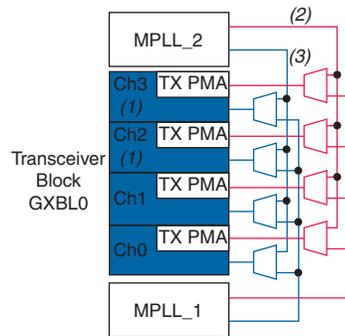
Table 10-3 lists the revision history for this chapter.

Table 10-3. Document Revision History

Date	Version	Changes
December 2013	1.3	<ul style="list-style-type: none">■ Updated the “EXTEST_PULSE” section.
November 2011	1.2	<ul style="list-style-type: none">■ Updated the “BST Operation Control” section.■ Updated Table 10-2.
February 2010	1.1	<ul style="list-style-type: none">■ Added Cyclone IV E devices in Table 10-1 and Table 10-2 for the Quartus II software version 9.1 SP1 release.■ Updated Figure 10-1 and Figure 10-2.■ Minor text edits.
November 2009	1.0	Initial release.

Figure 1-31 and Figure 1-32 show the high- and low-speed clock distribution for transceivers in F324 and smaller packages, and in F484 and larger packages in non-bonded channel configuration.

Figure 1-31. Clock Distribution in Non-Bonded Channel Configuration for Transceivers in F324 and Smaller Packages

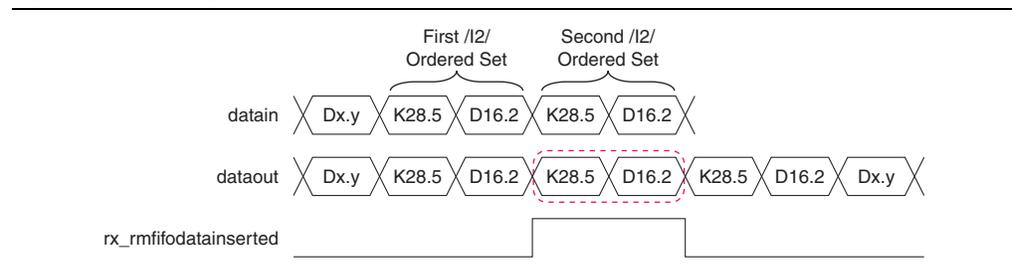


Notes to Figure 1-31:

- (1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
- (2) High-speed clock.
- (3) Low-speed clock.

Figure 1–59 shows an example of rate match FIFO insertion in the case where one symbol must be inserted. Because the rate match FIFO can only insert $/I2/$ ordered sets, it inserts one $/I2/$ ordered set (two symbols inserted).

Figure 1–59. Example of Rate Match FIFO Insertion in GIGE Mode



 The rate match FIFO does not insert or delete code groups automatically to overcome FIFO empty or full conditions. In this case, the rate match FIFO asserts the `rx_rmifofull` and `rx_rmifoempty` flags for at least two recovered clock cycles to indicate rate match FIFO full and empty conditions, respectively. You must then assert the `rx_digitalreset` signal to reset the receiver PCS blocks.

Serial RapidIO Mode

Serial RapidIO mode provides the non-bonded ($\times 1$) transceiver channel datapath configuration for SRIO protocol implementation. The Cyclone IV GX transceiver provides the PMA and the following PCS functions:

- 8B/10B encoding and decoding
- lane synchronization state machine

 Cyclone IV GX transceivers do not have built-in support for some PCS functions such as pseudo-random idle sequence generation and lane alignment in $\times 4$ bonded channel configuration. If required, you must implement these functions in a user logics or external circuits.

The RapidIO Trade Association defines a high-performance, packet-switched interconnect standard to pass data and control information between microprocessors, digital signals, communications, network processes, system memories, and peripheral devices. The SRIO physical layer specification defines serial protocol running at 1.25 Gbps, 2.5 Gbps, and 3.125 Gbps in either single-lane ($\times 1$) or bonded four-lane ($\times 4$) at each line rate. Cyclone IV GX transceivers support single-lane ($\times 1$) configuration at all three line rates. Four $\times 1$ channels configured in Serial RapidIO mode can be instantiated to achieve one non-bonded $\times 4$ SRIO link. When implementing four $\times 1$ SRIO channels, the receivers do not have lane alignment or deskew capability.

Table 2–2 lists the power-down signals available for each transceiver block.

Table 2–2. Transceiver Block Power-Down Signals

Signal	Description
pll_areset	Resets the transceiver PLL. The <code>pll_areset</code> signal is asserted in two conditions: <ul style="list-style-type: none"> During reset sequence, the signal is asserted to reset the transceiver PLL. This signal is controlled by the user. After the transceiver PLL is reconfigured, the signal is asserted high by the <code>ALTPLL_RECONFIG</code> controller. This signal is not controlled by the user.
gxb_powerdown	Powers down the entire transceiver block. When this signal is asserted, this signal powers down the PCS and PMA in all the transceiver channels. This signal operates independently from the other reset signals. This signal is common to the transceiver block.
pll_locked	A status signal. Indicates the status of the transmitter multipurpose PLLs or general purpose PLLs. <ul style="list-style-type: none"> A high level—indicates the multipurpose PLL or general purpose PLL is locked to the incoming reference clock frequency.
rx_freqlocked	A status signal. Indicates the status of the receiver CDR lock mode. <ul style="list-style-type: none"> A high level—the receiver is in lock-to-data mode. A low level—the receiver CDR is in lock-to-reference mode.
busy	A status signal. An output from the <code>ALTGX_RECONFIG</code> block indicates the status of the dynamic reconfiguration controller. This signal remains low for the first <code>reconfig_clk</code> clock cycle after power up. It then gets asserted from the second <code>reconfig_clk</code> clock cycle. Assertion on this signal indicates that the offset cancellation process is being executed on the receiver buffer as well as the receiver CDR. When this signal is deasserted, it indicates that offset cancellation is complete. This busy signal is also used to indicate the dynamic reconfiguration duration such as in analog reconfiguration mode and channel reconfiguration mode.

 For more information about offset cancellation, refer to the *Cyclone IV Dynamic Reconfiguration* chapter.

 If none of the channels is instantiated in a transceiver block, the Quartus® II software automatically powers down the entire transceiver block.

Blocks Affected by the Reset and Power-Down Signals

Table 2–3 lists the blocks that are affected by specific reset and power-down signals.

Table 2–3. Blocks Affected by Reset and Power-Down Signals (Part 1 of 2)

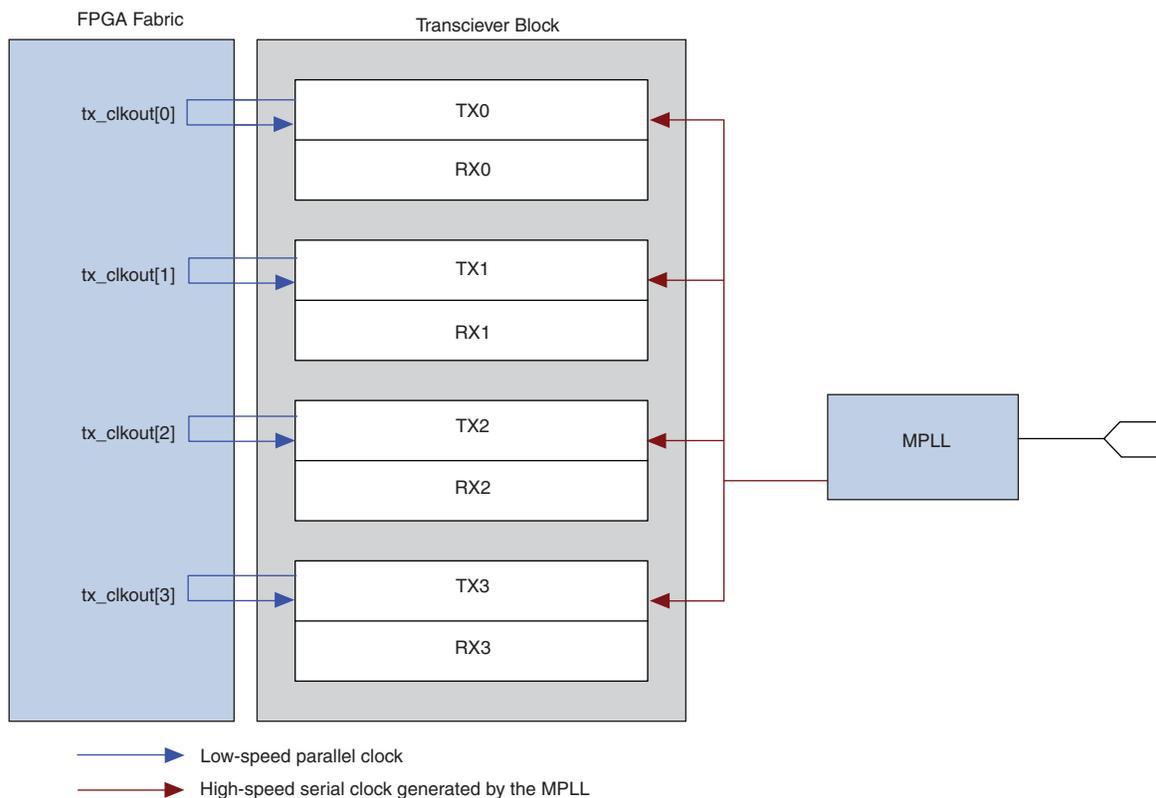
Transceiver Block	rx_digitalreset	rx_analogreset	tx_digitalreset	pll_areset	gxb_powerdown
multipurpose PLLs and general purpose PLLs	—	—	—	✓	—
Transmitter Phase Compensation FIFO	—	—	✓	—	✓
Byte Serializer	—	—	✓	—	✓
8B/10B Encoder	—	—	✓	—	✓

Option 2: Use the Respective Channel Transmitter Core Clocks

- Enable this option if you want the individual transmitter channel `tx_clkout` signals to provide the write clock to their respective Transmit Phase Compensation FIFOs.
- This option is typically enabled when each transceiver channel is reconfigured to a different functional mode using channel reconfiguration.

Figure 3-12 shows how each transmitter channel's `tx_clkout` signal provides a clock to the Transmit Phase Compensation FIFOs of the respective transceiver channels.

Figure 3-12. Option 2 for Transmitter Core Clocking (Channel Reconfiguration Mode)



Receiver core clocking refers to the clock that is used to read the parallel data from the Receiver Phase Compensation FIFO into the FPGA fabric. You can use one of the following clocks to read from the Receive Phase Compensation FIFO:

- `rx_coreclk`—you can use a clock of the same frequency as `rx_clkout` from the FPGA fabric to provide the read clock to the Receive Phase Compensation FIFO. If you use `rx_coreclk`, it overrides the `rx_clkout` options in the ALTGX MegaWizard Plug-In Manager.
- `rx_clkout`—the Quartus II software automatically routes `rx_clkout` to the FPGA fabric and back into the Receive Phase Compensation FIFO.

Table 1-23 lists the Cyclone IV GX transceiver block AC specifications.

Table 1-23. Transceiver Block AC Specification for Cyclone IV GX Devices ^{(1), (2)}

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Transmit Jitter Generation ⁽³⁾											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCIe Receiver Jitter Tolerance ⁽³⁾											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			UI
GIGE Transmit Jitter Generation ⁽⁴⁾											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance ⁽⁴⁾											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Notes to Table 1-23:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1-24 lists the clock tree specifications for Cyclone IV devices.

Table 1-24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)

Device	Performance								Unit
	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	I7	I8L ⁽¹⁾	A7	
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz

Table 1-35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t _{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1-35:

- (1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1-36. LVDS Receiver Timing Specifications for Cyclone IV Devices ^{(1), (3)}

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{HCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	—	400	—	400	—	400	—	550	—	640	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	—	700	ps
t _{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1-36:

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

